TECHNOLOGY TODAY

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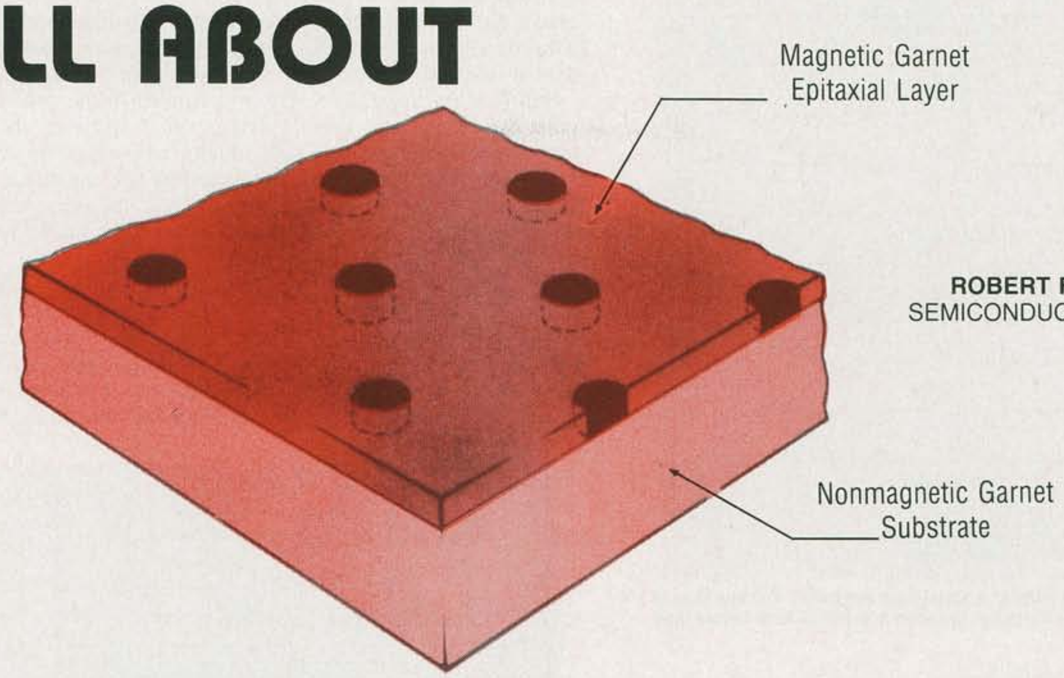

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BUBBLE MEMORY DEVICES

Bubble memories feature the read/write abilities of RAM's, the non-volatility of ROM's, and the mass-storage capabilities of a tape or disk-storage system. This month we'll look at the architecture of those devices and how they work.

Part 2 IN LAST MONTH'S ISSUE, WE INTRODUCED bubble memory devices and saw that bubbles are microscopic magnetic domains in a molecular-thin film of synthetic garnet. These bubbles are only a few micrometers (μm's) in diameter and can be moved about in the film by establishing and controlling a magnetic field across the film. The presence of a bubble at a given location corresponds to a binary "1" and the absence of a bubble corresponds to a binary "0".

In that discussion, we covered the basic theory and development of the magnetic bubble; showing how it is generated, annihilated, and replicated or transferred from one track to another. We left you with a brief word on the serial loop—the simplest of several bubble memory architectural schemes that have been developed.

The serial-loop track is a long serpentine arrangement as shown in Fig. 9. Bubbles produced by pulsing the generator travel in series around the loop. A bubble reaching the replicator splits in two. One goes to the detector and generates a current pulse that is read as a binary bit. The other bubble either remains in storage, continuing to circulate around the loop, or is erased by the annihilator and is replaced by new data from the generator. All gates used to generate, replicate, detect and erase data are called function gates.

The serial loop is seldom used because of the long access time associated with this scheme. The bubbles must circle around the loop before they can be read. For example, the Fujitsu 64K-bit serial-loop type FMB31DB device has a 370-ms access time while the 64K-bit FBM32A using a major/minor-loop scheme (that we will discuss shortly) requires an access time of only 4.3 ms.

A second disadvantage of the serial-loop system is that production yield is much lower than with other schemes that have been developed. A single defect in any part of a serial loop is cause for rejecting the chip. The other architectural systems that have been developed have greater tolerances for defects in the manufacturing process.

In our earlier story, we showed how bubbles are stretched before being read out by the detector. In an actual bubble memory device, two sets of detector elements are used in a differential detector that eliminates the effect of the rotating magnetic field.

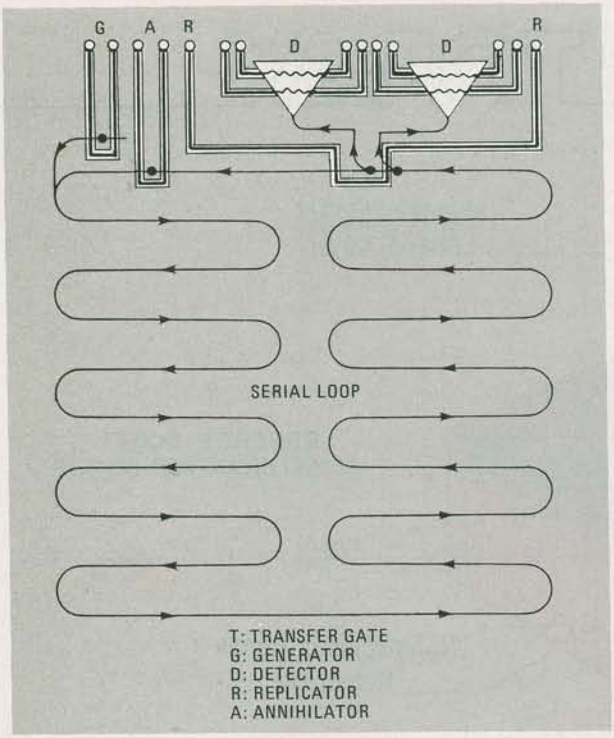

FIG. 9—LOOP ORGANIZATION of a serial-loop memory. Access time is long because bubbles must circulate in series around the loop before they can be read.

Major/minor loop architecture

The major/minor loop system is arranged in a serial-parallel-serial structure—serial input, parallel-loop storage, and serial output. A continuous major loop shift-register feeds into and out of the device while the large number of minor loops serve mainly for storage.

The minor loops are perpendicular and closely adjacent to the major loop. Thus, data generated and placed on the major loop can be loaded simultaneously and in parallel into the top positions of the minor loops for storage. Similarly, the minor loops can be rotated so the desired data blocks can be shifted back to the major loop to be read out.

A typical bubble memory device using a major/minor loop architecture (Motorola's MBM2256, for example) has 282 minor loops, each consisting of 1024 bit positions. Such a device has a potential of 288,768 bits. It will be operated with only 256 active minor loops in the memory. The 26 extra loops are designed into the chip structure to allow for possible manufacturing defects in several loops. In this way, a chip with several defective minor loops can still be used. This greatly increases production yield over that of the serial-loop design. With 256 active loops, we have a 256K memory with a capacity of 262,144 bits.

The locations of defective minor loops are stored in a PROM that is a part of the control circuitry. Data cannot be stored in or read out of a defective loop.

There are three different implementations of the major/minor loop architecture. These implementations are referred to as *transfer gate*, *block replicator transfer*, and *block replicator swap* systems.

The transfer-gate system of major/minor loop organization (see Fig. 10) consists of a major loop to write and read the information and transfer data bits to and from the minor storage loops upon demand. The minor loops are connected to transfer gates at alternate bit positions along the major loop. Information being fed in is loaded on the major loop in alternate bit positions.

Before data can be entered into a particular location, the old information in the minor loops at the desired address is conveyed to their respective loop exits and then transferred or dumped simultaneously into the major loop in what is called a transfer-out operation. The information bits are circulated in succession to the annihilator where they are erased to make room for incoming data from the generator. The data bits entered on the major loop are shifted around until the first data bit is at the entrance to the first minor loop, the second data bit is at the entrance to the second minor loop and so on. Finally, the transfer gate is pulsed and the new data is dumped into the minor loops in a transfer-in operation. The control circuitry assures that the new data is inserted in the "slot" vacated by the old information.

Information to be retrieved is circulated in the minor loop until they are in the correct exit position and then they are transferred simultaneously to the major loop when the transfer gate is pulsed. The data is duplicated by the replicator. One string of data bits is read by the detector; the other string is returned through the transfer gate to the proper address in the minor loops.

The transfer-gate system of major/minor loop architecture provides a fast, reliable system. But—access time is not fast enough for many applications. This is because of the alternate-bit spacing between minor loops. This design also calls for a rather large chip. These disadvantages are eliminated in the block-replicator transfer system shown in Fig. 11 and the block-replicator swap system shown in Fig. 12.

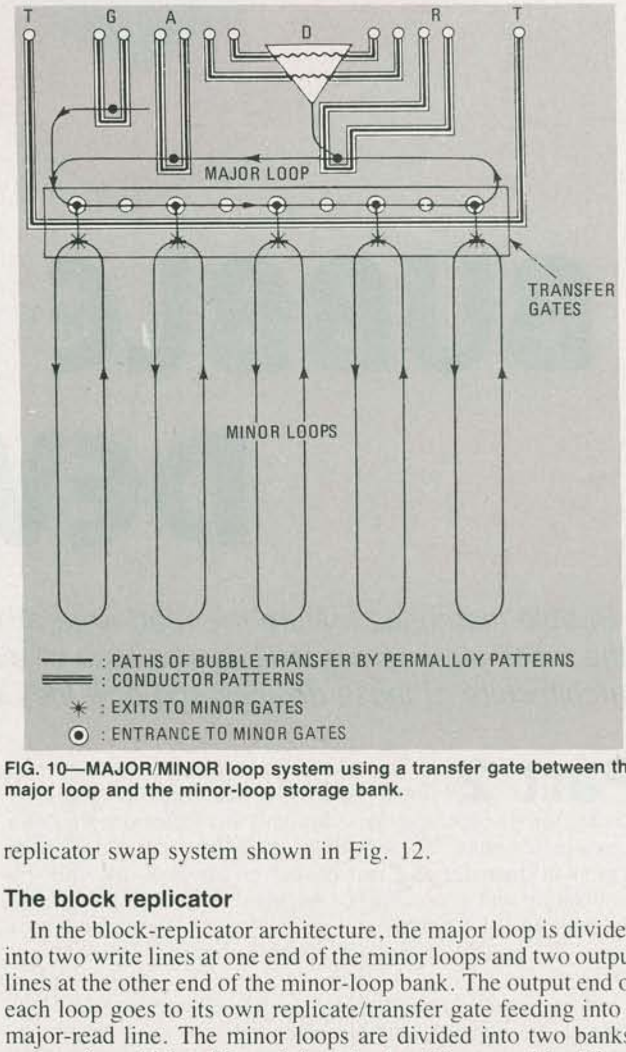

FIG. 10—MAJOR/MINOR loop system using a transfer gate between the major loop and the minor-loop storage bank.

The block replicator

In the block-replicator architecture, the major loop is divided into two write lines at one end of the minor loops and two output lines at the other end of the minor-loop bank. The output end of each loop goes to its own replicate/transfer gate feeding into a major-read line. The minor loops are divided into two banks; one storing odd data bits and the other handling even bits. There is a separate generator and input (write major line) for each loop bank. The generators are in series, so identical data is written on both major write lines.

Block replicator transfer system

When new information reaches the entrance to the transfer gates (see Fig. 11) for the proper minor loops, a current pulse is fed through the transfer-gate terminals and the data is loaded into the minor-loop banks for storage. Odd-number bits are loaded into one bank and even bits into the other. The odd bank has an extra bubble position, so identical data bits are offset one bubble position from those in the even bank. Therefore, every other bubble enters a loop—odd bits in one bank and even bits in the other.

Before new information can be entered for storage, old information at the desired address in the minor loops is circulated to the loop exits and transferrred simultaneously onto the major read lines when the transfer gate is pulsed. The bubbles are then conveyed to the detectors where they are read and then destroyed. Auxiliary control circuitry times the rotation of the loops and the transfer and replicate gates so the new information properly replaces the old.

To read out information, the control circuitry rotates the minor loops so the bits making up a specific data block are at the replicate gates. When the BR/T terminals in Fig. 11 are pulsed, the replicated copies are fed along the major read lines to the detectors. The original data bits are kept in storage in the minor loop bank.

The division of the minor loops into odd and even data banks makes the block replicate system twice as fast as the a transfer-gate loop system.

Block replicator swap system

Compare Figs. 11 and 12 and you'll see the close resemblence between the block replicator and swap replicator systems. The differences can be seen along the bottoms of the diagram. In Fig. 12, each minor loop is connected to the write entrance through a swap exit. A bank of swap gates replace the transfer gates in Fig. 11.

In the swap system, old information is transferred to the swap/write exits at the same time that new information is aligned along swap/write entrances to the minor loops. Thus, old data bits and corresponding new data bits face each other across the swap gates. At the proper time, the swap gate is energized and the old and new information swap places.

New data is entered on the minor loops while the old data is swept along the write major lines to be erased by an annihilator.

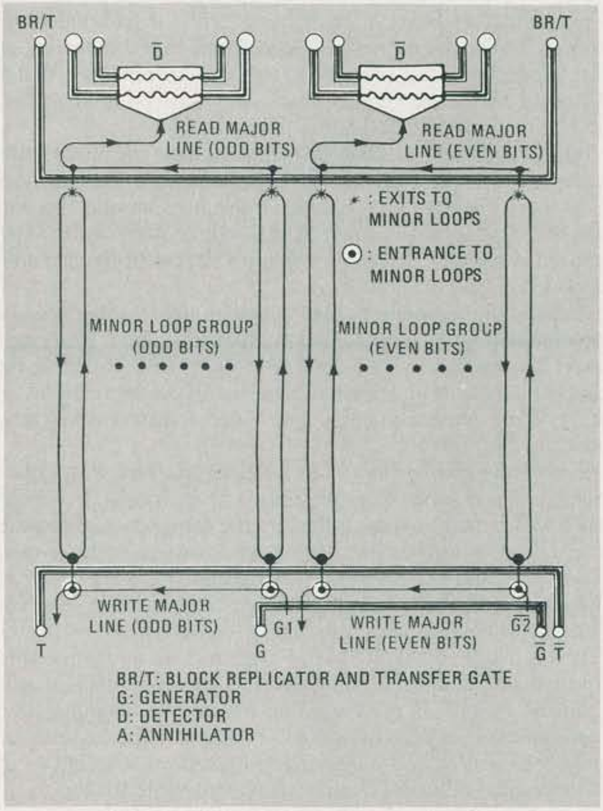
BR/T
BR/T
D̄
D̄
READ MAJOR LINE (ODD BITS)
READ MAJOR LINE (EVEN BITS)
*: EXITS TO MINOR LOOPS
⊙: ENTRANCE TO MINOR LOOPS
MINOR LOOP GROUP (ODD BITS)
MINOR LOOP GROUP (EVEN BITS)
WRITE MAJOR LINE (ODD BITS)
WRITE MAJOR LINE (EVEN BITS)
G1
G2̄
T
G
Ḡ T̄
BR/T: BLOCK REPLICATOR AND TRANSFER GATE
G: GENERATOR
D: DETECTOR
A: ANNIHILATOR

FIG. 11— **BLOCK REPLICATOR transfer system is twice as fast as the transfer-gate organization.**

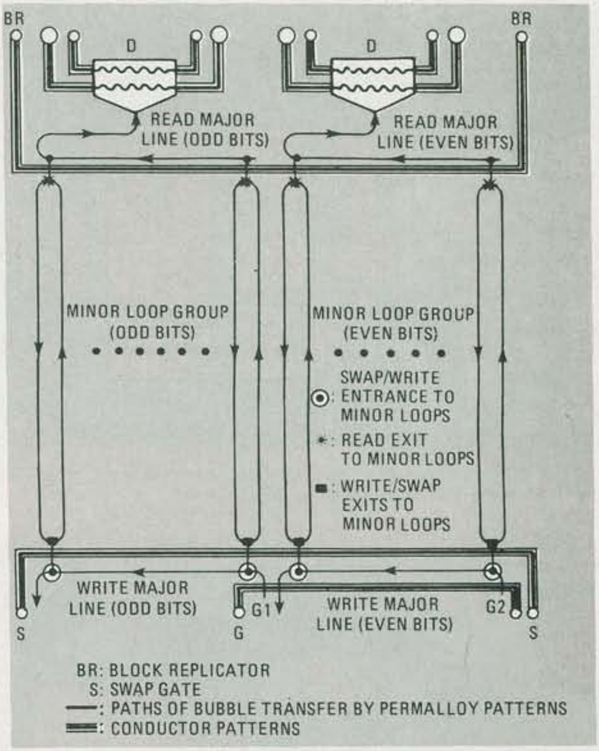
BR
BR
D
D
READ MAJOR LINE (ODD BITS)
READ MAJOR LINE (EVEN BITS)
MINOR LOOP GROUP (ODD BITS)
MINOR LOOP GROUP (EVEN BITS)
SWAP/WRITE
⊙: ENTRANCE TO MINOR LOOPS
*: READ EXIT TO MINOR LOOPS
■: WRITE/SWAP EXITS TO MINOR LOOPS
WRITE MAJOR LINE (ODD BITS)
WRITE MAJOR LINE (EVEN BITS)
G1
G2
S
G
S
BR: BLOCK REPLICATOR
S: SWAP GATE
—: PATHS OF BUBBLE TRANSFER BY PERMALLOY PATTERNS
═: CONDUCTOR PATTERNS

FIG. 12—BLOCK REPLICATOR swap system eliminates the need for old data to be erased before new data can be entered.

Unlike the block replicator transfer system, the swap arrangement eliminates the need to erase old information before writing new.

Peripheral circuits

A number of auxiliary circuit devices are needed to operate a bubble memory storage device. Some of these are called direct peripheral circuits because they connect directly to the bubble memory device. Figure 13 is a block diagram of a magnetic bubble memory system using Motorola's MBM2256 device. The direct peripheral devices are coil drivers, a function driver, and a sense amplifier. The coil drivers feed the X and Y coils with a triangle waveform. The triangle waveform that drives the X coil is 90° out-of-phase with the triangle waveform that drives the Y coil so as to produce a rotating magnetic field. The function driver supplies pulse currents to the function gates. The sense amplifier boosts the detected bubble information signals to a TTL level.

Indirect peripheral devices or circuits are those that control the direct peripheral circuits and provide the necessary interface between the bubble memory system and a microprocessor. The X and Y electromagnetic coils require comparatively high drive currents. The coil predriver is an interface device between the controller and the power transistors used in the coil drivers. The controller provides the timing and control for the coil-driver and function-driver circuits along with timing signals needed.

The MBM2256 is a low-cost, non-volatile solid-state memory device in a 16-pin DIP package approximately 1.1 × 1.15 inches. It is complete with the in-plane magnet coils to develop the rotating magnetic field and a permanent magnet structure to supply a fixed magnetic bias. A magnetic shield protects the device and data from the effects of external magnetic fields.

The memory module has a nominal capacity of 250K bits arranged as 256 storage loops; each with 1024 storage locations. One additional storage (map) loop stores the locations of defective loops and address reference locations. The architecture uses the block replicator swap system. This device can be started and stopped at will and does not lose data when power is either lost or disconnected. The general specifications of the device are listed in Table 1.

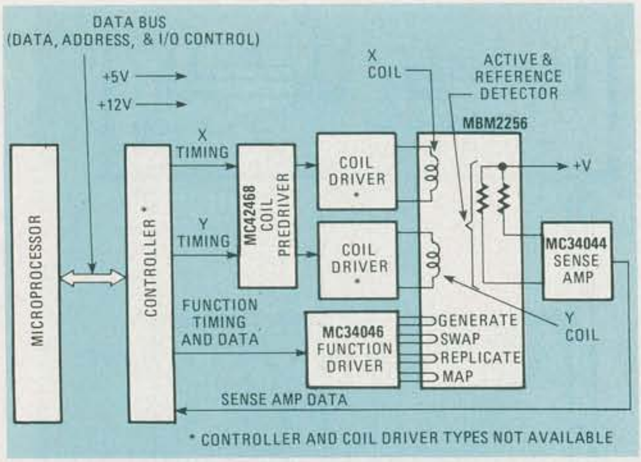

FIG. 13— BLOCK DIAGRAM of Motorola's bubble-memory system. The MBM device uses the block replicator swap system.

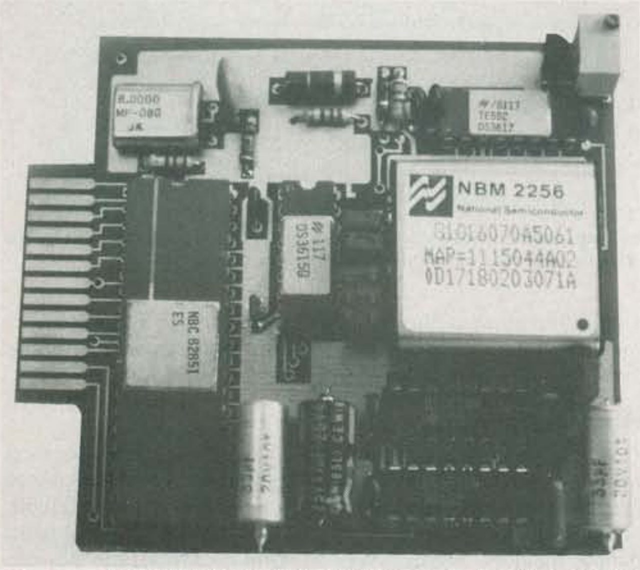

FIG. 14— AN MBM DEVELOPMENT BOARD can be less than 3-inches square and needs just 13 connections for complete interfacing.

The MBM2256, how it works

The device's storage loops have an input track with a swap gate on one side and an output track with a replicate gate on the other. The input track is driven by a generator and the output track leads into an area where the bubbles are stretched so they provide a reliable output signal that can be handled by ordinary electronic circuitry.

To enter data into the MBM2256 magnetic bubble memory, the generators must be fed sequential current pulses according to the data being entered. The swap gate is pulsed as soon as the data block is circulated around the input track and is aligned with the transfer-in gates of the storage loops. The swap gates exchange the new data block with the old in one step.

A read action occurs when the desired data block has been transferred to the transfer-out/replicate gate and the replicate gate is pulsed. The replicated copy of the original data is read by the detectors while the original data is returned to storage.

How bubble memories are implemented

Although a magnetic bubble memory (MBM) device has the performance characteristics of ROM's, RAM's, PROM's and floppy disks, it is not a replacement for any of these devices. Its primary purpose is as a support for the memory devices. (For a comparison of the performance characteristics of the MBM with other magnetic and solid-state memories, see Table 1 in Part 1 of this article in the October 1982 issue.)

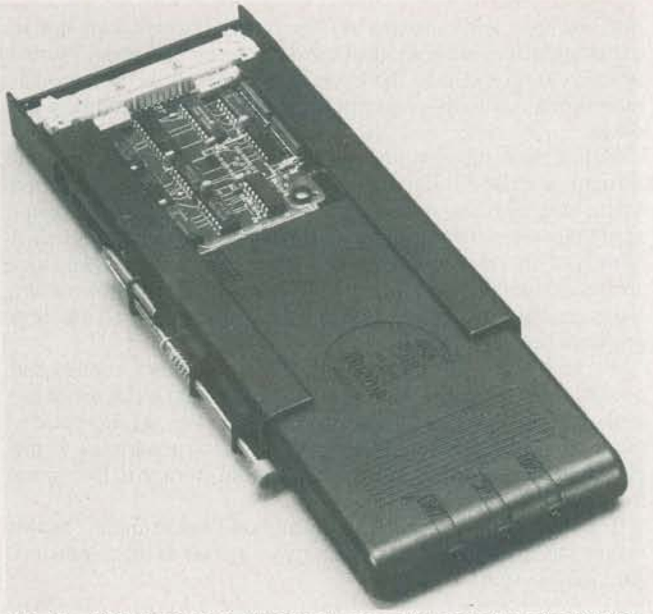

FIG. 15—INTEL'S PLUG-A-BUBBLE basic system consists of a 128 kilobyte system in a cassette that requires no more space than 5¼-inch floppy.

The MBM's ability to store vast amounts of data in a very small space gives it a tremendous advantage in reducing equipment size. It requires less space than either tape or floppy disk; even when several MBM's are paralleled into a 1- or 2-megabyte system. As a rule, the bubble memory manufacturer has a line of support devices designed to go with his system. The user can use a compact development board or plug the components into his PC board with comparatively little effort.

A development board using the MBM system outlined in the block diagram in Fig. 13 can be less than 3 inches square and needs only 13 connector pads for data, address and I/O control signals to and from the microprocessor. Such a board is shown in Fig. 14. (Note that the board in the photo is from National Semiconductor. That company has recently discontinued their work on bubble memories and have dropped those device, and their support devices, from its line. Also note, however, that the Motorola device we've been discussing thus far is identical to the National NBM2256 shown here.)

Intel Magnetics has a bubble memory prototype board featuring up to 512 kilobytes of non-volatile storage that measures 6.75 × 12-inches. The system is designed around the company's 7110 1,048,576-bit (128,000 byte) device. Four 7110's are used in parallel: driven by a single 7220 controller and allied support devices.

Perhaps the most exemplary innovation in bubble memory implementation is Intel's *Plug-A-Bubble* system featuring a removable bubble cassette designed to provide a compact, permanent memory storage system for critical data applications and use in harsh environments. The *Plug-A-Bubble* cassette is shown in Fig. 15.

The system consists of a 7110 128K-byte device with support circuitry in a cassette that measures 0.81 inch high, 6.1 inches long and 3.6 inches wide. It fits into the same space as required by a 5.25-inch floppy disk. The cassette features 48 ms average access time and 12.5 kilobytes-per-second data transfer rate. Ambient operating temperature range is 0° C to 55° C. Non-operating storage temperature range is −40° C to +100° C.

Packaging the complete MBM system in a cassette has three important advantages: First of all, it insures high data integrity because transients in the controller-to-bubble communications are minimized; secondly, the logic is built into the cassette so it can be removed while the system is powered-up, and finally, the self-contained plug-in system makes it possible for the microprocessor to accommodate future developments featuring greater data density. R-E