# Applications for a New Ultra-High Speed Buffer

National Semiconductor
Application Note 48

## INTRODUCTION

Voltage followers have gained in popularity in applications such as sample and hold circuits, general purpose buffers, and active filters since the introduction of IC operational amplifiers. Since they were not specifically designed as followers, these early IC's had limited usage due to low bandwidth, low slew rate and high input current. Usage of voltage followers was expanded in 1967 with the introduction of the LM102, the first IC designed specifically as a voltage follower. With the LM102, engineers were able to obtain an order of magnitude improvement in performance and extend usage into medium speed applications. The LM110, an improved LM102, was introduced in late 1969. However, even higher speeds and lower input currents were needed for very fast sample and holds, A to D and D to A converters, coax cable drivers, and other video applications.

The solution to this application problem was attained by combining technologies into a single package. The result, the LH0033 high speed buffer, utilizes JFET and bipolar technology to produce a ultra-fast voltage follower and buffer whose propagation delay closely approaches speed-of-light delay across its package, while not compromising input impedance or drive characteristics. Table I compares various voltage followers and illustrates the superiority of the LH0033 in both low input current or high speed video applications.

## CIRCUIT CONSIDERATIONS

The junction FET makes a nearly ideal input device for a voltage follower, reducing input bias current to the picoamp range. However, FET's exhibit moderate voltage offsets and offset drifts which tend to be difficult to compensate. The simple voltage follower of *Figure 1* eliminates initial offset and offset drift if $Q_1$ and $Q_2$ are identically matched transistors. Since the gate to source voltage of $Q_2$ equals zero volts, then $Q_1$'s gate to source voltage equals zero volts. Furthermore as $V_{P1}$ changes with temperature (approximately 2.2 mV/°C), $V_{P2}$ will change by a corresponding amount. However, as load current is drawn from the output, $Q_1$ and $Q_2$ will drift at different rates, A circuit which overcomes offset voltage drift is used in a new high speed buffer amplifier, the LH0033. Initial offset is typically 5 mV and offset drift is 20 μV/°C. Resistor $R_2$ is used to establish the drain current of current source transistor, $Q_2$ at 10 mA.

The same drain current flows through $Q_1$ causing a voltage at the source of approximately 1.1V. The 10 mA flowing through $R_1$ plus $Q_3$'s $V_{BE}$ of 0.6V causes the output to sit at zero volts for zero volts in. $Q_3$ and $Q_4$ eliminate loading the input stage (except for base current) and $CR_1$ and $CR_2$ establish the output stage collector current.

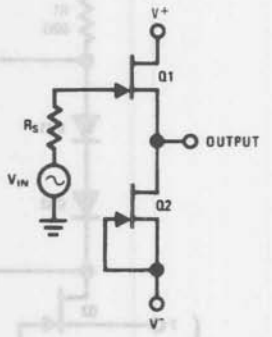


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**FIGURE 1. Simple Voltage Follower Schematic**

If $Q_1$ and $Q_2$ are matched, the resulting drift is reduced to a few μV/°C.

## PERFORMANCE OF THE LH0033 FAST VOLTAGE FOLLOWER/BUFFER

The major electrical characteristics of the LH0033 are summarized in Table II. All the virtues of a ultra-high speed buffer have been incorporated.

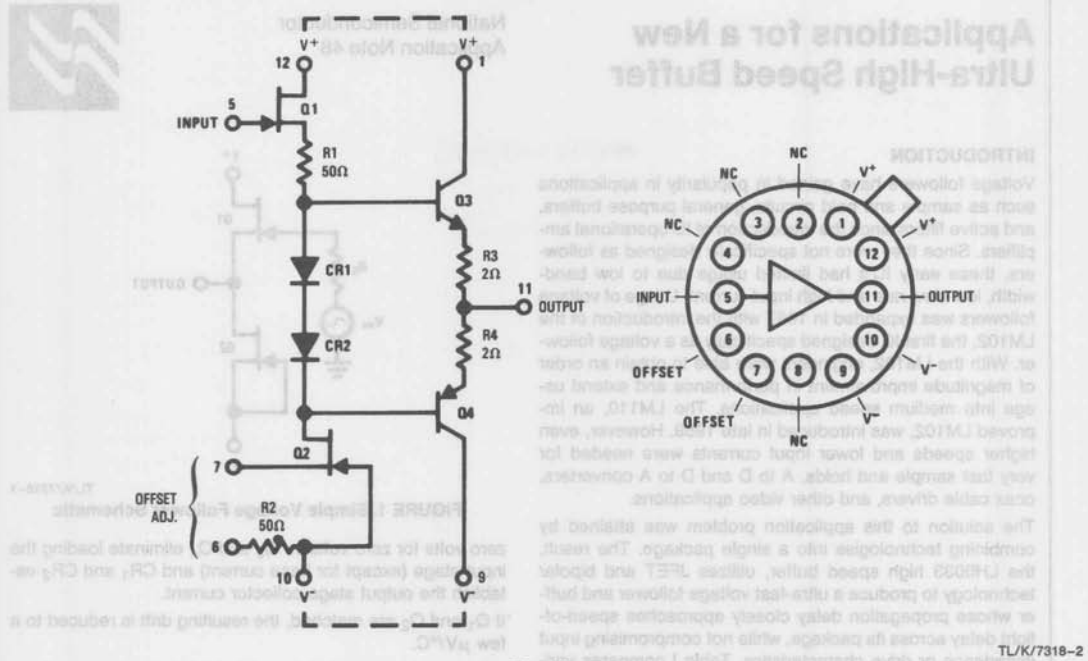
*Figure 3* is a plot of input bias current vs temperature and shows the typical FET input characteristics. Other typical performance curves are illustrated in *Figures 4* through *10*. Of particular interest is *Figure 8*, which demonstrates the performance of the LH0033 in video applications to over 100 MHz.

## APPLICATIONS FOR ULTRA-FAST FOLLOWERS

The LH0033's high input impedance ($10^{11}$ Ω, shunted by 2 pF) and high slew rate assure minimal loading and high fidelity in following high speed pulses and signals. As shown below, the LH0033 is used as a buffer between MOS logic and a high speed dual limit comparator. The device's high input impedance prevents loading of the MOS logic signal (even a conventional scope probe will distort high output impedance MOS). The LH0033 adds about a 1.5 ns to the total delay of the comparator. Adjustment of voltage divider $R_1$, $R_2$ allows interface to TTL, DTL and other high speed logic forms.

**TABLE I. COMPARISON OF VOLTAGE FOLLOWERS**

| Parameter | Conventional Monolithic Op Amp LM741 | First Generation Voltage Follower LM102 | Second Generation Voltage Follower LM110 | Specially Designed Voltage Follower LH0033 |
|---|---|---|---|---|
| Input Bias Current | 200 nA | 3.0 nA | 1.0 nA | 0.05 nA |
| Slew Rate | 0.5 V/μs | 10V/μs | 30V/μs | 1500V/μs |
| Bandwidth | 1.0 MHz | 10 MHz | 20 MHz | 100 MHz |
| Prop. Delay Time | 350 ns | 35 ns | 18 ns | 1.2 ns |
| Output Current Capability | ±5 mA | ±2 mA | ±2 mA | ±100 mA |




Top View

**FIGURE 2. LH0033 Schematic**

**TABLE II**

| Parameter | Conditions | Value | Parameter | Conditions | Value |
|---|---|---|---|---|---|
| Output Offset Voltage | $R_S$ = 100 kΩ | 5 mV | Output Current Capability | | ±100 mA peak |
| Input Bias Current | | 50 pA | Slew Rate | $R_S$ = 50Ω, $R_L$ = 1k | 1500V/μs |
| Input Impedance | $V_{IN}$ = 1.0 Vrms<br>$R_L$ = 1k, f = 1 kHz | $10^{11}$ Ω | Propagation Delay | | 1.2 ns |
| Voltage Gain | $V_{IN}$ = 1.0 Vrms<br>$R_L$ = 1k, f = 1 kHz, $R_S$ = 100k | 0.98 | Bandwidth | $V_{IN}$ = 1.0 Vrms<br>$R_S$ = 50Ω, $R_L$ = 1k | 100 MHz |
| Output Voltage Swing | $V_S$ = ±15V, $R_S$ = 100k<br>$R_L$ = 1k | ±13V | | | |

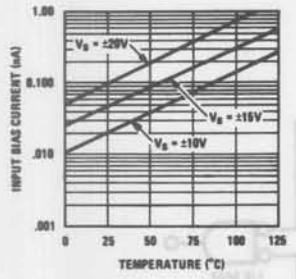



FIGURE 3. Input Bias Current vs Temperature

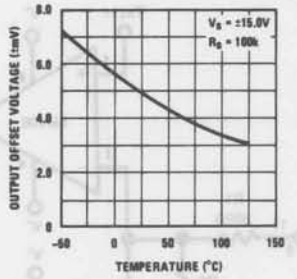



FIGURE 4. Output Offset Voltage vs Temperature

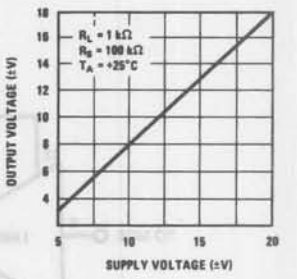



FIGURE 5. Output Voltage vs Supply Voltage

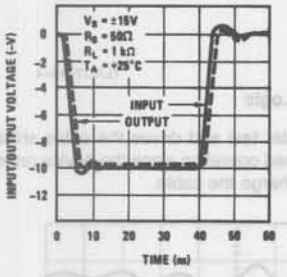



FIGURE 6. Negative Pulse Response

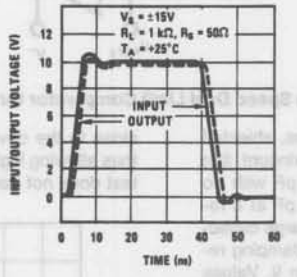



FIGURE 7. Positive Pulse Response

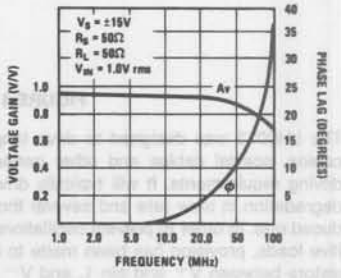



FIGURE 8. Frequency Response

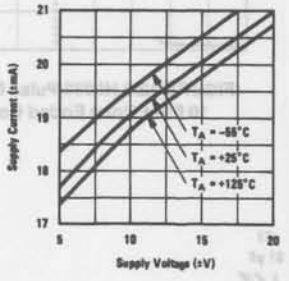



FIGURE 9. Supply Current vs Supply Voltage

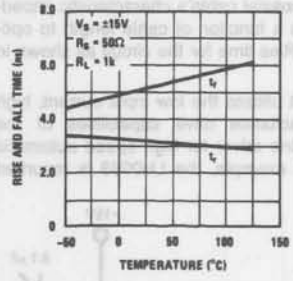



FIGURE 10. Rise and Fall Time vs Temperature

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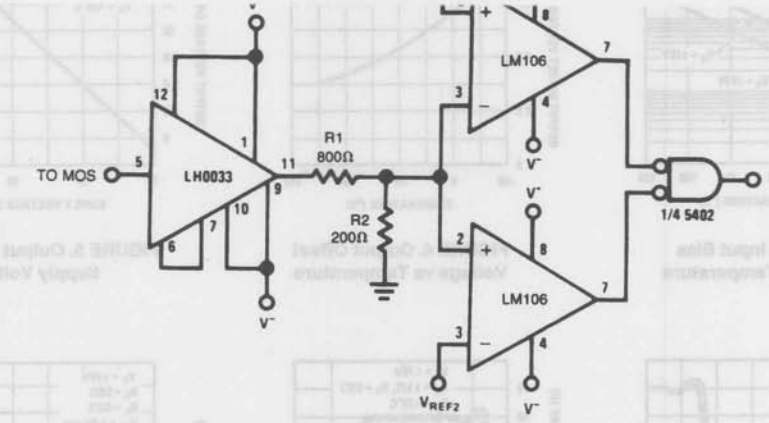


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**FIGURE 11. High Speed Dual Limit Comparator for MOS Logic**

The LH0033 was designed to drive long cables, shielded cables, coaxial cables and other generally stringent line driving requirements. It will typically drive 200 pF with no degradation in slew rate and several thousand pF at a reduced rate. In order to prevent oscillations with large capacitive loads, provision has been made to insert damping resistors between $V^+$ and pin 1, and $V^-$ and pin 9. Values between 47 and 100Ω work well for $C_L > 1000$ pF. For non-reactive loads, pin 12 should be shorted to pin 1 and pin 10 shorted to pin 9. A coaxial driver is shown in *Figure 13*. Pin 6 is shorted to pin 7, obtaining an initial offset of 5.0 mV, and the 43Ω coupled with the LH0033's output impedance (about 6Ω) match the coaxial cable's characteristic impedance. $C_1$ is adjusted as a function of cable length to optimize rise and fall time. Rise time for the circuit as shown in *Figure 12*, is 10 ns.

Another application that utilizes the low input current, high speed and high capacitance drive capabilities of the LH0033 is a shield or line driver for high speed automatic test equipment. In this example, the LH0033 is mounted close to the device under test and drives the cable shield thus allowing higher speed operation since the device under test does not have to charge the cable.

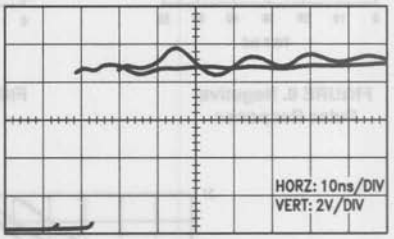


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**FIGURE 12. LH0033 Pulse Response into 10 Foot Open Ended Coaxial Cable**

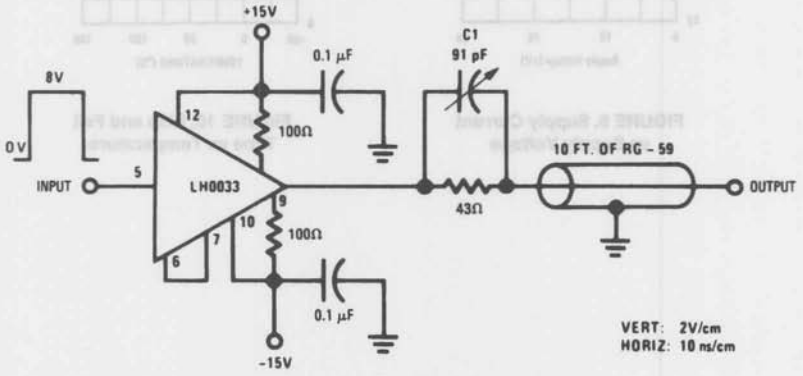


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**FIGURE 13**

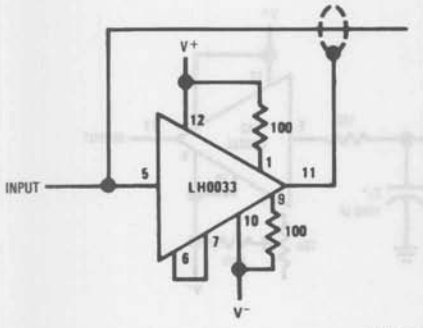


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**FIGURE 14. Instrumentation Shield/Line Driver**

The LH0033's high input impedance and low input bias current may be utilized in medium speed circuits such as Sample and Hold, and D to A converters. *Figure 15* shows an LH0033 used as a buffer in medium speed D to A converter.

Offset null is accomplished by connecting a 100Ω pot between pin 7 and $V^-$. It is generally a good idea to insert 20Ω in series with the pot to prevent excessive power dissipation in the LH0033 when the pot is shorted out. In non-critical or AC coupled applications, pin 6 should be shorted to pin 7. The resulting output offset is typically 5 mV at 25°C.

The high output current capability and slew rate of the LH0033 are utilized in the sample and hold circuit of *Figure 16*. Amplifier, A1 is used to buffer high speed analog signals. With the configuration shown, acquisition time is limited by the time constant of the switch "ON" resistance and sampling capacitor, and is typically 200 or 300 ns.

$A_2$'s low input bias current, results in drifts in hold mode of

$$\frac{50\text{ mV}}{\text{sec}} \text{ at } 25°C \quad \text{and} \quad \frac{1\text{V}}{\text{sec}} \text{ at } 125°C.$$

The LH0033 may be utilized in AC applications such as video amplifiers and active filters. The circuit of *Figure 17* utilizes boot strapping to achieve input impedances in excess of 10 MΩ.

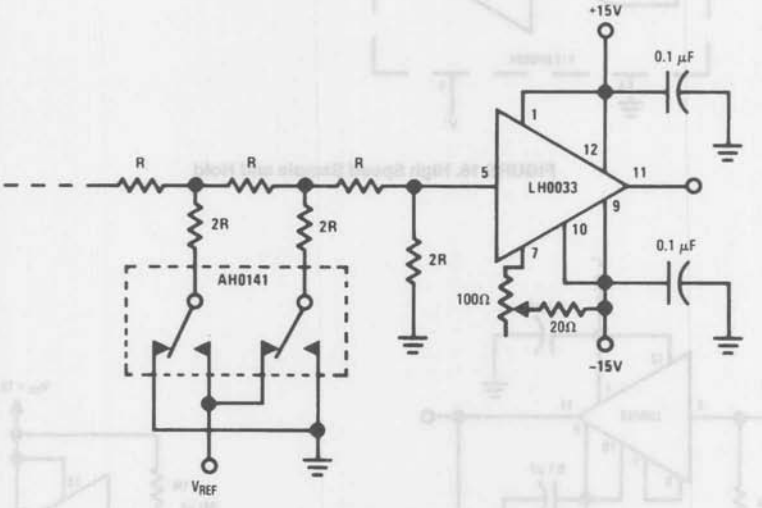


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**FIGURE 15**

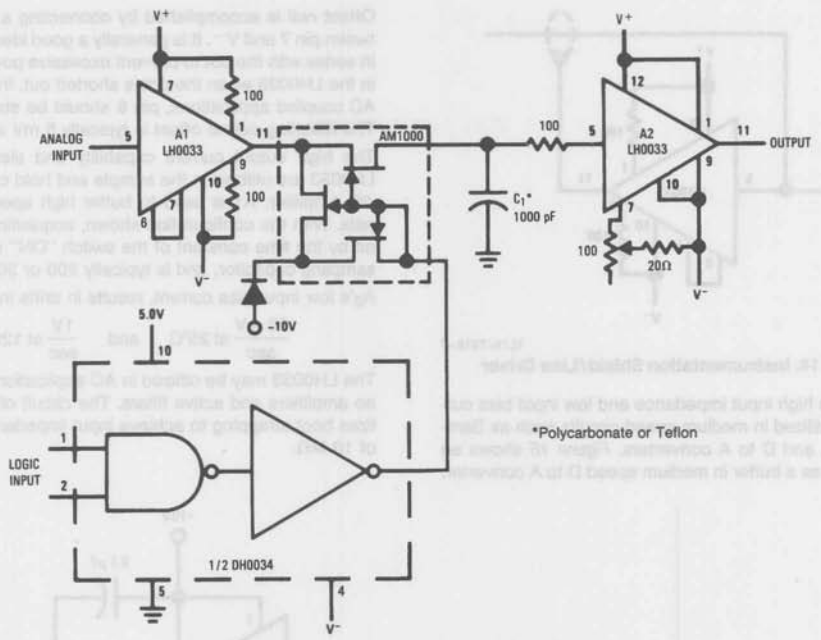


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**FIGURE 16. High Speed Sample and Hold**

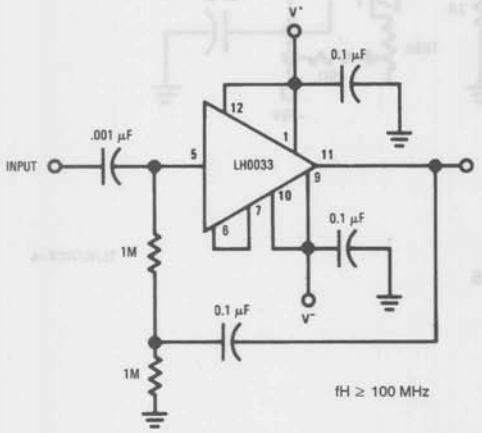


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**FIGURE 17. High Input Impedance AC Coupled Amplifier**

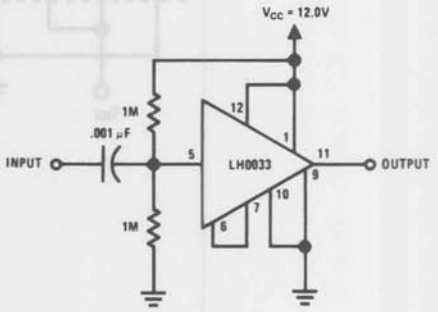


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**FIGURE 18. Single Supply AC Amplifier**

A single supply, AC coupled amplifier is shown in *Figure 18.* Input impedance is approximately 500k and output swing is in excess of 8V peak-to-peak with a 12V supply.

The LH0033 may be readily used in applications where symmetrical supplies are unavailable or may not be desirable. A typical application might be an interface to an MOS shift register where $V^+ = 5.0V$ and $V^- = -25V$. In this case, an apparent output offset occurs. In reality, the output voltage is due to the LH0033's voltage gain of less than unity.

The output voltage shift due to asymmetrical supplies may be predicted by:

$$\Delta V_O \cong (1 - Av)\frac{(V^+ - V^-)}{2} = .005\,(V^+ - V^-)$$

where: Av = No load voltage gain, typically 0.99.

$V^+$ = Positive Supply Voltage.

$V^-$ = Negative Supply Voltage.

For the foregoing application, $\Delta V_O$ would be −100 mV. This apparent "offset" may be adjusted to zero as outlined above.

*Figure 19* shows a high Q, notch filter which takes advantage of the LH0033's wide bandwidth. For the values shown, the center frequency is 4.5 MHz.

The LH0033 can also be used in conjunction with an operational amplifier as current booster as shown in *Figure 20*. Output currents in excess of 100 mA may be obtained. Inclusion of 150Ω resistors between pins 1 and 12, and 9 and 10 provide short circuit protection, while decoupling pins 1 and 9 with 1000 pF capacitors allow near full output swing.

The value for the short circuit current is given by:

$$I_{SC} \cong \frac{V^+}{R_{LIMIT}} = \frac{V^-}{R_{LIMIT}}$$

where: $I_{SC} \leq 100$ mA.

## SUMMARY

The advantages of a FET input buffer have been demonstrated. The LH0033 combined very high input impedance, wide bandwidth, very high slew rate, high output capability, and design flexibility, making it an ideal buffer for applications ranging from DC to in excess of 100 MHz.

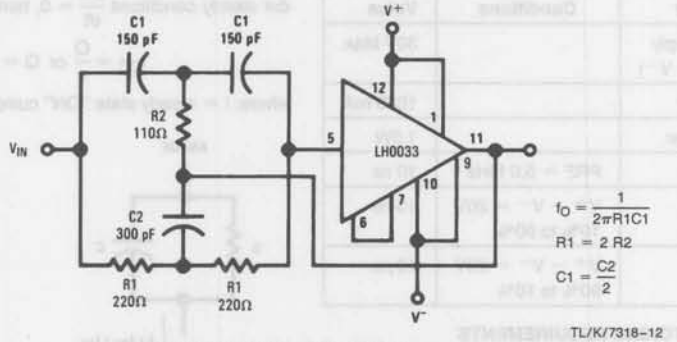


**FIGURE 19. 4.5 MHz Notch Filter**

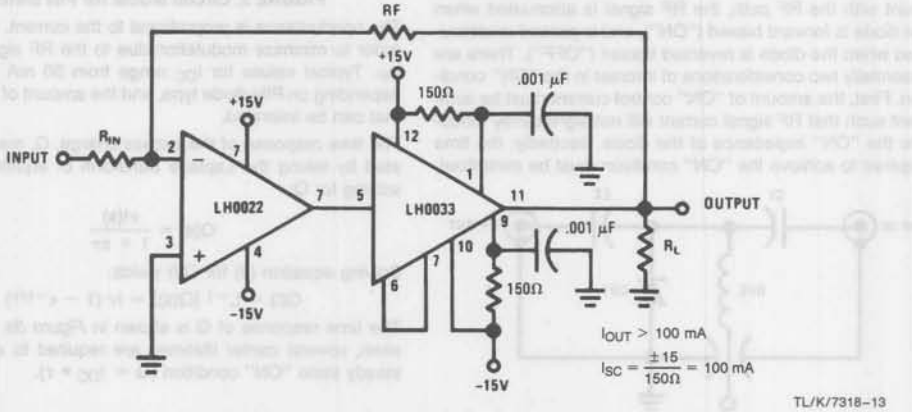


**FIGURE 20. Using LH0033 as an Output Buffer**

# PIN Diode Drivers

National Semiconductor
Application Note 49

## INTRODUCTION

The DH0035/DH0035C is a TTL/DTL compatible, DC coupled, high speed PIN diode driver. It is capable of delivering peak currents in excess of one ampere at speeds up to 10 MHz. This article demonstrates how the DH0035 may be applied to driving PIN diodes and comparable loads which require high peak currents at high repetition rates. The salient characteristics of the device are summarized in Table I.

**TABLE I. DH0035 Characteristics**

| Parameter | Conditions | Value |
|---|---|---|
| Differential Supply Voltage ($V^+ - V^-$) | | 30V Max. |
| Output Current | | 1000 mA |
| Maximum Power | | 1.5W |
| $t_{delay}$ | PRF = 5.0 MHz | 10 ns |
| $t_{rise}$ | $V^+ - V^- = 20V$ 10% to 90% | 15 ns |
| $t_{fall}$ | $V^+ - V^- = 20V$ 90% to 10% | 10 ns |

## PIN DIODE SWITCHING REQUIREMENTS

*Figure 1* shows a simplified schematic of a PIN diode switch. Typically, the PIN diode is used in RF through microwave frequency modulators and switches. Since the diode is in shunt with the RF path, the RF signal is attenuated when the diode is forward biased ("ON"), and is passed unattenuated when the diode is reversed biased ("OFF"). There are essentially two considerations of interest in the "ON" condition. First, the amount of "ON" control current must be sufficient such that RF signal current will not significantly modulate the "ON" impedance of the diode. Secondly, the time required to achieve the "ON" condition must be minimized.

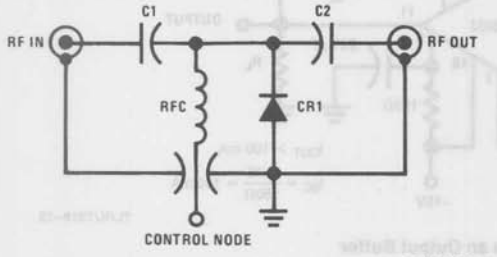


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**FIGURE 1. Simplified PIN Diode Switch**

The charge control model of a diode[1,2] leads to the charge continuity equation given in equation (1).

$$i = \frac{dQ}{dt} + \frac{Q}{\tau} \quad (1)$$

where: Q = charge due excess minority carriers

$\tau$ = mean lifetime of the minority carriers

Equation (1) implies a circuit model shown in *Figure 2*. Under steady conditions $\frac{dQ}{dt} = 0$, hence:

$$I_{DC} = \frac{Q}{\tau} \text{ or } Q = I_{DC} \bullet \tau \quad (2)$$

where: I = steady state "ON" current.

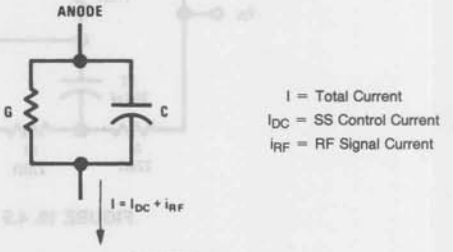


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**FIGURE 2. Circuit Model for PIN Switch**

The conductance is proportional to the current, I; hence, in order to minimize modulation due to the RF signal, $I_{DC} \gg i_{RF}$. Typical values for $I_{DC}$ range from 50 mA to 200 mA depending on PIN diode type, and the amount of modulation that can be tolerated.

The time response of the excess charge, Q, may be evaluated by taking the Laplace transform of equation (1) and solving for Q:

$$Q(s) = \frac{\tau I(s)}{1 + s\tau} \quad (3)$$

Solving equation (3) for Q(t) yields:

$$Q(t) = L^{-1}[Q(s)] = I\tau\,(1 - \epsilon^{-t/\tau}) \quad (4)$$

The time response of Q is shown in *Figure 3a*. As can be seen, several carrier lifetimes are required to achieve the steady state "ON" condition ($Q = I_{DC} \bullet \tau$).

The time response of the charge, hence the time for the diode to achieve the "ON" state could be shortened by applying a current spike, Ipk, to the diode and then dropping the current to the steady state value, $I_{DC}$, as shown in *Figure 3b*. The optimum response would be dictated by:

$$(Ipk)\,(t) = \tau \bullet I_{DC} \qquad (5)$$

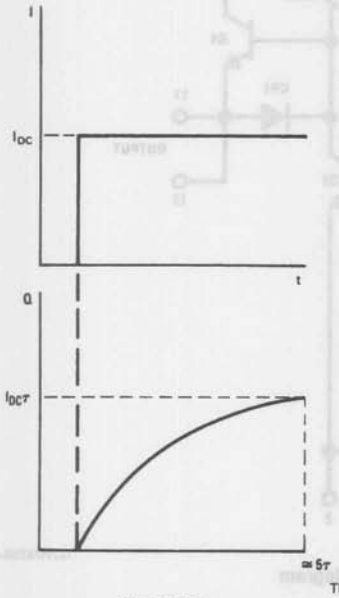


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**FIGURE 3a**

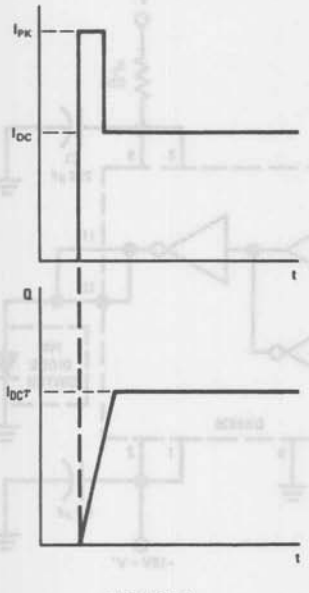


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**FIGURE 3b**

The turn off requirements for the PIN diode are quite similar to the turn on, except that in the "OFF" condition, the steady current drops to the diode's reverse leakage current.

A charge, $I_{DC} \bullet \tau$, was stored in the diode in the "ON" condition and in order to achieve the "OFF" state this charge must be removed. Again, in order to remove the charge rapidly, a large peak current (in the opposite direction) must be applied to the PIN diode:

$$-Ipk \geqslant \frac{Q}{\tau} \qquad (6)$$

It is interesting to note an implication of equation (5). If the peak turn on current were maintained for a period of time, say equal to $\tau$, then the diode would acquire an excess charge equal to Ipk • T. This same charge must be removed at turn off, instead of a charge $I_{DC} \bullet \tau$, resulting in a considerably slower turn off. Accordingly, control of the width of turn on current peak is critical in achieving rapid turn off.

## APPLICATION OF THE DH0035 AS A PIN DIODE DRIVER

The DH0035 is specifically designed to provide both the current levels and timing intervals required to optimally drive PIN diode switches. Its schematic is shown in *Figure 4*. The device utilizes a complementary TTL input buffer such as the DM7830/DM8830 or DM5440/DM7440 for its input signals.

Two configurations of PIN diode switch are possible: cathode grounded and anode grounded. The design procedures for the two configurations will be considered separately.

### ANODE GROUND DESIGN

Selection of power supply voltages is the first consideration. Table I reveals that the DH0035 can withstand a total of 30V differentially. The supply voltage may be divided symmetrically at ±15V, for example. Or asymmetrically at +20V and −10V. The PIN diode driver shown in *Figure 5*, uses ±10V supplies.

When the Q output of the DM8830 goes high a transient current of approximately 50 mA is applied to the emitter of $Q_1$ and in turn to the base of $Q_5$.

$Q_5$ has an $h_{fe} = 20$, and the collector current is $h_{fe} \times 50$ or 1000 mA. This peak current, for the most part, is delivered to the PIN diode turning it "ON" (RF is "OFF").

Ipk flows until $C_2$ is nearly charged. This time is given by:

$$t = \frac{C2\Delta V}{Ipk} \qquad (7)$$

where: $\Delta V$ = the change in voltage across $C_2$.

Prior to $Q_5$'s turn on, $C_2$ was charged to the minus supply voltage of −10V. $C_2$'s voltage will rise to within two diode drops plus a $V_{sat}$ of ground:

$$V = |V^-| - Vf(\text{PIN Diode}) - Vf_{CR1} - V_{sat_{Q5}} \qquad (8)$$

for $V^- = -10V$, $\Delta V = 8V$.

Once $C_2$ is charged, the current will drop to the steady state value, $I_{DC}$, which is given by:

$$I_{DC} = \frac{V}{R_M} - \frac{V^+}{R_3} - \frac{V_{CC}}{R_1} \qquad (9)$$

where: $V_{CC} = 5.0V$

$R_1 = 250\Omega$

$R_3 = 500\Omega$

$$\therefore R_M = \frac{(R_3\,(\Delta V)\,(R_1)}{R_1V^+ + I_{DC}R_3R_1 + V_{CC}R_3} \qquad (9a)$$

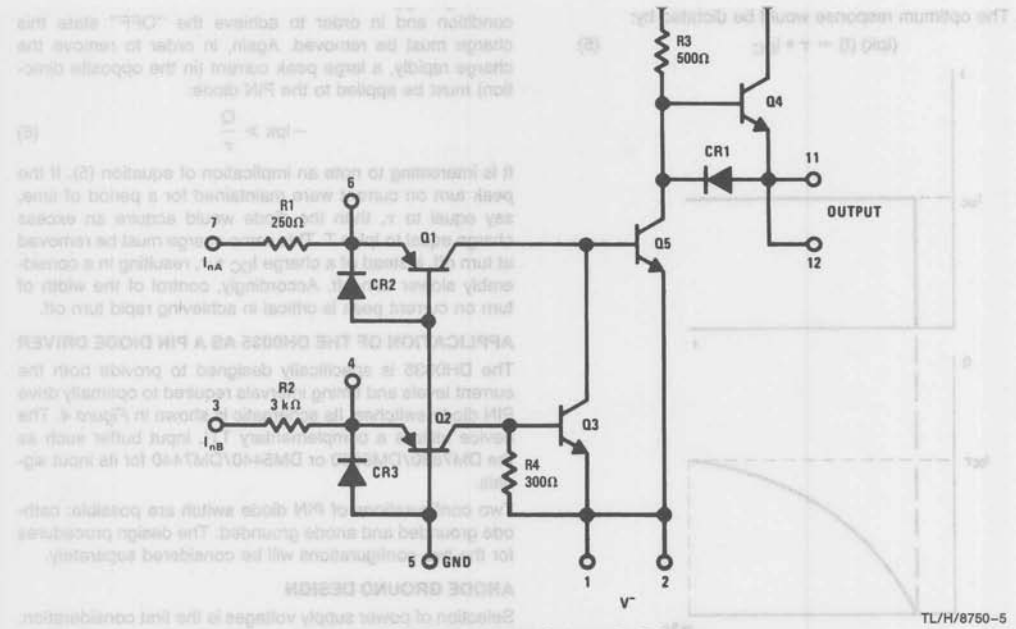


**FIGURE 4. DH0035 Schematic Diagram**

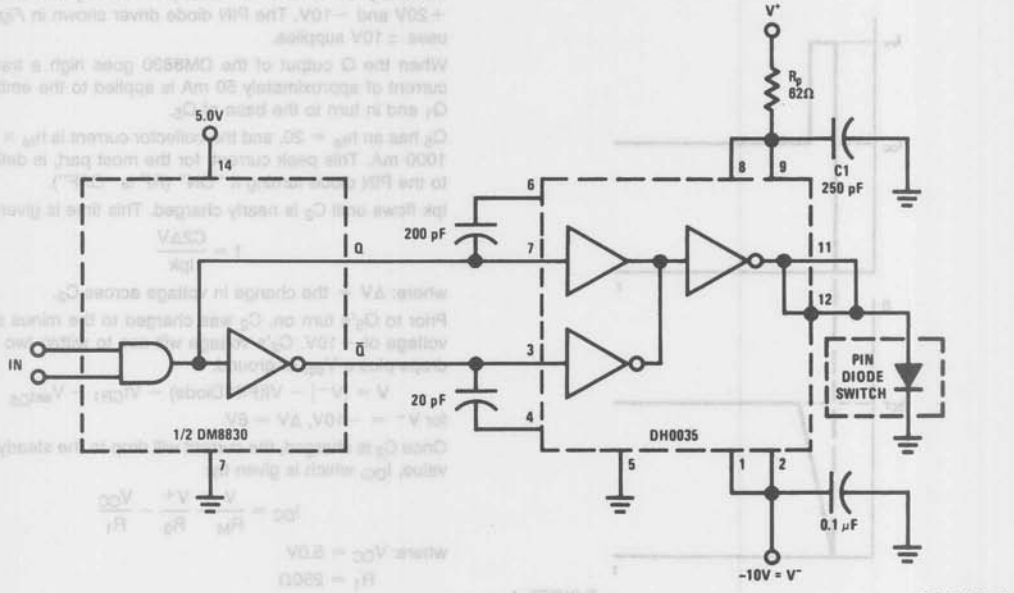


**FIGURE 5. Cathode Grounded Design**

For the driver of *Figure 5*, and $I_{DC}$ = 100 mA, $R_M$ is 56Ω (nearest standard value).

Returning to equation (7) and combining it with equation (5) we obtain:

$$t = \frac{\tau I_{DC}}{Ipk} = \frac{C_2 V}{Ipk} \quad (10)$$

Solving equation (10) for $C_2$ gives:

$$C_2 = \frac{I_{DC}\tau}{V} \quad (11)$$

For $\tau$ = 10 ns, $C_2$ = 120 pF.

One last consideration should be made with the diode in the "ON" state. The power dissipated by the DH0035 is limited to 1.5W (see Table I). The DH0035 dissipates the maximum power with $Q_5$ "ON". With $Q_5$ "OFF", negligible power is dissipated by the device. Power dissipation is given by:

$$P\,diss \cong \left[I_{DC}(|V^-| - \Delta V) + \frac{(V^+ - V^-)^2}{R3}\right] \times (D.C.) \leq P_{max} \quad (12)$$

where: D.C. = Duty Cycle =

$$\frac{(\text{"ON" time})}{(\text{"ON" time} + \text{"OFF" time})}$$

Pmax = 1.5W

In terms of $I_{DC}$:

$$I_{DC} \leq \frac{\left[\frac{(Pmax)}{(D.C.)} - \frac{(V^+ - V^-)^2}{500}\right]}{|V^-| - \Delta V} \quad (12a)$$

For the circuit of *Figure 5* and a 50% duty cycle, P diss = 0.5W.

Turn-off of the PIN diode begins when the Q output of the DM8830 returns to logic "0" and the $\overline{Q}$ output goes to logic "1". $Q_2$ turns "ON", and in turn, causes $Q_3$ to saturate. Simultaneously, $Q_1$ is turned "OFF" stopping the base drive to $Q_5$. $Q_3$ absorbs the stored base charge of $Q_5$ facilitating its rapid turn-off. As $Q_5$'s collector begins to rise, $Q_4$ turns "ON". At this instant, the PIN diode is still in conduction and the emitter of $Q_4$ is held at approximately −0.7V. The instantaneous current available to clear stored charge out of the PIN diode is:

$$Ipk = \frac{V^+ - V_{BE\,Q4} + V_{f(PIN)}}{\frac{R3}{h_{fe} + 1}} \cong \frac{(h_{fe} + 1)(V^+)}{R_3} \quad (13)$$

where:

$h_{fe}$ + 1 = current gain of $Q_4$ = 20

$V_{BE\,Q4}$ = base-emitter drop of $Q_4$ = 0.7V

$V_{f(PIN)}$ = forward drop of the PIN diode = 0.7V

For typical values given, Ipk = 400 mA. Increasing $V^+$ above 10V will improve turn-off time of the diode, but at the expense of power dissipation in the DH0035. Once turn-off of the diode has been achieved, the DH0035 output current drops to the reverse leakage of the PIN diode. The attendant power dissipation is reduced to about 35 mW.

## CATHODE GROUND DESIGN

*Figure 6* shows the DH0035 driving a cathode grounded PIN diode switch. The peak turn-on current is given by:

$$Ipk \cong \frac{(V^+ - V^-)(h_{fe} + 1)}{R3} \quad (14)$$

= 800 mA for the values shown.

The steady state current, $I_{DC}$, is set by Rp and is given by:

$$I_{DC} = \frac{(V^+ - 2V_{BE}}{\frac{R3}{h_{fe} + 1} + R_P} \quad (15)$$

where: $2V_{BE}$ = forward drop of $Q_4$ base emitter junction plus $V_f$ of the PIN diode = 1.4V.

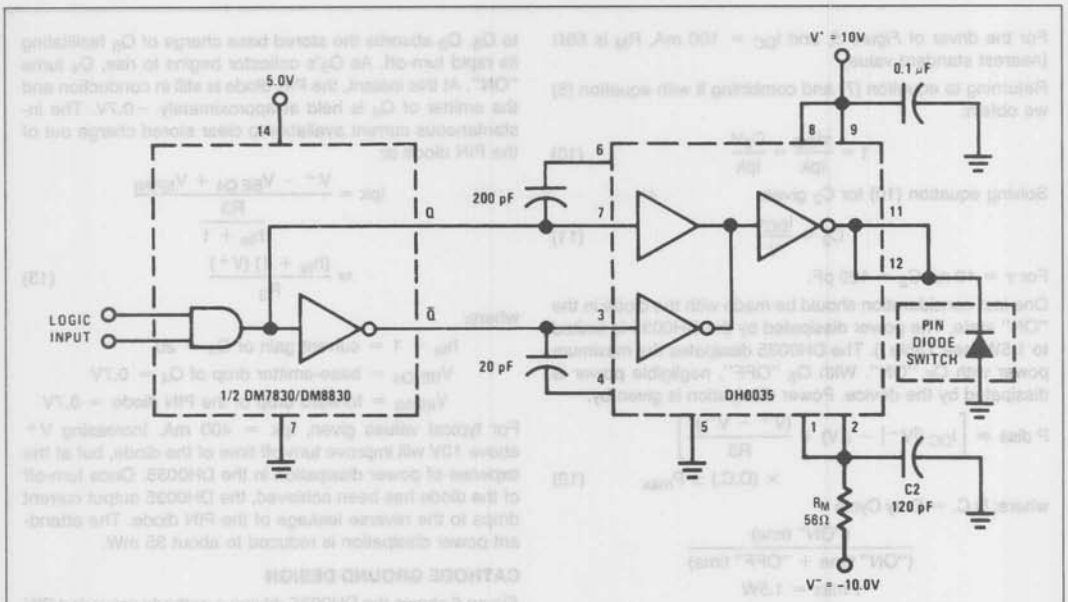


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**FIGURE 6. Anode Grounded Driver**

In terms of Rp, equation (15) becomes:

$$Rp = \frac{(h_{fe} + 1)(V^+ - 2V_{BE}) - I_{DC}R_9}{(h_{fe} + 1)\, I_{DC}} \qquad (15a)$$

For the circuit of *Figure 6*, and $I_{DC}$ = 100 mA, Rp is 62Ω (nearest standard value).

It now remains to select the value of $C_1$. To do this, the change in voltage across $C_1$ must be evaluated. In the "ON" state, the voltage across $C_1$, Vc, is given by:

$$(Vc)_{ON} = \frac{V^+R_3 + Rp(h_{fe} + 1)(2V_{BE})}{R_3 + (h_{fe} + 1)\, Rp} \qquad (16)$$

For the values indicated above, $(Vc)_{ON}$ = 3.8V.

In the "OFF" state, Vc is given by:

$$(Vc)_{OFF} = \frac{V^+R_3 - |V^-|Rp}{Rp + R_3} \qquad (17)$$

= 8.0V for the circuit of *Figure 6*.

Hence, the change in voltage across $C_1$ is:

$$V = (Vc)_{OFF} - (Vc)_{ON} \qquad (18)$$
$$= 8.0 - 3.8$$
$$= 4.2V$$

The value of $C_4$ is given, as before, by equation (11):

$$C_1 = \frac{I_{DC}\tau}{V^-} \qquad (19)$$

For a diode with $\tau$ = 10 ns and $I_{DC}$ = 100 mA, $C_1$ = 250 pF.

Again the power dissipated by the DH0035 must be considered. In the "OFF" state, the power dissipation is given by:

$$P_{OFF} = \left[\frac{V^+ - V^-)^2}{R_3}\right] (D.C.) \qquad (20)$$

where: D.C. = duty cycle = $\frac{\text{"OFF" time}}{\text{"OFF" time} + \text{"ON" time}}$

The "ON" power dissipation is given by:

$$P_{ON} = \left[\frac{(Vc)_{ON}^2}{R_3} + I_{DC} \times (Vc)_{ON}\right](1 - D.C.) \qquad (21)$$

where: $(Vc)_{ON}$ is defined by equation (16).

Total power dissipated by the DH0035 is simply $P_{ON} + P_{OFF}$. For a 50% duty cycle and the circuit of *Figure 6*, P diss = 616 mW.

The peak turn-off current is, as indicated earlier, equal to 50 mA × $h_{fe}$ which is about 1000 mA. Once the excess stored charge is removed, the current through $Q_5$ drops to the diodes leakage current. Reverse bias across the diode = $V^- - V_{sat} \cong -10V$ for the circuit of *Figure 6*.

**REPETITION RATE CONSIDERATIONS**

Although ignored until now, the PRF, in particular, the "OFF" time of the PIN diode is important in selection of $C_2$, $R_M$, and $C_1$, Rp. The capacitors must recharge completely during the diode "OFF" time. In short:

$$4\, R_M C_2 \leq t_{OFF} \qquad (22a)$$
$$4\, RpC_1 \leq t_{OFF} \qquad (22b)$$

## CONCLUSION

The circuit of *Figure 6* was breadboarded and tested in conjunction with a Hewlett-Packard 33622A PIN diode.

$I_{DC}$ was set at 100 mA, $V^+ = 10V$, $V^- = 10V$. Input signal to the DM8830 was a 5V peak, 100 kHz, 5 $\mu$s wide pulse train. RF turn-on was accomplished in 10–12 ns while turn-off took approximately 5 ns, as shown in *Figures 7* and *8*.

In practice, adjustment $C_2$ ($C_1$) may be required to accommodate the particular PIN diode minority carrier lifetime.

## SUMMARY

A unique circuit utilized in the driving of PIN diodes has been presented. Further a technique has been demonstrated which enables the designer to tailor the DH0035 driver to the PIN diode application.

## REFERENCES


1. "Pulse, Digital, & Switching Waveforms", Jacob Millman & Herbert Taub, *McGraw-Hill Book* Company, Inc., New York, N.Y.
2. "Models of Transistors and Diodes", John G. Linvill, *McGraw-Hill Book* Company, Inc., New York, N.Y.
3. *National Semiconductor AN-18,* Bert Mitchell, March 1969.
4. *Hewlett-Packard* Application Note 314, January 1967.