Logic design — 5

Clock-driven circuits

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A four-step algorithm for the design of clock-driven (synchronous) sequential circuits is described. Realistic circuit constraints are automatically taken into account by the design process.

The main features to be considered in the design of clock-driven circuits are reliably correct functioning, observation of gate fan-in and fan-out restrictions and ease of maintenance. It is desirable that maintenance engineers should understand the circuit even though it has undergone simplification – a process which can obscure its function. In general the circuits obtained do not use a minimum number of gates, but the design effort is minimal. The design steps are easy to apply and do not require any specialist knowledge.

Functionally the essential characteristic of synchronous sequential circuits is that their operation is synchronised with clock pulses between which no changes of state can occur.

Clocked flip-flops

Clock driven circuits depend on the use of clocked flip-flops, the principal types of which are described in this section. A clocked flip-flop is a bistable element in which the change of the output signal Q is coincident with either the leading or trailing edge of a pulse signal, commonly referred to as the clock pulse. There are four basic types of flip-flop. Toggle or T flip-flop (TFF); SR flip-flop (SRFF); JK flip-flop (JKFF); D flip-flop (DFF).

Toggle flip-flop. The flip-flop is represented symbolically by the diagram in Fig. 1(a). It has no data input terminals and physically its output "toggles" or changes state with every clock pulse. The logical behaviour of this flip-flop is described by the truth table shown in Fig. 1(b). If the T flip-flop is a modified master/slave JK flip-flop it will turn-on when $Q=0$ and C is changing from 1 to 0, that is on the trailing edge of the C-pulse. Similarly it will turn-off when $Q=1$ and C is changing from 1 to 0. The terminal behaviour of this flip-flop is described by the state diagram shown in Fig. 1(c).

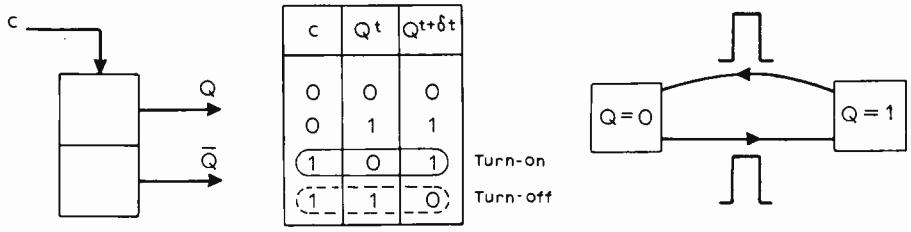

Fig. 1. Symbol (a), truth table (b) and state diagram for a toggle or T-type flip-flop.

SR flip-flop. The sequential equation, $Q=S+\bar{R}Q$, for the SR flip-flop, shown symbolically in Fig. 2(a), was developed in Part 3 of this series. An implementation of an unclocked SR flip-flop, using NAND gates, is shown in Fig. 2(c), and this is frequently drawn in the form shown in Fig. 2(d). A condensed form of the truth table for this flip-flop, called the steering table, is shown in Fig. 2(b) where the entry Φ in the S and R columns means that the input can be either 0 or 1.

By means of the simple modification shown in Fig. 2(e) the SR flip-flop can be clocked. An examination of this diagram shows that if $C=0$ the outputs of g_1 and g_2 will always be logical 1 irrespective of the present values of S and R, or of any changes in these two inputs. The flip-flop can only change its output during a clock pulse transition and, assuming zero gate delay, the output Q will change state on the leading edge of a clock pulse, when C is changing from 0 to 1.

Examination of the steering table or the circuit shows that a clocked SR flip-flop is turned on when $S=1$, $R=0$, and C changes from 0 to 1. Conversely it is turned off when $S=0$, $R=1$, and C is changing from 0 to 1. Hence the terminal behaviour of the flip-flop can be described with the aid of the state diagram shown in Fig. 2(g).

Besides the S, R and C inputs, a clocked SR flip-flop may have one or two additional controls which allow it to assume one of its two states irrespective of whether $C=0$ or $C=1$. These controls are frequently called Clear and Preset. Most commercially-available flip-flops are provided with a clear control, whereas the preset control is not nearly as common. The operation of these controls is described by the table shown in Fig. 2(h) and it should be observed that in the circuit of Fig. 2(f) these signals are active when low.

* With both controls at logical 1 the flip-flop is enabled and operates in the normal way. If $R=0$ and $P=1$ the output $\bar{Q}$ of g_4, in Fig. 2(f) becomes $\bar{Q}=1$. Hence $Q=0$, and the flip-flop is unconditionally reset. If $R=1$ and $P=0$ the output Q of g_3 becomes $Q=1$, and the flip-flop is now preset. The inclusion of these controls leads to a modified state diagram as shown in Fig. 2(i).

The reader should note that if a preset facility is required when the P terminal is not provided it is possible to interchange the Q and $\bar{Q}$ terminals and the input terminals. The clear terminal can then be used as a preset control.

JK flip-flop. The symbolic representation of the JK flip-flop is shown in Fig. 3(a) and the truth table describing its logical operation in Fig. 3(b). The operation of this flip-flop differs in one respect from that of the SR flip-flop in that it is allowable for J and K to be simultaneously equal to 1. If $J=K=1$ the flip-flop "toggles", that is, in row 7 the flip-flop changes state from 0 to 1, whilst in row 8 the converse action takes place. In rows 4 and 5 normal reset and set operations take place as described for the SR flip-flop in the last article.

An examination of the truth table shows that the flip-flop is turned on in

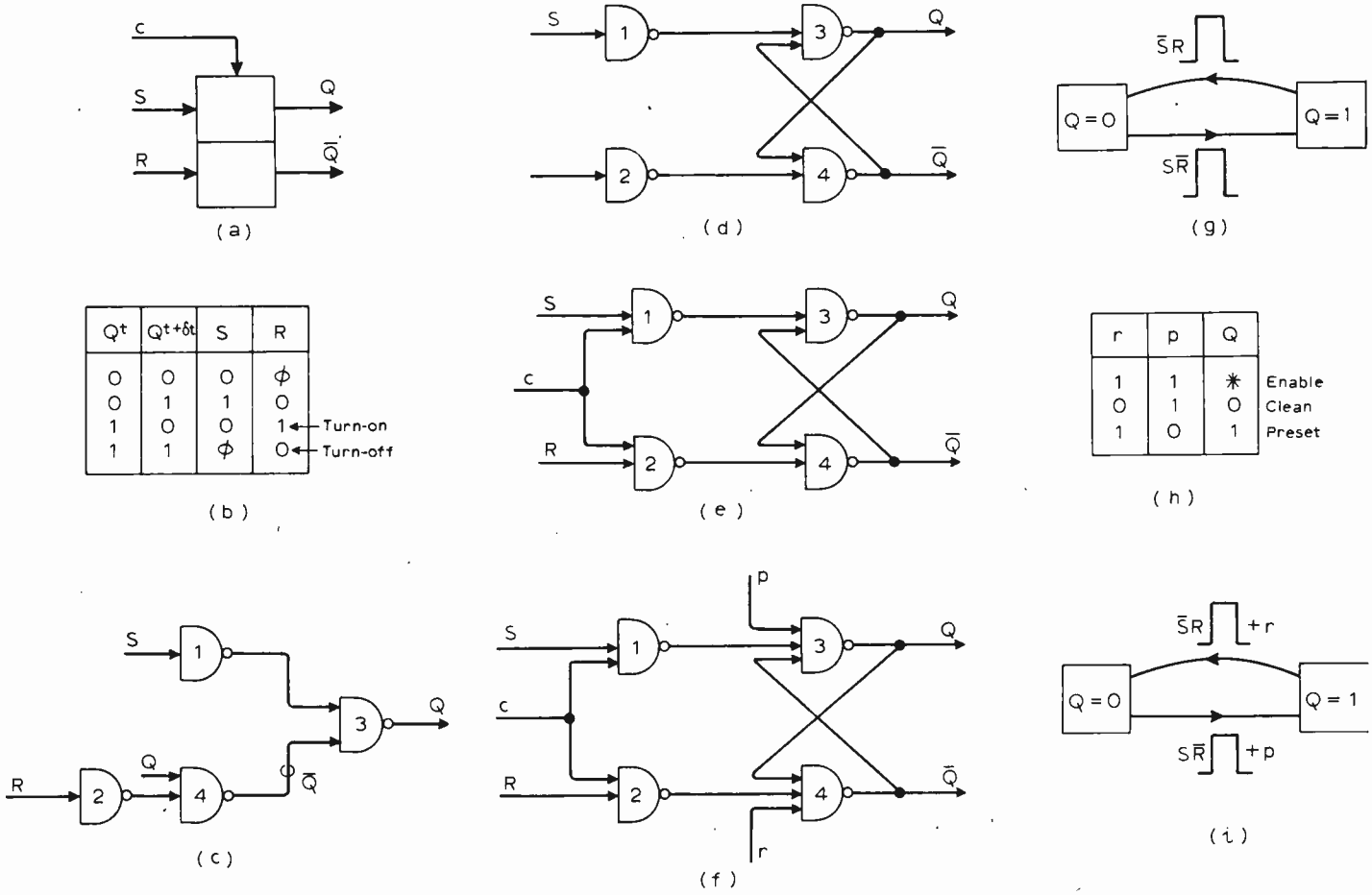

Fig. 2. (a) Symbol for the SR flip-flop, whose steering table is at (b), where Φ indicates either 0 or 1. The SR can be realized, in unclocked form, by NAND gates, as in (c) shown rearranged in a more familiar form at (d). A clocked type of SR is seen at (e) and, with preset and clear, at (f). State diagram for the clocked SR is at (g) and the truth table for P and C can be seen at (h). At (i) is the state diagram for a clocked SR with P and C controls.

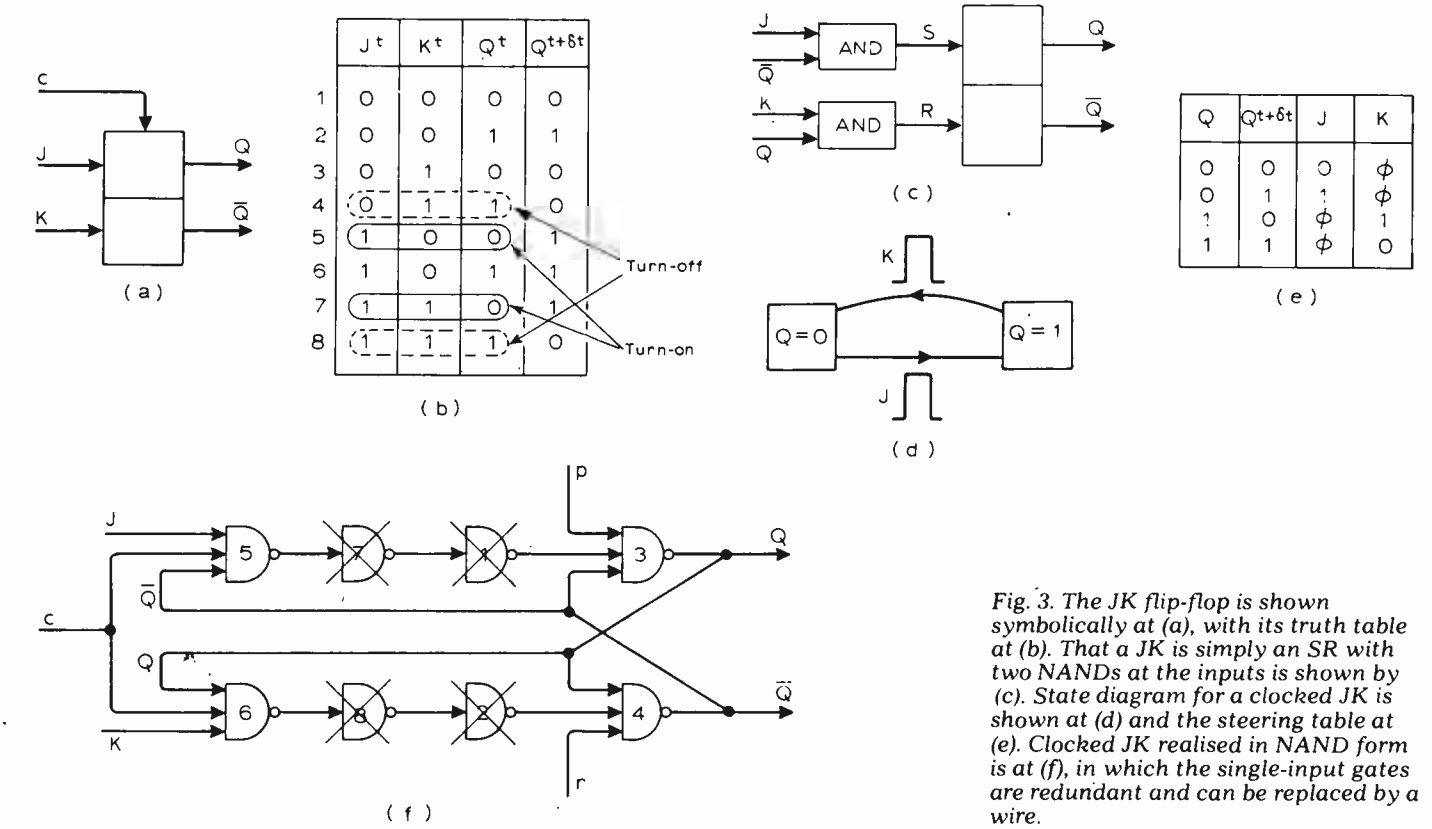

Fig. 3. The JK flip-flop is shown symbolically at (a), with its truth table at (b). That a JK is simply an SR with two NANDs at the inputs is shown by (c). State diagram for a clocked JK is shown at (d) and the steering table at (e). Clocked JK realised in NAND form is at (f), in which the single-input gates are redundant and can be replaced by a wire.

rows 5 and 7, whilst it is turned off in rows 4 and 8.

The turn-on set of Q: $S = J\bar{K}\bar{Q} + JK\bar{Q} = J\bar{Q}$

The turn-off set of Q: $R = \bar{J}KQ + JKQ = KQ$

These two equations indicate that a JK flip-flop is in practice an SR flip-flop preceded by two AND gates which implement the functions $J\bar{Q}$ and KQ respectively, as shown in Fig. 3(c).

The state diagram describing the terminal behaviour of the flip-flop is shown in Fig. 3(d). If the flip-flop is in the state $Q=0$ with $J=1$ and C changes from 0 to 1, it makes a transition to the state $Q=1$. Similarly if in the state $Q=1$ with $K=1$ and C changes from 0 to 1, it makes a transition to $Q=0$.

A steering table for the JK flip-flop is shown in Fig. 3(e). Comparing the steering tables of the SR and JK flip-flops shown in Figs. 2(b) and 3(e) respectively, it will be observed that the JK flip-flop has more Φ or optional input conditions and consequently this type of flip-flop leads to simpler logic when used in the design of clock-driven circuits.

A JK flip-flop can be implemented by connecting the output of the two AND gates in Fig. 3(c) to the S and R inputs of the SR flip-flop of Fig. 2(f). Simultaneously the Q and $\bar{Q}$ outputs of this flip-flop and its clock connections are fed to the inputs of the two AND gates, in conjunction with the J and K lines, as shown in Fig. 3(f). Notice that the AND gates are formed from two pairs of NAND gates in cascade, namely g_5 and g_7, and g_6 and g_8. Clearly gates g_7 and g_1 and gates g_8 and g_2 provide a double inversion. These four gates are therefore redundant and can be omitted from the implementation.

The race-around condition. Unfortunately, satisfactory flip-flop operation is not possible with the circuit shown in Fig. 3(f), for the following reason. If the outputs of the flip-flop, Q and $\bar{Q}$, in Fig. 3(f), change before the termination of the clock pulse the input conditions at gates g_5 and g_6 will also change. For example if $J=K=1$ and $Q=0$, when the clock pulse is first applied Q changes to a 1. This change takes place at $t=\Delta t$ after the start of the clock pulse, as shown in Fig. 4, where Δt is equal to the propagation delay through two NAND gates. At $t=\Delta t$, $J=K=1$, $Q=1$ and $C=1$, consequently there will now be a further change in the output to $Q=0$ at $t=2\Delta t$. The conclusion is that the output of Q oscillates between 0 and 1 for the duration of the clock pulse. Further, at the end of the clock pulse the value of Q is indeterminate.

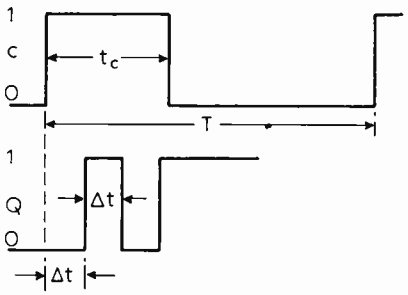

Fig. 4. Illustration of a "race-around", where the output oscillates during the duration of the trigger pulse, t_c.

This phenomenon is called the "race-around" condition. It can be avoided if $t_c < \Delta t < T$. Unfortunately, with modern integrated circuits $t_c >> \Delta t$ and the inequality is not satisfied. This has led to the development of the master/slave or double-rank flip-flop.

Master/slave flip-flop. This consists of two flip-flops in cascade. The leading one, called the master, is connected as a JK flip-flop, whilst the second one, the slave, is connected as an SR flip-flop. Clock pulses are used to enable the master whilst inverted clock pulses are used to enable the slave.

A NAND implementation of a master/slave flip-flop is shown in Fig. 5. Examination of this diagram shows that the master flip-flop changes its state on the leading edge of a clock pulse. For example if $J=1$, $Q_m=0$ and C is changing from 0 to 1, then the output state of the flip-flop changes to $Q_m=1$. Since Q_m is also the set input of the slave flip-flop, $S=1$.

The slave flip-flop is enabled when $\bar{C}$ is changing from 0 to 1, that is on the trailing edge of the clock pulse. If $Q_s=0$, $S=1$ and $\bar{C}$ is changing from 0 to 1 the output state of the slave changes to $Q_s=1$. The change which occurred at the output of the master on the leading edge of the clock pulse is transferred to the output of the slave on the trailing edge of the same clock pulse.

The reader will observe that the slave output cannot change state until after the termination of the clock pulse and consequently the race-around condition can never occur with this type of flip-flop.

D flip-flop. The symbolic representation of a D flip-flop is shown in Fig. 6(a) and its logical operation is described by the truth table in Fig. 6(b).

From the truth table:

$$Q^{t+\delta t} = (D\bar{Q} + DQ)',$$

or:

$$Q^{t+\delta t} = D^t.$$

The interpretation of this equation is that the output Q assumes the logical value of the input at the time of the clock pulse.

In Fig. 6(c) the terminal behaviour of the flip-flop is described with the aid of a state diagram. Assuming that the flip-flop is of the master/slave type, and if $Q=0$, $D=1$ and C changes from 1 to 0, it makes a transition to $Q=1$. Similarly if the state is $Q=1$, $D=0$ and C changes from 1 to 0, it makes a transition to $Q=0$.

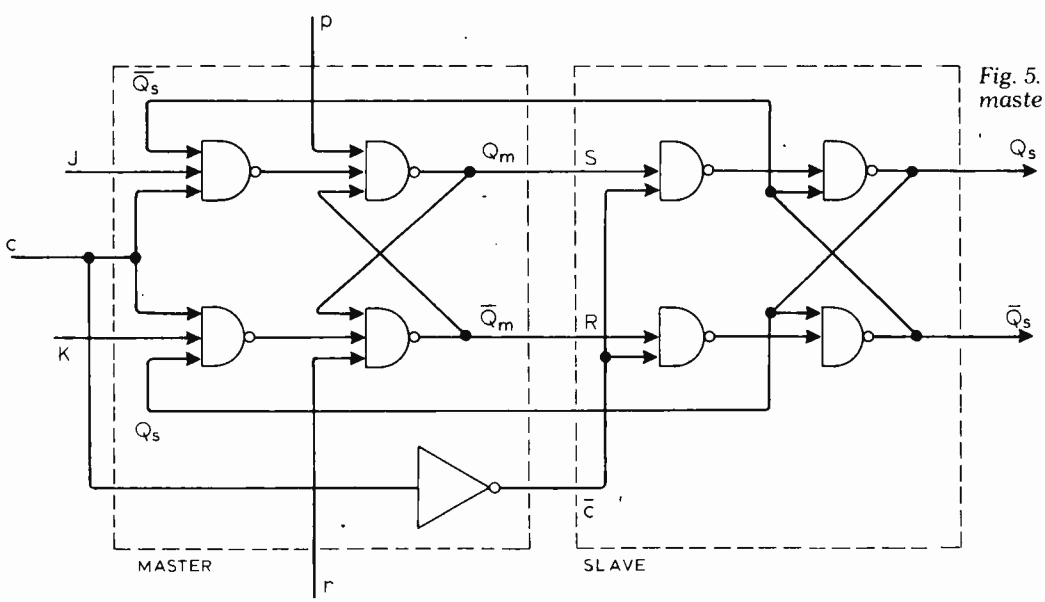

Fig. 5. NAND embodiment of a master/slave flip-flop.

JK versatility. A JK flip-flop can be easily converted to a T type by connecting the J and K lines to logical 1, as shown in Fig. 7(a). The flip-flop then toggles on the receipt of every clock pulse.

To convert a JK flip-flop to a D type the J line, besides being connected to the J input, is also connected to the K input through an inverter, as seen in Fig. 7(b). Referring to the truth table for the JK flip-flop shown in Fig. 3(b), the only entries valid for the configuration of Fig. 7(b) are those in rows 3, 4, 5 and 6. If the column headed J is identified as D and the column headed K is omitted, then the entries in these rows are identical to the entries in the truth table for the D flip-flop shown in Fig. 6(b).

Design steps

The sequence of four design steps for clock-driven circuits is as follows:

(1) **I/O characteristics.** In this step a block diagram is drawn to show the available input signals and the required output signals.

(2) **Internal characteristics.** In the second step the designer specifies the internal performance of the circuit with the aid of a state diagram. The inexperienced designer should be primarily concerned that the specification of the internal circuit operation is complete and free of ambiguities.

(3) **State reduction.** This step is optional and can be omitted. Its main purpose is to provide the designer with the means for reducing the number of internal states used in step 2, if such a reduction is possible. To avoid redundant states this step would be used to reduce the number of states to some power of 2. For example, whereas it would be used to reduce five states to four, it would not be used to reduce four states to three.

(4) **Primitive circuits.** In contrast to the situation with event-driven circuits, the design of clocked circuits does not require that only one secondary signal may change during a transition between two states. This is based on the assumption that all changes of secondary signals take place on the trailing (or leading) edge of the clock pulse that initiates them, and of course before the next clock pulse.

Having allocated the secondary signals, the turn-on and turn-off conditions are written down for each of these signals. For example, in the state diagram of Fig. 8,

Turn-on set of A: $S_A = S_1\bar{X} + (S_2X)$
Turn-off set of A: $R_A = S_3\bar{X} + (S_0X)$
Turn-on set of B: $S_B = S_0X + S_2X$
Turn-off set of B: $R_B = S_1\bar{X} + S_3\bar{X}$

Examination of these equations shows that the turn-on conditions of secondary signal B, S_B, is the disjunction (ORing) of the total states which are necessary for the next clock pulse to cause B to change value from 0 to 1. Similarly the turn-off condition of secondary signal B, R_B, is the disjunction of the total states which are necessary to cause B to change value from 1 to 0.

The expressions for the turn-on and turn-off conditions of the flip-flops can be reduced using as optional products those terms which define "don't care" circuit conditions or alternatively products which define total states involved in transitions in which the signal concerned does not change its value. For example when moving from S_2 to S_3 in Fig. 8, signal A retains its value of 1 and its turn-on conditions can be allowed to arise during this transition. Hence the turn-on equation for A consists of the disjunction of a genuine turn-on condition $S_1\bar{X}$ and an optional product (S_2X). Similarly the turn-off condition for A consists of the disjunction of a genuine turn-off condition $S_3\bar{X}$ and an optional product (S_0X).

The turn-on and turn-off conditions derived by the foregoing process define directly the set and reset signals respectively for a pair of SR flip-flops. However the most readily available and versatile flip-flop is the JK type. As this is used extensively it is worthwhile recalling the relationships derived earlier in this article between S and J, and R and K respectively. They are:

$$S_Q = J\bar{Q} \text{ and } R_Q = KQ$$

Clearly the expressions for J and K can be obtained from the expressions for S and R by dropping $\bar{Q}$ and Q respectively. This is a very useful result and the reader is advised to make a note of it.

The design procedure described above will be illustrated in the next article with the aid of a series of examples.

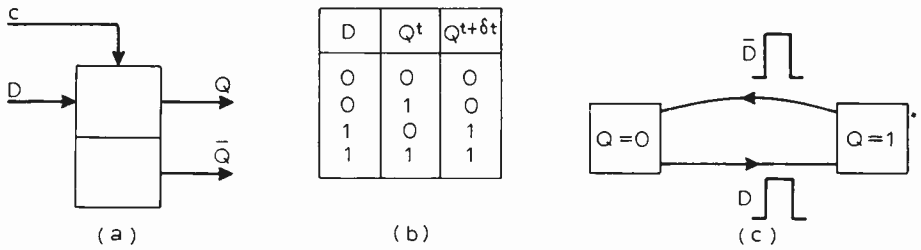

Fig. 6. D type flip-flop symbol (a), truth table (b) and state diagram (c).

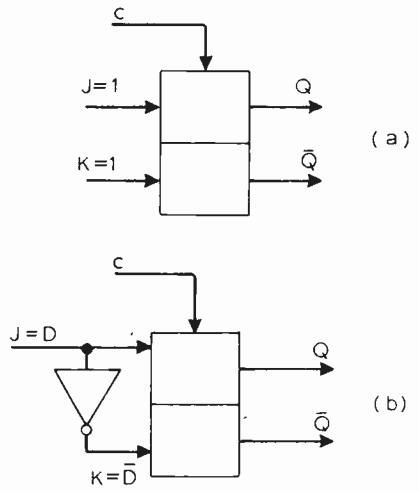

Fig. 7. Illustration of the JK used as a T type flip-flop (a) and as a D type (b)

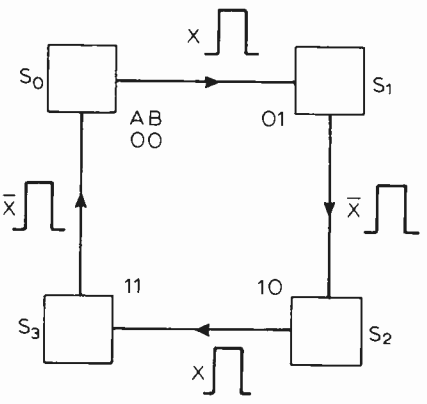

Fig. 8. State diagram for a clock-driven circuit.

Literature Received

Catalogue of power supply components (transistor, rectifiers, regulators) and comple Abbey Barn Road, Electronics Co. High Wycombe, Bucks WW401

Application notes from Hewlett-Parkard on the use of spectrum analysers in noise figure (AN150-9), field strength (AN150-10) and distortion (AN150-11) measurements. Hewlett-Packard Ltd, King Street Lane, Winnersh, Workingham, Berks. WW402

Microwave Newsletter from Walmore, on video detectors, balanced amplifiers, fluorglas laminates, Gunn oscillators and a log amplifier. Walmore Electronics Ltd, 11-15 Betterton Street, London WC2H 9BS WW403

Short-form catalogue of digital-to-analogue and a.-to-d. converters, sample-and-hold amplifiers and data acquisition units, all in dual-in-line packages, from Micro Networks. Tranchant Electronics (UK) Ltd, Tranchant House, 100a High Street, Hampton, Middlesex WW404

Guide to the specification and use of surface-coating resins of many types, prepared by Cray Valley Products Ltd, St Mary Cray, Kent BR5 3PP WW405

Instrument-case catalogue from Lektrokit details the complete ranges of Motek and Lektrokit modular cases, including the newer Transistek types. Available from Lektrokit Ltd, 3 Trafford Road, Reading, RG1 8JR WW406

Data sheet on the Weir 250mA, plug-in power supply for op-amps, with an output variable from ± 12V to ± 15V. Weir Instrumentation Ltd, Durban Road, Bognor Regis, Sussex WW407