The maximum power transfer theorem

Why do we not match loads to the output resistance?

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ELECTRONIC equipment contains many examples of signal sources connected to loads: a microphone feeding an amplifier, an amplifier driving a loudspeaker and an i.f. stage leading to a diode detector are a few typical examples.

In each of these a signal is transferred from a generator to a load and the circuit can be represented in essentials as in Fig. 1, in which the generator is shown with an internal resistance r_g and the load is a resistance R_L. If it is desired to transfer maximum signal voltage from generator to load then R_L should be large compared with r_g but if maximum signal current transfer is required R_L should be small compared with r_g.

To transfer maximum power from generator to load, R_L should be equal to r_g. This can be shown readily by mathematics. The current in the load is given by $I = E/(r_g+R_L)$ and therefore the power I^2R_L is equal to $E^2R_L/(r_g+R_L)^2$. This is a maximum for given values of E and r_g when $R_L=r_g$. When R_L equals r_g the voltage across the load is one half the open-circuit voltage of the generator (i.e. the value obtained across an infinite load resistance) and the current in the load is one half that delivered by the generator into a zero-value load resistance.

Now transistors and valves behave approximately as resistive generators and Fig. 1 is often used as the equivalent circuit for an active device, r_g being replaced by r_a, the anode a.c. resistance of a valve, or r_c, the collector a.c. resistance of a bipolar transistor, or r_d, the drain a.c. resistance of a field-effect transistor. It is rare, however, in practical circuits to find an active device driving a load equal to its own internal resistance. For example a rule of thumb commonly advocated to obtain maximum output power from triode valves is $R_L = 2r_a$ whereas for pentode valves the recommended optimum load is usually a small fraction of r_a (e.g. a pentode with r_a = 100 kilohms might require an optimum load of 7 kilohms). For transistors there is in general no apparent relationship between the optimum load and the transistor internal a.c. resistance.

Fig. 1 can also be taken as representing the output stage of an amplifier as indicated in Fig. 2, and here the generator internal resistance is shown as r_{out}, the output resistance of the amplifier. If the output stage of the amplifier consisted of a single transistor without feedback r_{out} would be equal to r_c but it is common practice in linear amplifiers to apply considerable negative feedback, one effect of which is to reduce the effective value of r_c. Thus r_{out} is normally small compared with r_c and in high-quality amplifiers is commonly only a fraction of an ohm – smaller than likely values of load resistance. The ratio of load resistance to output resistance is known as the damping factor and a typical value is 25. For maximum power output the load resistance should, according to the maximum power transfer theorem, be equal to r_{out} so here is another example where the theorem is apparently ignored.

Consider a typical transistor stage which is required to deliver appreciable power. An example is the final i.f. stage in a receiver which is required to feed a diode detector. The mean collector current of such a stage might be 3mA and the mean collector voltage 9V. For a silicon planar transistor the collector a.c. resistance might be 1 megohm but if the circuit connecting the transistor to the diode is designed to present the transistor with an effective load of 1 megohm then it is immediately obvious

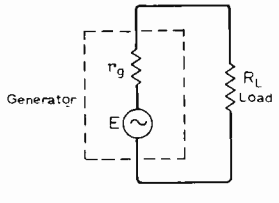


Fig. 1. *A purely-resistive load R_L connected to a purely-resistive generator r_g.*

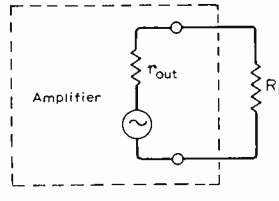


Fig. 2. *The circuit of Fig. 1 arranged to represent conditions at the output of an amplifier.*

that full advantage cannot be taken of the collector current swing available. The maximum undistorted current swing available is 3mA but this, in a 1-megohm load, will generate a collector voltage of 3kV! In fact only a 9-V collector voltage swing is possible without distortion and this can be generated across a 1-megohm load by a current swing of 0.009mA – less than one three hundredth of that available! The power output under these conditions is less than 0.05mW, certainly insufficient to drive a diode detector.

Thus in this example the transistor could not be presented with a load equal to its own r_c because of the enormous collector voltage excursion which would be required to make full use of the current swing available. A more practical value of collector load resistance is 3 kilohms, for this makes full use of the current swing of 3mA and the voltage swing of 9V. The power output so obtained is 13mW, quite adequate for diode detector operation.

Now consider an emitter follower stage and suppose the emitter current is 1mA. The emitter a.c. resistance will be of the order of 25 ohms and, according to the maximum power transfer theorem, this should also be the resistance of the optimum load. Let us suppose that the transistor has a supply of 9V. The emitter potential swing is then limited to ±4.5V but to generate such a value across a 25-ohm load requires an emitter current swing of 180mA! The maximum swing possible is only 1mA, giving a maximum output voltage swing of 25mV. In this example we could not use a load resistance equal to the output resistance because of the very high emitter current required.

In the two examples described above use of a load resistance equal to the output resistance necessitated a very high output voltage or output current. This was because we were attempting to obtain the maximum output power of which the active device was capable with the given values of quiescent collector voltage and current: in fact we were trying to make maximum use of the available voltage and current swings, which is a normal design procedure for stages required to deliver appreciable power. But suppose instead we give the transistor an input signal so small that even with a load resistance

equal to the collector a.c. resistance the swings in collector voltage and collector current are small compared with the quiescent values. Admittedly this is an impractical form of amplifier because the output power would be minute, but the point is whether with such a small signal the optimum load is equal to the collector a.c. resistance.

It is interesting and instructive to try to answer this question using the transistor characteristics. Fig. 3 shows an idealised set of I_c-V_c characteristics, the slope of which is equal to the reciprocal of the collector a.c. resistance. Q is the quiescent point representing the static values of collector voltage and current. Through Q is drawn the load line PQR, the slope of which is equal to the reciprocal of the load resistance. If the small input signal swings the base current between the limits of I_{b1} and I_{b2} then the output current swing is given by PS and the output voltage swing by RS. The area of the triangle PRS is proportional to the power output: in fact if the area is expressed in terms of the horizontal and vertical scales it is equal to four times the power output. As the load resistance value is varied, the load line pivots about Q and the area of the triangle varies. For very small load values PR is nearly vertical and side RS tends to zero, whereas for very high value loads PR is nearly horizontal and PS tends to zero. Between these two extremes there is a position of PR which gives maximum area of PRS.

The solution to this exercise is that the area is a maximum when the slope of PR is equal to that of the characteristics, i.e. when the load resistance is equal to the generator resistance, thus confirming the maximum power transfer theorem. As we have seen this is true provided very small signals are used, and this is a useful reminder that the equivalent circuit for active devices applies only to small signals.

What has been said about the impracticality of using the theoretical optimum load in an amplifier with normal signal amplitude will help us to understand the observation made earlier that the load resistance for a high-quality amplifier is usually many times the output resistance. Let us assume initially that the output stage is a single class A amplifier. The I_c-V_c characteristics of a bipolar transistor are shown in idealised form in Fig. 4. The collector current swings above and below the quiescent value when an input signal is applied and there are limits to both swings if distortion is to be avoided. On the upward swing the collector current must not exceed the maximum value $I_{c(max)}$ prescribed by the manufacturer. Moreover the collector dissipation must not exceed the maximum $P_{c(max)}$ quoted by the maker.

There are other causes of current limitation: in valves, for example, attempts to drive the anode current above a certain value cause the grid to go positive with respect to the cathode so that distortion occurs in the input circuit as a result of damping due to grid current. A similar limitation occurs in junction field-effect transistors, the input circuit of which also conducts when the gate potential equals that of the source. Because of these limitations collector current must not enter the upper shaded area in Fig. 4: the boundary of this area consists of a straight line representing $I_{c(max)}$ and a curve representing $P_{c(max)}$.

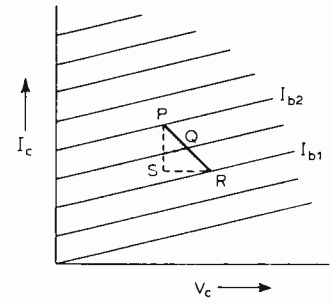
Similarly the greatest negative excursion of the collector current is that which causes its value just to reach zero. Thus the area below $I_c = 0$ is another region which must not be used. The quiescent point Q is located midway between the base line (which we can call the floor) and the lower limit of the upper shaded area (the ceiling). The load line must pass through Q and, to use the full range of collector current, must touch the ceiling and the floor at its ends. It should also use the full voltage excursion between zero and twice the supply voltage: its position is thus fixed at PQR. This represents a load resistance given by the supply voltage divided by the mean collector current. It is thus independent of the a.c. resistances of the transistor.

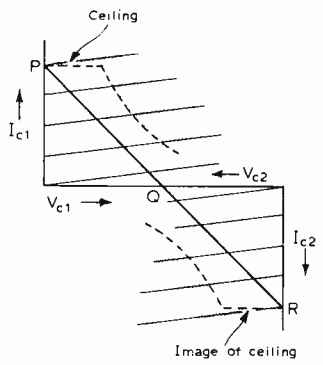
The effect of applying voltage-derived negative feedback is to replace the I_c-V_c characteristics shown solid in Fig. 4 by a new set (shown dashed) much more vertical (implying a lower effective collector a.c. resistance), more evenly spaced (showing improved linearity) and more closely spaced (indicating reduced gain). The manner in which these new characteristics may be deduced was given in an earlier article.* According to the maximum power transfer theorem the slope of the optimum load line should be equal to that of the dashed characteristics (as shown by P'QR') but clearly this is impractical because, to utilise the full voltage excursion, the current would extend well into the shaded areas as in the emitter-follower example considered earlier. The application of feedback has no effect on the position of the floor and ceiling: it, therefore, has no effect on the load line and on the value of the load resistance.

It is, of course, more usual to use a push-pull pair operating in class B in the output stage of a high-quality amplifier. The output voltage is not now accommodated between a ceiling and a floor because the half cycles of signal are handled alternately by the two transistors. There is therefore no floor as in Fig. 4. Instead the load line is bounded by two ceilings, the lower of which can be regarded as a skew-symmetrical image of the upper ceiling situated below the zero-current axis (Fig. 5). Nevertheless the result is that the optimum load line is confined between the two ceilings and fixed in position by the need to exploit the available swings in current and voltage. As before the application of feedback replaces the near-horizontal characteristics by near-vertical ones but has no effect on the position or slope of the load line. Thus the value of the optimum load is unaffected by feedback which is used to improve linearity and to reduce the value of the output resistance. □

* *Wireless World* August 1976, p.66.

Fig. 3. *A load line PQR superimposed on a set of I_C-V_C characteristics. The shaded area represents the power output.* ▼





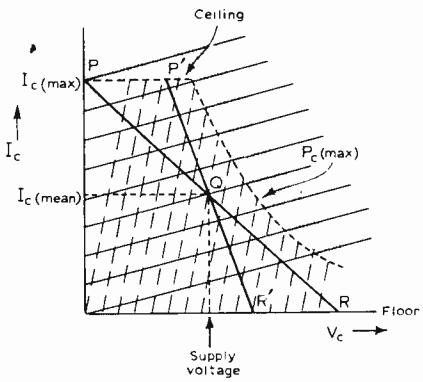


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Fig. 4. *The ceiling and floor which limit the current excursions in a class A amplifier. PQR represents the optimum position of the load line. The dashed characteristics show the effect of negative feedback.*

◀ **Fig. 5.** *In a push-pull amplifier the floor is replaced by an image (skew symmetrical) of the ceiling.*