RECONFIGURABLE ELECTRONICS AND NON-VOLATILE MEMORY RESEARCH

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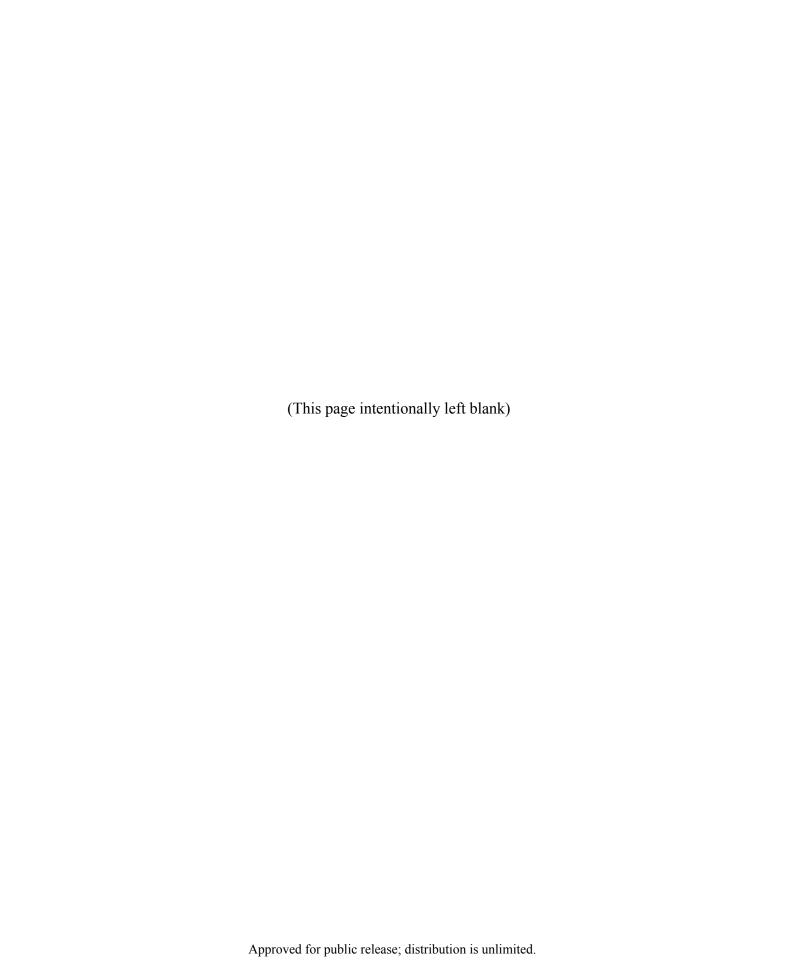Approved for public release; distribution is unlimited.

13. SUPPLEMENTARY NOTES

14. ABSTRACT
The purpose of this research was to investigate reconfigurable electronics and non-volatile memory materials and devices. The primary focus of this work was on device types such as ion-conducting resistive, zero-field splitting memory theory (atomic or molecular memory devices that operate based on a specific quantum mechanical property referred to as zero-field splitting of the atoms/molecules held within a material matrix), as well as multi-state chalcogenide devices based on a layered chalcogenide material structure. Devices were fabricated as single elements or as arrays of devices in order to test their performance. Materials characterization was used to aid in an understanding of device operation and to ultimately improve device performance through better material selection.

15. SUBJECT TERMS
Electronics, memory, nonvolatile, phase change, space

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1   SUMMARY

The purpose of this research was to investigate non-volatile memory device technologies that could be applied to reconfigurable electronics applications and provide power reduction, radiation tolerance, smaller size, and improved reliability over the existing non-volatile memory devices. The research described in this report encompasses: 1) the materials and device design, and 2) the fabrication and testing of the devices. The initial efforts on this work were partially collaborative with another reconfigurable electronics grant through the Air Force Office of Scientific Research (AFOSR) under grant number FA9550-07-1-0546. The types of memory devices that were investigated are divided into three categories:

1) Ion-Conducting, Resistance Variable Memory Devices (also referred to as memristors).
These are devices that change resistance via the movement of metal ions (Cu and Ag ions) through an active device layer, upon proper application of an electric signal. Devices were designed that showed high speed, low voltage/current operation, variable resistance programmability (through spike-timing-dependent-plasticity tests over timing windows of ns to ms), cycling greater than 1 million cycles, and operating temperatures of at least 150 °C without degradation. Many of these materials were tested in two-terminal devices, integrated with CMOS circuits, and in small cross-point arrays during this work.

     Recommendation: Based on the factors of device electrical response and ease of fabrication, the ion-conducting resistance variable memory device has the highest potential for successful application to the area of reconfigurable electronics and non-volatile memory. Based on the materials researched during this work, this type of device also has the most flexibility in altering the device electrical characteristics to fit specific applications.   Devices can exhibit bi-directional resistance tuning using low voltage, small pulse width signals. The technology can be integrated into a CMOS back-end-of-line process with no consequence to an existing CMOS fabrication facility.

2) Atomic or Molecular Memory Based on Zero-Field Splitting (ZFS). This category comprises devices that define the memory state by the interaction energy of the spin-spin and spin-orbit angular moment of the electrons around an atom and the angular momentum (spin-spin and spin-orbit) of the nucleus. The theoretical operation of this type of device is based on the energy splitting produced by this interaction (in the absence of an externally applied magnetic field), referred to as zero-field splitting.   Materials were investigated in order to try find a suitable material that exhibited this property at room temperature with enough electron spin density in one of the energy states for a detectable microwave signal absorption upon transition of an electron between energy states. Materials were investigated in the bulk form, with some showing promise for this application, as observed via electron paramagnetic resonance spectroscopy. However, deposited thin films of these materials did not show high enough signal absorption to indicate that they would be viable for detection at the nanoscale in a memory device. Preliminary device fabrication with these materials also failed to yield a functional ZFS device. This could be due to the electron density being too small in a given state in a device to achieve a high enough signal to noise ratio to detect.

     Recommendation: The ZFS device concept is still high risk and theoretical. It seems that one of the best approaches for exploring the viability of this theory for further study would be to investigate organic molecules as potential candidates since organic molecules frequently

exhibit large spin polarization at room temperature. This increase in signal intensity due to the spin polarization could give rise to a detectable signal within the small size of a bit.

3) Phase-Change Memory. The work in this category included devices consisting of stacked chalcogenide (S-, Se- or Te-containing material) thin films and phase-change alloys that are potentially capable of producing multiple memory states.

Devices fabricated at Boise State University were large compared to the current technology node (1 um diameter vs < 20 nm). This has significant consequences for device operation due to device volume dependence (for melting and quenching the volume of material to change phase). In addition to the larger two-terminal devices fabricated at Boise State, devices were tested that had been fabricated (in collaboration with another project funded by NASA through the Idaho Space Grant Consortium) on integrated circuit die which had been fabricated through the MOSIS consortium, with feature sizes at 0.5 um. Boise State also had the opportunity to collaborate with Micron Technology to test the phase-change stack materials on smaller feature sized devices (40 nm) using Micron's 300 mm wafer test process flow.

Recommendation: It is difficult to change the resistance of a phase-change device consistently and between multiple values. The operation of this type of device depends significantly on the device structure and on the materials and fabrication processes. The energy required to change the resistance of a device is significantly higher than the ion-conducting memory device due to the need to heat the volume of material past the melting temperature. The device structures and fabrication processes needed in order to have lower energy switching and consistent device operation are much more complex, which translates into being more prone to processing errors. However, devices constructed which operate with both the phase-change and an ion-conducting mechanisms within the same device material are viable.

2   INTRODUCTION

The work done in each of the three areas will be described in this report. In this section, background information for each type of memory studied will be presented. The audience for this report is expected to have basic understanding of the non-volatile memory types, electrical characterization techniques, basic properties of materials knowledge, and basic knowledge of semiconductor device fabrication processing.

2.1   Ion-Conducting, Resistance Variable Memory Devices (Memristors)

Background: Variable resistance devices, or memristors [1], have been studied for their potential use in applications such as non-volatile memory [2], neuromorphic and bio-inspired computing [3-9], and threshold logic applications [10]. In general, ion-conducting devices are a type of memristive device that changes resistance through a mechanism involving the generation of mobile metal ions upon application of a potential across the device [11]. The mobile metal ion is generated from an easily oxidized metal, such as an Ag or Cu layer, when a positive potential greater than the oxidation potential of the metal is placed on the electrode nearest the metal layer. A mobile metal cation generated in this process moves via the applied electric field towards the more negative electrode. In the case of a chalcogenide-based device, the mobile metal ions migrate into and through an amorphous material, such as As_xS_y [12], $AgInSbTe$ [13], Ge_xSe_y, or Ge_xS_y [14,15], to eventually form a conductive pathway between the two electrodes in contact with the amorphous material [2,11,12-18], thus lowering the device resistance. Reversing voltage polarities between the electrodes causes the conductive pathway to disperse via generation of metal ions that migrate back towards the metal layer, thus increasing the resistance.

Problems/Challenges: Chalcogenide-based ion-conducting devices comprised of $(Ge_xSe_{1-x})_yAg_{1-y}$ or $(Ge_xS_{1-x})_yAg_{1-y}$ are typically fabricated by either depositing a ternary material (e.g. Ge-S-Ag) to a desired stoichiometry [17], or by photodoping and/or thermally annealing the Ag or Cu metal into the active amorphous material matrix [14,18]. These fabrication methods offer deposition challenges since precise control of the amount of metal included in the chalcogenide and the stoichiometry of the chalcogenide material are both difficult to achieve and are critical to the consistent operation of the device [19,20]. In addition, these fabrication methods limit the maximum temperature allowed in subsequent processing steps due to the reduced glass transition temperatures of Ag or Cu doped chalcogenide glasses, thus limiting even simple processes such as a photolithography photoresist bake step (which is often above 100 ºC). For example, many of the Ge_xSe_y, or Ge_xS_y glasses that can be photodoped with Ag or Cu have glass transition temperatures that are less than 200 ºC [21] prior to doping. These glass transition temperatures drop precipitously when Ag or Cu is added to the material, thus rendering these materials even more sensitive to processing temperatures [19-21]. Therefore, the back-end-of-line (BEOL) processing temperatures as well as device operating temperatures must remain quite low for these processing methods, sometimes lower than 80 ºC, to ensure that crystallization is avoided since the devices do not function consistently when the glass crystallizes. Furthermore, devices incorporating Ag or Cu directly into the chalcogenide film are prone to over saturation with the metal during repeated cycling or as the device is heated (either through Joule or ambient heating), thus eventually limiting and degrading device operation. Lastly, devices which incorporate Ag or Cu directly into the chalcogenide layer are prone to significant electrical

inconsistencies from device-to-device and within the same device. This lack of consistency makes their use in reconfigurable electronics difficult to implement.

Methods of addressing the challenges: Devices with the structure shown in Figure 1, consisting of a Ge_2Se_3 layer adjacent to an M-Se layer material (M-Se = SnSe, Sb_2Se_3, Ag_2Se, PbSe, or In_2Se_3) have previously been fabricated and characterized for high temperature operation (150 °C), cycling endurance, and switching consistency (under grant AFOSR FA9550-07-1-0546). The Ge_2Se_3 layer is the 'active' switching layer with a high glass transition temperature (~ 350 °C), and contains homopolar Ge-Ge bonds. Homopolar bonds were a requirement for material selection in this work since they have previously been empirically shown to produce the most consistent ion-conducting resistance switching in an M-Se device structure [28]. These devices have no Ag-doping requirement; the separate Ag layer provides the source of ions during operation without the need to photodope or thermally drive Ag into the Ge_2Se_3 layer. Since there is no addition of Ag to the Ge_2Se_3 active layer during fabrication, the glass transition temperature remains high throughout processing, thus allowing higher back-end-of-line processing temperatures.
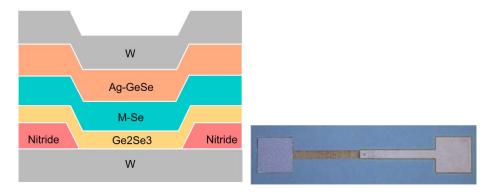
Figure 1. (left) Cross-section illustration of an example device structure. (right) Optical top-down image of a fabricated device. The device is located in the center

The M-Se materials were selected in order to investigate the influence of metal ion oxidation state, size, redox potential, and preferred bonding environment [30] on the device electrical characteristics, with the expectation that the metal from the M-Se layer could migrate into the Ge_2Se_3 layer and perturb a Ge-Ge bonding site, thus altering the device switching properties. Devices with an M-Se layer of either Ag_2Se or SnSe have previously been shown to exhibit memristive behavior [25-28]. It was also previously shown that a Ge_2Se_3/SnSe device with no Ag layer operates with a phase-change mechanism and that Sn migrates into the Ge_2Se_3 layer during operation [29]. In addition, the previous AFOSR study determined that the device structure with an SnSe layer produced an easy to fabricate device with low switching voltages and high temperature (> 140 °C) continuous operation with good cycling endurance (> 1 million cycles), Figure 2. Based on these results, the IC stack in Figure 1 with M-Se = SnSe was selected as the baseline for comparison in device materials studies in this work.
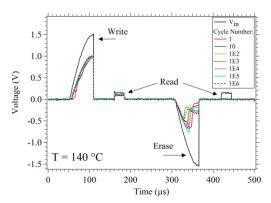
Figure 2. IC stack device cycling response at T = 140 °C.

In order to explore reconfigurability of a device as determined by the ability to tune a device's resistance, the materials and layers were investigated and their influence on device electrical characteristics measured. With every change in material there is likely a corresponding change in the operational parameters, such as cycling lifetime, resistance range, ability to achieve variable resistance, temperature tolerance, energy requirements, etc. A good understanding of the physics of device operation is needed to address how a chemical modification in an ion-conducting device will affect the operation. Theoretical calculations on metal movement into Ge_2Se_3 (both Ag and Sn ions) were initiated in this work. However, due to the time-consuming nature of theoretical calculations, devices were fabricated and tested simultaneously with the ongoing theoretical calculation effort. Without a good understanding of the physics of how the device operates, functionality of devices was addressed through chemical modification of material layers during device fabrication.

Since electrical conduction in amorphous materials is quite different than in crystalline semiconductors, temperature dependence measurements were performed on certain device types in order to help elucidate the conduction mechanisms of the devices. The temperatures studied included the range from 5 K to 350 K, thus covering the full range of possible conduction mechanisms from extended states conduction (~ 270 – 350 K), through variable range and nearest neighbor hopping and tunneling (lower temperature ranges) [30].

In addition, pulsed testing (i.e., application of electrical pulses with shape, variable amplitude and width) was performed on devices with Ag or Cu mobile metal ions in order to investigate differences in speed introduced by the different metal ion and the complexity of the ion movement through the active glass layer. The mobility of the metal ion could also influence the programmable resistance range, and provide information on the influence of the metal ion (size, charge, polarizability) on movement in the device and data retention.

2.2   Atomic or Molecular Memory Based on ZFS

Background: When a paramagnetic transition metal atom or paramagnetic molecule is contained in a matrix material (e.g. glass, protein, liquid) and placed in a magnetic field, the electron spin energy levels split apart as the magnetic field is increased (referred to as Zeeman splitting) as shown in Figure 3 [31-34] for the specific case of the paramagnetic Mn^{3+} ion in the biological enzyme Mn Superoxide Dismutase [34]. The amount of energy splitting can be determined by application of an electrical signal with a frequency that corresponds to the energy separation (splitting) between spin levels; if the signal is absorbed, the frequency of the absorbed signal corresponds to the energy difference between spin states since the absorption is due to the excitation of electrons from one spin level to the other (with consideration to the transition probability). In some transition metals, particularly those with a total electron spin which is an integer value (such as Mn^{3+} which has a total electron spin, S = 2) splitting between the electron

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spin energy levels can occur in the absence of an applied magnetic field. This is referred to as zero-field splitting (ZFS), an example of which is shown in the inset of Figure 3, circled. This ZFS splitting means that no externally applied magnetic field is required to split energy levels, thus allowing for an electron transition between spin states even in the absence of a magnetic field.

The ZFS absorption energy can be predicted from the electron spin Hamiltonian [31]:

$$H = \beta e \vec{B}_O \cdot \tilde{g}_e \cdot \hat{S} + D\left[\hat{S}_z^2 - \frac{1}{3}S(S+1)\right] + E(\hat{S}_x^2 - \hat{S}_y^2) + \hat{S} \cdot \tilde{A} \cdot \hat{I} \qquad (1)$$

This Hamiltonian was applied to the Mn^{3+} metal ions in Mn Superoxide Dismutase to calculate the electron spin energy levels, Figure 3. The calculated energy levels show that there is an energy separation between the Ms = +/- 2 spin levels when the applied magnetic field is zero. This is the ZFS energy. The absorption of an applied electrical signal with a frequency corresponding to this energy would indicate that the material was in this particular spin configuration. Modification of the energy levels

Figure 3. Electron spin energy level diagram of Mn^{3+} in the protein Manganese Superoxide Dismutase (from [34])

(for example, through modification of the Mn oxidation state or the ligand environment around the metal ion) would change the absorption frequency, thus indicating a different 'ZFS state'.

Figure 4. Microwave absorption at zero magnetic field from a sample of Na₂O-CaO-MgO-SiO₂ glass doped with 0.1 wt. %MnO₂. Data collected at 77K [35]

If a device could be fabricated with a material that exhibited a reversible ZFS state, it could potentially be used as a non-volatile memory. It should be stressed that the ZFS concept is not similar to magnetic random access memory (MRAM) as there is no applied magnetic field needed, and there is no transfer of spins between material layers.

Another example of signal absorption (resonance) at zero magnetic field is given by Rakhimov who observed a microwave resonance at zero-magnetic field in SiO_2 glass containing Mn^{2+} ions [35] at a temperature of 77 K, Figure 4. These data show that zero-field absorption from transition metals (in this

case Mn^{2+}) can be observed in very simple glass matrices which are promising for ZFS memory.

In addition, initial work under AFOSR grant FA9550-07-1-0546 explored the $(Ge_{40}Se_{60})_{97}Mn_3$ and $(Ge_{23}Se_{77})_{97}Mn_3$ materials as potential candidates for ZFS memory since one shows a zero-field absorption and the other does not, Figure 5.
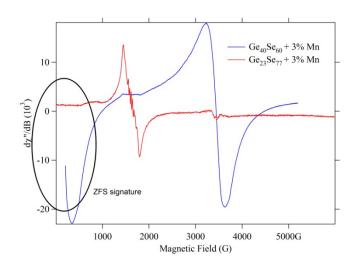
Figure 5. Electron paramagnetic resonance of bulk GeSe-Mn glasses at 4.2 K. A zero-field splitting signature was observed in the $(Ge_{40}Se_{60})_{97}Mn_3$ sample, circled

These systems needed to be explored at higher temperatures to obtain the energy level diagrams and elucidate the differences in the Mn ion environment in the two glass matrices. It was anticipated that understanding the underlying mechanism for the zero-field absorption in the $(Ge_{40}Se_{60})_{97}Mn_3$ glass would allow design of new materials with potential room temperature zero-field splitting absorption.

Of interest in this work is a material that exhibits ZFS at room temperature. There are some recent examples of molecules that have this property. For example, researchers at Oxford University have developed a modified fullerene molecule which exhibits zero-field splitting at room temperature [36].

Problems/Challenges: There are three major challenges to this type of memory. The first is the issue of spin concentration in a small device size. The second is finding a material that exhibits higher temperature (near room temperature or slightly below) electron spin transfer with a high enough signal to noise ratio to detect signal absorption. The challenge of spin concentration ties in directly with the challenge of finding a material that can flip enough electron spins at non-cryogenic temperatures. Since the electrons distribute among all of the energy levels according to a Boltzmann distribution, the higher the temperature, the lower the concentration of electrons in any one given spin state. This has the effect of lowering the detectable signal absorption due to a lower number of electrons in the spin state that exhibits ZFS. The spin concentration needs to be high enough in the appropriate energy levels that the signal to noise ratio of the loss of the input signal due to absorption within the material is large enough to detect whether the exciting signal was absorbed.

The third challenge is finding a method of reversibly perturbing the spin states so that the memory device can change states.

Methods of addressing the challenges: The first two challenges can be addressed by initially performing room temperature EPR measurements on various candidate (integer spin) materials in the bulk state and identifying those with likely ZFS states. Second, cold temperature EPR measurements can be used to map out the electron spin energy levels if an EPR spectrum can be observed and monitored as a function of temperature. Once these two issues are addressed, the

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subset of materials selected for further investigation (from the EPR measurements) is filtered for viable candidates for thin film deposition. From the resultant thin film investigation, likely material candidates and methods of perturbing their spin states can be investigated. These include electric field induced changes, reversible chemical changes, or optically induced spin state changes. Thin films as well as devices of some candidate materials were then tested at room temperature as a function of frequency and magnetic field to investigate potential absorption frequencies.

2.3   Phase-Change Multi-State Memory

Background: Phase-change memory includes chalcogenide materials that undergo a phase-change from a crystalline to an amorphous state upon application of a current through the material, Figure 6, thus creating a device that changes resistance between low and high values [37]. The memory state is held in the resistance value of the device.
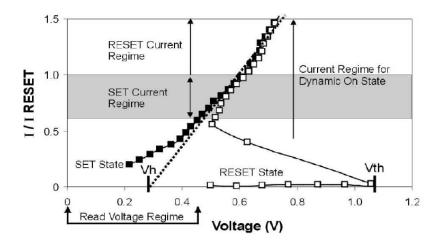
Figure 6. Current-voltage curve for a typical phase-change memory material

In the past several years, an increasingly large research effort within many memory manufacturing companies has gone into the development of a commercially viable phase-change electronic memory. BAE Systems was the first to offer a phase change memory array for sale in the mid 2000's. Later, engineering samples of phase-change memory arrays from Samsung were offered to the public in February 2007. Micron Technology offered a phase-change memory chip to the public for a short time in (beginning in 2012/2013). However, an ideal phase-change material for reconfigurable electronics, that can reliably switch between more than two resistance states to give a multi-state memory, has not been developed.

Previous work showed phase-change memory operation in devices fabricated with layers of chalcogenide materials rather than a single layer of an alloy (such as GST) [29]. The chalcogenide layers tested consisted of a Ge-chalcogenide glass layer and a metal-chalcogenide layer, Figure 7, and showed promise in terms of good cycling endurance.
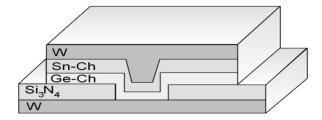
Figure 7. Cross sectional drawing of a stacked layer phase-change memory device. Ch denotes either S, Se, or Te

This previous work showed that phase-change operation was facilitated by the migration of the metal from the metal-chalcogenide layer into the glass layer when a voltage of an appropriate polarity with respect to the metal-chalcogenide layer was applied across the device [29]. Devices with this structure offer advantages over the traditionally studied single layer systems, such as:

- Lower current required for switching, and thus lower power required for operation
- Improved adhesion of the chalcogenide material to the electrodes, thus improving endurance
- Simpler material deposition processes since the phase-change material can be easily sputtered, depending upon the material selection
- The ability to have multiple resistance values depending upon the materials used

The thermal properties of some of the alloys formed when a metal migrates into a Ge-chalcogenide glass layer during operation of a layered film phase-change memory device were studied under a previous Air Force contract, FA9550-07-1-0546. Raman Spectroscopy and differential scanning calorimetry (DSC) were used to observe the bonding structure and glass transition and crystallization temperatures of the alloys. Alloys with multiple crystallization transitions in the DSC data were identified as potential candidates for device fabrication.

Problems/Challenges: Some of the issues associated with fabrication of devices comprising the metal-doped chalcogenide materials include thin film deposition process development. It is not possible in many cases to evaporate a bulk material that exhibits the multiple crystalline transitions into a thin film and maintain the desired material stoichiometry. The physical properties of the resultant thin film can be much different than the bulk starting material. Characterization of the resultant thin film structural and physical properties is also a challenge.

Another challenge involves the electrical characterization of devices fabricated with the new materials. Without the ability to make the device volume very small (such as is the case with a fabrication facility equipped with state-of-the-art photolithography processes capable of < 20 nm feature sizes) it is possible that the fabricated device may require more potential, for longer time periods, to cycle between crystalline and amorphous states than may actually be necessary when used within a memory array with small feature size. This is due to the volume dependent heating necessary to change physical states of the material.

It is also challenging to determine the stability of the device in a given state (data retention) [38] since thermally heating a phase change material, like is done for traditional NVM lifetime

acceleration studies, can cause material migration (from another layer, for example [39, 40]) or structural relaxation of the material.

Methods of addressing the challenges: Materials deposition challenges can be addressed through exploration of materials deposition techniques other than evaporation. Techniques investigated in this work include PECVD deposition of Ge_2Se_3 and transition metals, such as Ti, through collaboration with Prof. Rene Rodriguez at Idaho State University, and cosputtering metals and Ge_2Se_3 at Boise State University. Devices were fabricated using both of these film deposition techniques.   The thin film characterization techniques of Raman spectroscopy and UV-Vis spectroscopy were used to investigate the thin film structure of the materials.

Additionally, the migration of metal between layers of the layered phase change memory stack was investigated through time-resolved X-ray diffraction studies [39, 40] through collaboration with Prof. Santosh Kurinec at Rochester Institute of Technology.

Electrical characterization was addressed through DC and pulsed switching on the large devices fabricated at Boise State, as well as through fabrication of devices on platforms with smaller vias, either through collaboration with Micron Technology or through die fabricated through the MOSIS consortium.

The issue of data retention and stability was not addressed in this work.

3   METHODS, ASSUMPTIONS, AND PROCEDURES

3.1   General Experimental Methods

3.1.1   Fabrication

For each device technology, device fabrication followed similar process flows. The devices are fabricated with either (1) a common bottom electrode (a blanket electrode over the entire wafer/die) or (2) an isolated bottom electrode (all devices are isolated from each other and the substrate). The main process steps in device fabrication for a common bottom electrode process are shown in Figure 8. The isolated bottom electrode process flow is shown in Figure 9. The common bottom electrode process flow is fast and allows for quick turnaround materials tests. These process flows are similar despite the type of mask used, since for any situation, the devices will have either a common or an isolated bottom electrode.

The devices were typically fabricated on 100 or 200 mm p-type Si wafer substrates. These wafers were purchased with the metal bottom electrode layer (W over Cr, Figures 8 and 9). For the case of

Figure 8. Common bottom electrode process flow

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the common bottom electrode devices, the wafers were purchased with a layer of nitride above the metal layer.

The device active area diameter (referred to as the 'via') ranged from 0.13 μm to 60 μm, depending upon the layout and where the via photolithograph was performed. The minimum via size for the Boise State University clean room (the Idaho Microfabrication Laboratory) was 1 μm.

The wafers were sputtered with Ar^+ to clean the W bottom electrode followed by in-situ sputter deposition of a Ge_2Se_3 layer, using an AJA International ATC Orion 5 UHV Magnetron sputtering system and a Ge_2Se_3 target from Process Materials. If present, M-Se layers were deposited by either thermal evaporation using a CHA Industries SE-600-RAP thermal evaporator equipped with three 200/100 mm wafer planetary rotation or sputtering with the AJA sputtering system. The rate of material deposition during evaporation was monitored using an Infincon IC 6000 with a single crystal sensor head. The base system pressure was 1×10^{-7} Torr prior to evaporation. Bulk materials were deposited via thermal evaporation. A W top electrode was deposited by sputtering W (350 Å) using the AJA International system. Etching was performed with a Veeco ME1001 ion-mill by etching through the W and the memristor device materials and stopping on nitride.

Typically devices used three separate layers above the active layer, 150 Å Ge_2Se_3/500 Å Ag/100 Å Ge_2Se_3, which intermingle during sputter deposition to create a mixed conductive layer that is the source of metal ions during operation (denoted Ag-GeSe in Figure 1). The purpose of using these three layers is to create a good adhesion layer for the W top electrode to the active layer.
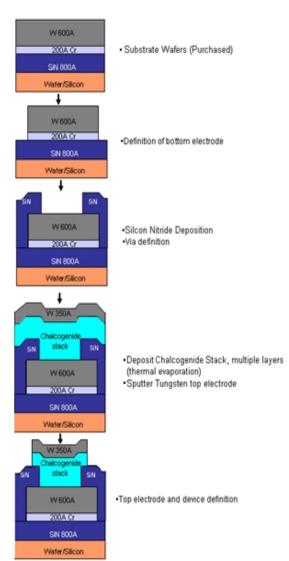
Figure 9. Isolated bottom electrode process flow

3.1.2 Mask Layouts

The main masks created and used in this work for all device types are the in-via layout (which can be used for isolated and common bottom electrode tests), the 10 x 10 array, the 150 x 150 array, and the ZFS layout (high frequency device structures). Each mask is described in this section.

3.1.2.1 *In-via layout.*

The in-via layout includes die with 20 rows of devices, and 9 columns of devices ranging is size from 1 um to 30 um in diameter (Figure 10, isolated bottom electrode case). Variations on this layout were made in which the top and bottom electrodes both have bond pads (Figure 1, right side) instead of the varying length top electrode contacts (shown in Figure 10).

3.1.2.2 *10 x 10 and 150 x 150 array layouts.*

The 10 x 10 and 150 x 150 array layouts are isolated bottom electrode layouts with die each containing one, Figure 11.
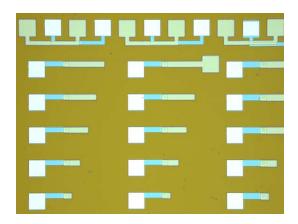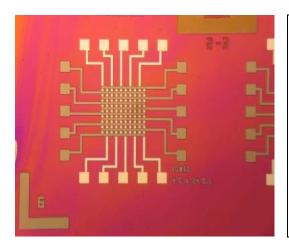
Figure 10. Isolated bottom electrode in-via layout. Top electrode is on the right (varying length lines) and bottom electrode is the square on the left

Split 090520-1E wafers 18 & 19
Completed device pictures
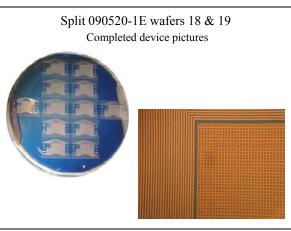
Figure 11. Optical image of a completed 10 x 10 array and portion of 150 x 150 array. The wafer image of the 150 x 150 array is in the center and contains 12 die
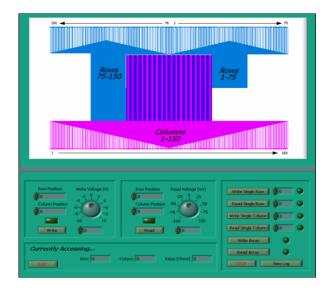
Figure 12. Front panel of the 150 x 150 testing program showing the layout of electrical contacts to the array

3.1.2.3 *ZFS mask layout.*

The ZFS mask set was designed to allow high frequency measurements of devices. To do these measurements, three separate high frequency test structures need to be available during testing. Therefore, the ZFS mask consists of three separate die types on one mask. The three die types are: one-port, two-port, and stacked-one-port. Figure 13 shows the one and two port device layout. In addition, each die contains five types of calibration and test structures (see Figure 14) which is also necessary for high frequency measurements. On each die, device sizes range from 3 um to 60 um. The large die was included to provide more volume for signal detection in the ZFS memory experiments.
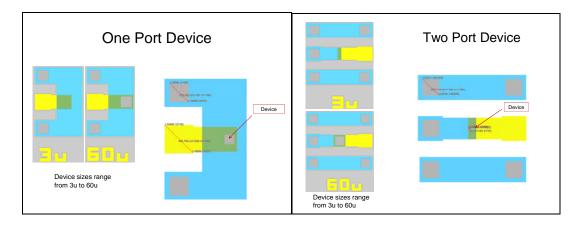
Figure 13. One and Two Port device layouts
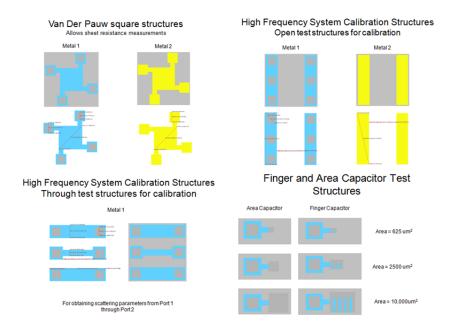
Figure 14. Test structures on ZFS layout. Not shown is the short test structure

3.1.3   Material Characterization and Fabrication Process Step Qualification

All fabrication process steps needed to be developed and qualified before device fabrication.
Characterization methods/tools used for active layer film monitoring include:
1) Raman spectroscopy – active device material characterization
2) UV-Vis – active device material characterization for new materials
3) n&k 1280 broadband spectrometer – film thickness qualification for process steps
4) SEM – as needed for film thickness, profiles, overall cross section view
5) EPR – for thin film ZFS investigations

3.1.3.1   *Raman spectroscopy.*
Raman spectroscopy is typically used to characterize and then monitor in-line the active device
layer films. The Raman spectroscopy investigations were performed with a backscattering
configuration using a Renishaw Invia Raman Microscope with a resolution of 1 cm^{-1}. The
scattered light was dispersed by a spectrometer fitted with a 1200 lines/mm grating. The
excitation wavelength was 785 nm produced by a single-mode wavelength stabilized laser diode
(Innovative Photonic Solutions). The Raman spectra were measured three times on different
points for each sample with a 20x objective lens (Leica, N.A. = 0.40) for all room temperature
measurements. The beam spot size was approximately 10 μm at this configuration.

Slight changes in chalcogenide material stoichiometry can be detected easily in the Raman
spectrum. Therefore, a Raman sample and spectrum was collected with each lot split.   Figure 15
shows Raman spectra for several films of Ge$_2$Se$_3$, deposited at different deposition tool pressure
and power conditions. The changes in the spectra correspond to differences in the Ge-Ge and
Ge-Se bonding environment. The spectrum corresponding to the film that is most desirable for
the IC stack device is the third from the bottom. If a process qualification run produces a Raman
spectrum that is different from this (which is rare once the process conditions for a given sputter

target have been set) then the processing parameters are varied until the film has the desired Raman spectrum (and therefore, associated chemical structure).
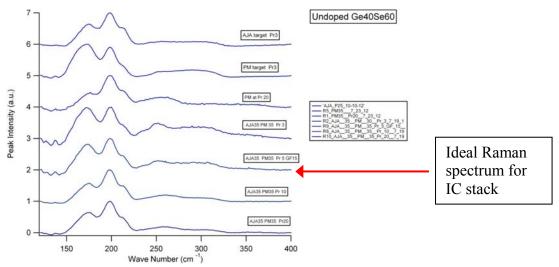
Figure 15. Raman spectra of Ge$_2$Se$_3$ films collected under different processing conditions.

3.1.3.2   n&k tool.

The n&k 1280 broadband spectrophotometer tool uses film reflectance to calculate film thickness via a set of proprietary algorithms and a developed recipe for material type. The tool can also be used to collect transmission spectra. Recipes must be developed for each film type (and stack) that is measured. Once the recipe has been developed, the film thickness can be determined to typically 50 Å. This tool is necessary for processing since it is a fast and reliable way to determine film thicknesses in-line.

3.1.3.3   UV-Vis.

New materials are characterized with UV-Vis in addition to Raman to try and learn more about the electronic structure of the material. The n&k tool is used to collect transmission and reflection spectra.

3.1.3.4   SEM imaging.

SEM imaging is typically used for initial materials morphology and thickness studies, or when something has gone wrong in the process and the source of the breakdown needs to be determined. Figure 16 shows a SEM image of evaporated SnSe above a W layer. Note in this case, the SEM imaging was used to investigate the structure of the rough SnSe film.

Figure 16. SEM image of evaporated SnSe film above a layer of W

3.1.3.5   EPR spectroscopy.

The EPR spectra of chalcogenide glasses were recorded on a Bruker ESP 300E spectrometer operating at X-band

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microwave frequency. A dual mode microwave cavity (Bruker, 4116M/0705) was used in order to allow spectra recording with perpendicular (H1 ⊥ H) or parallel (H1 ∥ H) polarization of the magnetic field vector H1 of the microwave relative to the static magnetic field H. Cryogenic temperatures were obtained with an Oxford ESR900 liquid helium cryostat. The temperature was controlled with an Oxford ITC503 temperature and gas flow controller, typically. Thin films were deposited on mylar strips cut to fit an EPR-grade quartz tube (Wilmad, 707-SQ).

A finger dewar flask (Wilmad, WG-819-B) was used to carry out measurements at 77 K in liquid nitrogen when temperatures did not need to go below 77 K.

Sample illumination was performed using a Dolan-Jenner MI-150R light source with EKE 21 V 150 W halogen lamp of color temperature 3250 K. Light was transmitted from the light source into the dual-mode cavity optical port through Dolan-Jenner B460 fiber with 6.35 mm output diameter, 152.4 cm length, 0.4 to 2.0 microns spectral transmittance and maximum 10 %/ft. at 0.6 microns transmission losses. EPR spectra were recorded on all samples in dark conditions, followed by spectra recording during in-situ illumination. Subsequently, EPR spectra was measured at dark and also, after 15 min of annealing at 300 K.

3.1.4   Electrical

This section describes the experimental requirements for electrical testing of single devices, continuous-wave (CW), pulsed, high frequency, and temperature dependent studies.

3.1.4.1   *Single device measurements.*

Electrical measurements included DC (quasi-static), continuous-wave, pulsed, or RF/microwave absorption. A MicroManipulator 6200 microprobe station, resting on a Technical Manufacturing Corporation MICRO-g air table for vibration reduction, equipped with a temperature controllable wafer chuck was used for the wafer-level device DC, CW and pulse measurements.

DC: DC measurements were performed with either HP4145B, HP4156A, or an Agilent B1500 semiconductor parameter analyzer.

CW: CW measurements were performed on ion-conducting devices using either an HP33250A arbitrary waveform generator and an Agilent 54815A oscilloscope using the circuit shown in Figure 17, or without the external circuit, using only the Agilent B1500 and two integrated waveform generation units for direct measurement of the current through the device upon application of a continuous-wave signal.
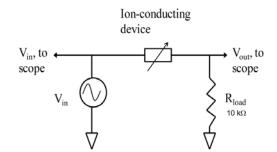
Figure 17. Continuous-wave device measurement circuit schematic for the pulse generator and scope measurement technique

For the oscilloscope and circuit version of the CW measurement, a load resistor (typically, 1 kΩ < Rload < 50 kΩ) was used to limit the current through the device during CW measurements

(since programming current can influence the programmed resistance of an ion-conducting device [18, 22, 23]), and to allow measurement of the voltage drop across the device.   The IV curves of the device, showing the hysteresis loops, are recorded during measurement, Figure 18.
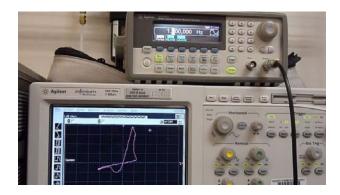
Figure 18. Test set up for the CW measurement using the test set up in Figure 17, showing an IV curve measured for a memristor device

Pulsed: Pulsed measurements (and the B1500 CW measurements) were performed with an Agilent B1500 Semiconductor Parameter Analyzer equipped with two B1511A medium-power Semiconductor Measurement Units (SMU) for DC measurements and a two channel B1530A
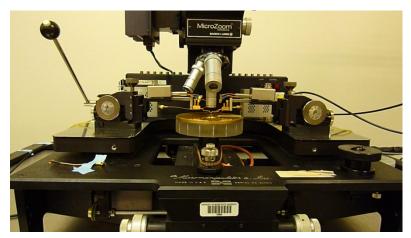
Figure 19. Probe station for pulsed measurements showing the WGFMUs (right and left, rear)

Waveform Generator/Fast Measurement Unit (WGFMU) with two B1531A Remote-sense and Switch Units (RSU) for AC (alternating current) pulsing measurements. The probe station equipped with the micromanipulators and RSUs are shown in Figure 19.

The two-channel WGFMU is a self-contained module with each channel able to generate arbitrary linear waveforms with a 10 ns minimum time step. Each channel can also simultaneously measure current or voltage with a variety of options for measurement range and speed, and the channels share a common ground. The ability to simultaneously apply a test voltage while measuring voltage and current makes it a good tool for rapidly observing changes in device resistance. Each channel of the WGFMU is connected to an RSU located near the probes to improve timing and sourcing. Additionally, each RSU features a switch that allows a direct connection from the SMUs to the device to facilitate high precision DC measurements without the need to lift the probes which could disturb the device state.

Temperature dependence from 298 K to 423 K: Temperature dependence measurements on this probe station were performed using an MC-Systems Hot Chuck Controller with a maximum temperature of 150 °C for the high temperature measurement studies. Devices were equilibrated at the chuck temperature for at least 30 minutes prior to all measurements.

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Cold Temperature from 5 K to 350 K: Low temperature measurements were made using a Lake Shore CRX-4K Probe Station, Figure 20. The CRX-4K facilitates temperature control using two Lake Shore Model 340 temperature controllers, a SHI RDK-408D2 Closed Cycle Refrigerator and an RC-EM10-208230-60 CE Liquid Helium Recirculating Chiller for dewerless operation. Lake Shore ZN50R alumina ceramic probe cards with 25 µm tungsten tips were used for measurements. Probe cards were anchored to the sample stage with copper braiding to ensure temperature equilibration between stage and probe. Vacuum was maintained and monitored with a Varian V-81 turbo pump. Each temperature was equilibrated at least 20 minutes prior to a measurement at that temperature.

Figure 20. Cold temperature probe station

3.1.4.2   10 x 10 and 150 x 150 crossbar array measurements

A test system was designed using a probe card and a National Instruments PXI platform to test the DC response of devices in the array structures. The wafer level probe card is designed to make electrical contact with all of the row and column pads on each array. An autoprober can sequentially step through each die. This system, without the autoprober, is shown in Figure 21 and consists of the following:

1) Completed Wafer Test Demonstration Platform
    a) A wafer-level probe station is used for wafer level access to custom memristor devices
    b) A wafer level probe card has been designed to interface the test electronics to the devices under test
    c) Custom switching circuitry is used to allow multiplexing the 150 rows by 150 columns of devices to 10 rows by 10 columns
    d) Breakout box conversion is used to convert the cabling from the switching circuitry to the input channels of the switch matrix
    e) A National Instruments switch matrix is implemented to convert to 10 rows by 10 columns of circuit output to a single row and column device access point
    f) An Agilent 4156A semiconductor parameter analyzer is used to measure each device in the cross-point array
    g) An EG1032 autoprober can be used to step through all of the test die on a wafer
    h) A custom user interface has been designed to control device access and initiate testing
    a) Data is streamed to CSV files by the test system for storage
    b) Analysis is accomplished using custom Matlab scripting
    c) Reports are auto-generated in MS Powerpoint
2) Control software, written in National Instruments LabView
3) MatLab scripts automatically extract, categorize, and plot data of interest for further analysis and experimentation.
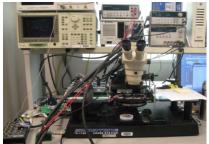
Figure 21. From left to right: Completed array test station; custom decoder board, 300 pin wafer probe card; 10 x 10 probe card; PXI matrix interface board

The 150 x 150 Automated Memristor Test System control software is written in National Instruments LabVIEW and enables fully automated testing and data collection (the main software interface screen is shown in Figure 12). Devices may be tested one at a time, or stepped through a sequence containing user defined measurements.

A memristor test platform was also developed to be used primarily with devices that have been packaged in 16 or 24-pin DIPs, Figure 22. This National Instruments PXI memristor test platform:

1) Was designed to be used with either a wafer level probe station or a pre-packaged test chip
2) Leverages the National Instruments RT PXI instrumentation BUS
   a) High speed, deterministic test hardware
   b) Fully parallel test capabilities
   c) Reconfigurable FPGA based I/O
3) 4-PXI-4132 high precision source/measurement units (SMU) provides synchronized device measurements
4) NI PXI 4x512 switch matrix facilitates device access from a row/column architecture
5) Software written in NI LabVIEW controls the test and data collection system
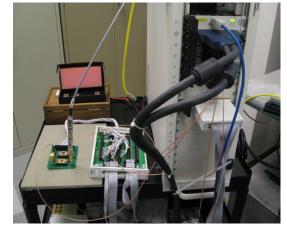
Figure 22. The completed PXI memristor test system showing the PXI based drive electronics (right) and the measurement fixtures (left) configured for package-based testing

The National Instruments PXI based memristor test system is driven by LabVIEW. The primary GUI, Figure 23, provided flexible access to instrumentation settings and devices inside a test array (wafer level or packaged).

An example of data plotted for each measurement as it is collected is shown in Figure 24. Each submenu provides precision control of the PXI system, including fully parallel test and

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measurement capabilities. As with the primary control panel, these panels dynamically adapt to the current measurement sequence.

Figure 23. Data collection software user interfaces for the memristor test platform
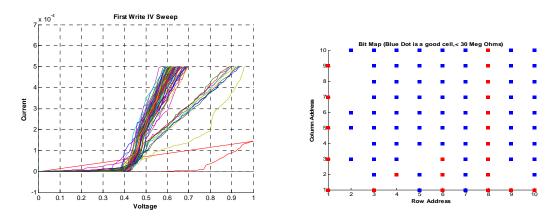
Figure 24. (left) Matlab generated IV plots from 10 x 10 array test data produced by the automated PXI test system. (right) red indicates failed bit; blue good bit

3.1.4.3 ZFS device measurements

The high frequency measurements for the ZFS studies use an Agilent N5224A PNA Microwave Network Analyzer for launching a signal into and measuring the signal through a device with the ZFS structure. This probe station includes a magnetic field, capable of applying fields from 0 to 3500 G, Figure 25. Probe tips used were GSG-150-40A-E-NM (RF probe tip, GSG configuration, 40 GHz, 150 µm pitch, non-magnetic). This measurement is useful during materials characterization to help map out the energy levels in the event that no signal is detected at 0 G (zero-field).
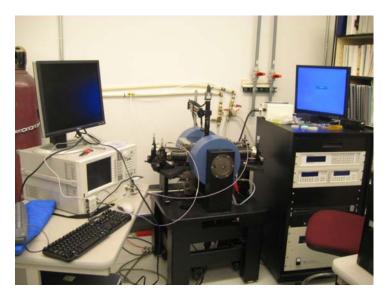
Figure 25. ZFS layout device high frequency test station equipped with a LakeShore EMPX-HF magnetic probe station and an Agilent N5224A PNA Microwave Network Analyzer

3.2   Approach to Ion-Conducting, Resistance Variable Memory Devices (Memristors)

The materials and structure of devices was selected based on the hypothesis that the homopolar (Ge-Ge) bond structure of the active Ge_2Se_3 glass layer influenced the mobility of metal within the ion-conducting device, and thus influenced all of the electrical parameters. Therefore, materials were initially tested for which impurities were added to the active glass layer, building on previous work with the AFOSR (FA9550-07-1-0546) in which bulk materials of Ge_2Se_3 doped with transition metal atoms were fabricated and characterized. By adding these impurities, the Ge-Ge bonding concentration is disrupted, either by increasing or decreasing the amount of Ge-Ge bonds. The electrical response of a device fabricated with these chemical changes could then help elucidate the influence of the Ge-Ge bonding on the electrical properties. Better understanding of the influence of the Ge-Ge bond on the electrical response will help in the design of a device with selected electrical properties for a given application.

The ion-conducting devices fabricated do not require either the ternary deposition or photodoping/annealing processing methods [17, 18, 22-24]. The typical device structure (see Figure 1) is a Ge_2Se_3/SnSe-based structure, referred to as the IC stack (for Ion-Conducting stack).

Ion-conducting devices were fabricated with the four different mask sets as described in Section 3.1.2: 1) a via structure with top and bottom electrodes (an example device stack is given in Figure 1, left), each of which extends to a metal pad for wirebonding or electrical probing access (Figure 1, right); 2) a 10 x 10 cross point array of via structured devices; 3) a 150 x 150 cross point array of via structured devices; and 4) high frequency measurement via structured devices, referred to as the ZFS layout. Devices were also fabricated in collaboration with Micron, using their 300 mm wafer test part with 40 nm device structures.

Electrical characterization over a broad temperature range (5 K to 350 K) was used to further study conduction mechanisms.

Other electrical characterization measurements included: 1) pulsed response (pulse width and amplitude); 2) CW cycling; 3) DC; and 4) pulse programming for incremental, or reconfigurable, response, including spike-timing-dependent-plasticity learning programming.

DC measurements were typically performed using a 'write – erase – write' voltage sweep sequence where 'write' refers to programming a device to a lower resistance by application of a positive potential to the top electrode (the electrode closest to the Ag layer) and 'erase' refers to programming a device to a higher resistance by application of a negative potential to the top electrode. A compliance current set on the semiconductor parameter analyzer limits the current through the device during a DC measurement, and also influences the resistance to which the device is written [18, 22, 23]. The first 'write' is responsible for device conditioning and formation of the channel.

The experiments performed for the ion-conducting device investigations are outlined in Table 1.

In addition to the experimental device fabrication approach, theoretical calculations on the Ge_2Se_3 layer was performed by Dr. Art Edwards (AFRL/RVSE) in order to investigate the movement of Sn and Ag into Ge_2Se_3. The purpose of these calculations was to investigate how the Sn and Ag may ionize and incorporate into the Ge_2Se_3 material. Calculations were performed using the Sandia National Labs supercomputer.

Table 1. Ion-Conducting Experiments

	Project	Description	Comments
1	Ge$_2$Se$_3$ - metal cosputtered films and devices*	Process development	Metals cosputtered include: W, Sn, Cr, Co, Ag, Cu, Ti
		Deposition of cosputtered films	Sputtered on Si (Raman) wafers, quartz slides, and mylar strips (for EPR)
		Characterization of films: Raman, UV-Vis, EPR	
		Fabrication with cosputtered films	Includes process development for device fabrication processes
		Electrical characterization	DC and CW where possible.
2	Cu vs Ag devices*	Electrical characterization	DC temperature studies (5 K to 350 K) and pulsed testing
3	Cu/SnO and Ag/SnO devices*	Electrical characterization	DC and pulsed tests
4	S vs Se devices*	Electrical characterization	
5	Differential Negative Resistance Testing*	Electrical characterization of DNR mode	DC temperature studies (5 K to 350 K) and pulsed testing
6	Constant Current Source Testing*	Electrical characterization of constant current mode	Investigation of programmability and stability of constant current operational mode.
7	Spike Timing Dependent Plasticity Testing*	Developed instrument control, data collection, and analysis software	
8	High frequency electrical testing*	Measurements of the device conduction between DC and 20 GHz.	
9	Idaho State University Collaboration (Prof. Rene Rodriguez)	PECVD deposition of Ti-Ge$_2$Se$_3$ films	Various Ge$_x$Se$_y$ stoichiometries
		Fabrication with ISU's PECVD film	
		Electrical characterization of devices fabricated with the PECVD film.	
10	Micron Technology Collaboration (John Smythe)	Device fabrication on 300 mm wafers	Device active layers were processed at BSU; the rest of the processing was done at Micron.
		Electrical testing of devices	
11	Arizona State University Collaboration (Hugh Barnaby)	Develop masks and a back-end-of-line process for an IC test chip from ASU.	
		Process chips through BEOL process at BSU	
		Electrically characterize devices on chip (not the IC functionality)	
12	Theoretical calculations (Arthur Edwards, AFRL)	Incorporation of Ag and Sn into Ge$_2$Se$_3$	

* These devices use the 'IC stack' which is a basic Ge$_2$Se$_3$/SnSe/Ag-GeSe/W structure. In some cases, the Ge$_2$Se$_3$ layer is replaced with another material.

3.3   Approach to Atomic or Molecular Memory Based on ZFS

In order to determine feasibility of ZFS memory, we initiated the work with an investigation of materials that could potentially exhibit a ZFS absorption. These included metal-doped GeSe materials (from our previous work, this was considered a good candidate), $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO) which was expected to have a ZFS in one of the structural forms, and several organic materials, including pentacene and tri(8-hydroxyquinolinato)aluminum. The materials for which measurements were made are listed in Table 2.

Table 2. Samples investigated for ZFS

Material	Notes
$Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO)	Sputter deposition
$Ge_{23}Se_{77}$ + Mn	Co-Sputtered and evaporated
Ge_xSe_y + Ti	CVD and co-sputtered
$Ge_{40}Se_{60}$ doped with metals. Metals include: W, Cr, Ti, Co, Mn, Sn, Ag, Cu	Co-sputtered
tris(8-hydroxyquinoline)aluminum (Alq3)	Bulk sample only
Pentacene	Bulk sample only

The chalcogenide and PCMO materials were used to fabricate devices. Both of these materials systems can change resistance through the application of an electric field across the device; however in both cases this is also accompanied by a change in structure of the active layer which is what is of interest in the case of ZFS. For the chalcogenides considered, the device must also contain a mobile metal ion in order to modify the material composition. The structural change that PCMO undergoes alters the ligand field environment and subsequently the ZFS parameters.

The organic materials, pentacene and Alq3, provided through collaboration with Prof. John Kymissis at Columbia University, were investigated in bulk through EPR; however, actual fabrication of devices with the candidate organic materials was not performed.

The challenges to the ZFS materials investigation were addressed by first performing room temperature EPR measurements on various candidate (integer spin) materials in the bulk state and identifying those with likely ZFS. From these results, viable candidates for thin film deposition were investigated. In most cases, film deposition was attempted before some of the issues with film deposition were discovered.

Simultaneously with the materials experiments, a study was performed to investigate the possibility of using signal processing techniques to detect the absorption signal for a bit that has multiple ZFS producing species present (Figure 26). The multi-bit cell concept uses multiple transition metal ions within a single bit. Each of these transition metal ions would have a different ZFS energy, thus each absorbing a different frequency of an incoming signal. The cell would then have a state corresponding to any combination of ZFS spin states. For the example shown in Figure 26, the cell with three ions could have a total of 2^3 possible memory cell states. The bit would be read by detecting the transmitted signal as shown in Figure 27.
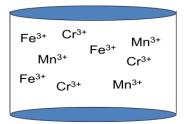
Figure 26. Multi-state memory cell concept for ZFS. With three transition metal ions in the cell, there are potentially three separate ZFS energies
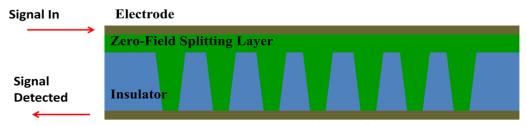
Figure 27. Bit reading scheme for ZFS array row

Signal processing techniques were explored by Prof. Zhu Han at the University of Houston and Prof. John Chiasson at Boise State University. Professor Han applied an approach referred to as the quickest detection method. The quickest detection method built on the hypothesis test, which is the standard way to determine the state of stored bits. In this model, the received signal is y(t) is a function of h(t) and noise n(t). The hypothesis testing (either H0 or H1) is:

$$H1: y(t) = h(t) + n(t) \quad \text{(with signal)} \tag{2}$$

$$H0: y(t) = n(t) \qquad \text{(no signal)} \tag{3}$$

The optimal decision is given by the Likelihood ratio test (Nieman-Pearson Theorem), P(y|H0) and P(y|H1) are the conditional probabilities, and g is a threshold.

$$\text{Select H1 if } \Lambda(y) = \log(P(y|H1)/P(y|H0)) > g; \tag{4}$$

otherwise select H0.

This approach fits well for single user detection. However, for multi-user detection (MUD), multiple locations can store multiple bits. The received signal can be written as:

$$y_i(t) = \sum_{k=1}^{K} A_k e^{-j2\pi F\left[t - \frac{d_k}{C}\right]} b_k + n_i(t)$$

<div align="right">(5)</div>

Where K is the number of locations, A is the gain, d is the distance, F is the frequency, b is the information bit, and n is the noise.

The Quickest Detection Method is a technique to detect distribution changes of a sequence of observations as quick as possible (aqap) with the constraint of false alarm or detection probability. The classification of aqap includes:

- Sequential detection: determine aqap between two known distributions, starting from time zero.
- Bayesian detection: at unknown time, distribution changes between two known distribution. Detect aqap.
- CUSUM test: at unknown time, distribution changes to unknown distribution, Detect aqap.

The ZFS problem fits in sequential detection. The problem has multiple bits and multiple hypothesis. The MUD cannot guarantee the false alarm probability and missing probability constraints. The quickest decision is possible.

The approach to this problem is to join the quickest detection method and MUD. To do this:

- Decode the strongest bit first by regarding the others as noise, then decode the second strongest bit by eliminating the influence of the already decoded bit, and so on.
- The objective for the detection is not to minimize the error, but to minimize the detection time under the false alarm and detection probability
- Can achieve asymptotic optimality
- Compare with the other techniques
- Consider the simple hardware implementation
- Try to develop other joint schemes with linear MUD decoders
- Consider the hardware implementation concerns

3.4   Approach to Phase-Change Multi-State Memory

In this research area, the electrical properties of stacked chalcogenide phase-change materials were investigated. Additionally, a collaboration with Prof. Santosh Kurinec at Rochester Institute of Technology investigated the diffusion of Sn into GeTe and Ge_2Se_3 layers. This research project also collaborated with Micron Technology to test the phase-change layered devices on their 300 mm wafer test part.

Initially in this work, device fabrication was attempted using materials that showed the potential to exhibit multiple resistance states based on the DSC data which showed multiple crystallization temperatures, and did not show inhomogeneity in the Raman spectra (defined from our previous AFOSR grant work). The goal was to determine if there was a correlation between the presence of multiple crystallization peaks in the DSC data of GeSe-M ternary materials and the ability of devices fabricated with $Ge_{40}Se_{60}$/M-Se layers (M = Sn, In, Sb, and Zn) to exhibit multiple

programmed resistance states. With a correlation between multi-state phase-change memory response in a device and multiple crystallization peaks in DSC data one would be able to use DSC as a fast and inexpensive predictive tool to investigate a large number of materials for use as multi-state phase-change memory devices.

For phase-change multi-state memory, the proposed work consisted of the following goals and objectives:

- Fabrication of single bits and arrays for electrical testing and spectroscopic characterization of materials in functional device structures.
- Electrically characterizing multi-state response for applicability in reconfigurable electronics
- Spectroscopic characterization of chalcogenide films and confined materials.
- Recommendation of materials or materials properties for operation in a reconfigurable electronics circuit.

To complete this research, the structure of chalcogenide materials within electrically switchable single-bit devices and arrays was investigated in order to elucidate the structural changes that take place during the phase change, using EXAFS measurements in collaboration with Prof. Michael Paesler at North Carolina State University. This work was also done in collaboration with research performed in the AFOSR grant (FA9550-07-1-0546) and was reported in the final report for that grant in July 2011.

This work also investigated the electrical response of devices comprised of layers of chalcogenide material that have promise for exhibiting multiple stable resistance states.

4   RESULTS AND DISCUSSION

4.1   Ion-Conducting, Resistance Variable Memory Devices (Memristors)

The typical electrical response of the IC stack under DC voltage sweep conditions is shown in Figure 28. In this case, the first and second write threshold voltages are around 0.2 V. The first write sweep forces a potential from 0 to +0.4 V across the device (in this case, with a compliance current of 100 uA). The sweep returns from 1 V through 0 to − 0.3 V. This device erased between -0.06 and -0.1 V. A second write sweep occurs from -0.3 back towards +0.4 V and the sweep ends at 0 V.

This device structure has been shown to operate continuously at temperatures as high as 150 °C.
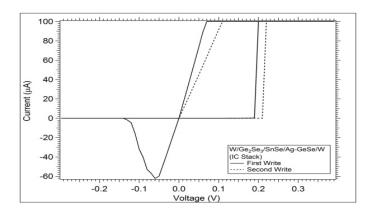
Figure 28. DC voltage sweep of IC stack

Typical CW response for the IC stack is shown in Figure 29. The resistive load test circuit was used for this measurement. The input is a sinusoidal waveform as shown in Figure 29 (a). The voltage measured across the load resistor is shown in Figure 29 (b). The voltage across the device is calculated from the difference (see Figure 29 (a)-(b)) and is shown in Figure 29 (c). The device current is calculated using the load resistance and the voltage across the load resistor and is used to display the device IV curve shown in Figure 29 (d).

IC stack devices typically have a long cycling endurance. During measurements, it is typical to run out of dedicated measurement time before the end of the device cycling lifetime has been achieved. Therefore, the maximum cycles achieved during testing due to this time limitation is 10^{11}.

The resistance calculated for an IC stack device operating at 140 °C is shown in Figure 30 as a function of cycle number.   The voltage across the device was continuously monitored and sampled every decade up to 1 million cycles and used to calculate the resistance shown in Figure 30.
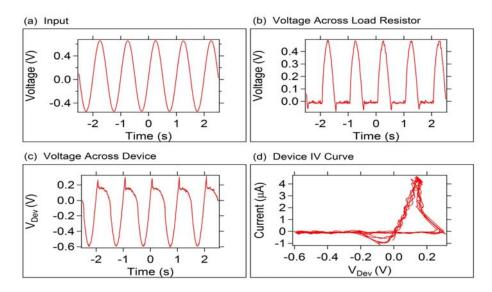
Figure 29. IC stack CW response.

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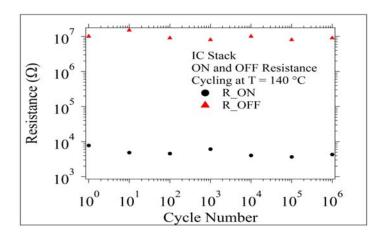
Figure 30. Resistance for the ON and OFF states as a function of cycle number for a device operating continuously at T = 140 °C

The IC stack devices exhibit characteristics of a generic memristor, according to Prof. Chua's classification system [1]. Figure 31 shows the IV curves as a function of frequency for a sinusoidal input. The device was tested at 100 kHz first, Figure 31 (a). The frequency was slowly reduced down to 0. 5 Hz. For the tests at 1 Hz and 0.5 Hz shown in Figure 31 (h) and (i), the amplitude of the sine wave was reduced below the threshold voltage. It was then increased until the device cycled, Figure 31 (j) and (k). Figure 32 shows an expanded view of Figure 31 (l) showing the overlay of all IV curves.
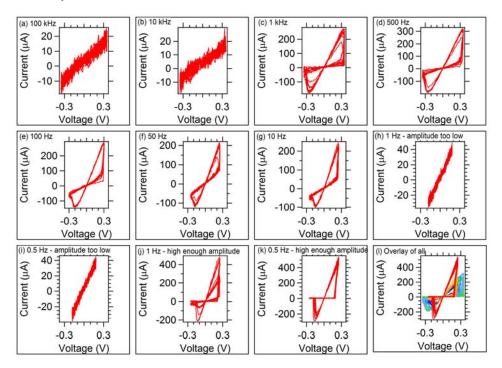
Figure 31. IV curve for IC stack memristor per sinusoidal input frequency and peak amplitude in order tested (a)-(k). An overlay of all of the frequency response IV curves is given in (l)
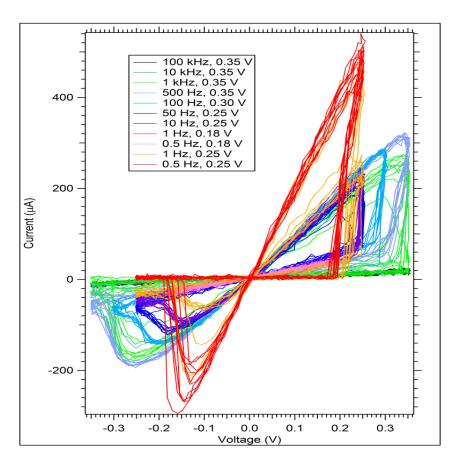
Figure 32. The overlay plot from the previous figure of the IV curves taken as a function of sinusoidal signal excitation for an IC stack memristor

The frequency response of the memristor shows that the areas of the lobes of the hysteresis loops increase as the frequency is reduced. As the frequency is increased, the lobe area goes to zero (see Figure 31 (a) and (b)). This is a classic generic memristor characteristic.

4.1.1 Metal Cosputtered Films and Devices

Film deposition processes for metal doped films were developed using the technique of cosputtering Ge_2Se_3 and metal target. This cosputtering process usually involved one metal target and the Ge_2Se_3 target. In two cases, ternary cosputtering between two metal targets and the Ge_2Se_3 target was developed.

In some cases, film compositions were determined through collaboration with Micron Technology, using ICP-MS, and optimized so that the concentration of metal in the Ge_2Se_3 film was around 1 to 8% (see the example for Ti-doped films, Figure 33). In most cases, devices fabricated with metal concentrations higher than this produced conductive devices with no resistance switching.

	Sample Description	Ti power 0	Ti Power 12 W	Ti Power 15 W	Ti Power 18 W	Ti Power 21 W	Ti Power 25 W
	Analysis Date	10/3/2012	10/3/2012	10/3/2012	10/3/2012	10/3/2012	10/3/2012
mole ratio	Ge	38.1	34.5	33.4	32.0	31.0	29.9
	Se	61.9	56.7	54.8	53.7	52.0	50.1
	Ti	0.0	8.8	11.8	14.4	17.0	20.0
	Mole ratio sum	100.0	100.0	100.0	100.0	100.0	100.0
Analyte Recovery	Mass (g)	0.0030	0.0030	0.0030	0.0031	0.0019	0.0031
	% of samp. wt.	87.0	94.3	96.9	103.7	107.7	95.7
Sample Weight	pre-etch wt.	9.6369	9.6475	9.6811	9.6884	5.9437	9.661
	post-etch wt.	9.6335	9.6443	9.678	9.6854	5.9419	9.6578
	wt. removed	0.0034	0.0032	0.0031	0.003	0.0018	0.0032
Solution S1	bottle tare wt.	24.8055	24.8639	24.8367	24.843	24.8426	24.7207

Analysis performed by Micron Technology Inc. No contamination of Al, Ag, Cu, Ni, or W seen within the detectable limits

Sample ID	Al (ug/wafer)	Ag (ug/wafer)	Cu (ug/wafer)	Ni (ug/wafer)	W (ug/wafer)
1	<1.3	<1.3	<2.2	<3.3	<4.2
2	<1.3	<1.3	<2.2	<3.3	<4.2
3	<1.3	<1.3	<2.2	<3.3	<4.2
4	<1.3	<1.3	<2.2	<3.3	<4.2
*5	<2.1	<2.1	<3.6	<5.4	<6.9
6	<1.3	<1.3	<2.2	<3.3	<4.2

* Wafer was broken, largest piece was etched

Figure 33. Example ICP-MS analysis for Ti-cosputtered films. The power for the Ti target was varied from 0 to 25 W; the corresponding increase in Ti concentration was measured

4.1.1.1 Raman

Figure 34 shows the Raman spectra of the cosputtered films and the bulk materials. The bulk material contains 3 % of metal dopant. The films contained between 1 and 8 % metal. Note that bulk samples with Ni and Fe were also synthesized (during AFOSR collaboration), but are not included in the graph since they did not have features different than the Ge_2Se_3 undoped sample and due to the sample appearance there was a question as to the homogeneity of the sample synthesized.

Processes could not be developed for the V, In, Sb, Zn, Fe, or Ni co-sputtered films, so devices were not made with these.

Major differences between the bulk and the thin film structure (as seen in the Raman) exist for the W, Sn, Mn, Cu, Cr, and Co cases. However, the concentration of metal dopant is different as well and this can have a significant impact on the chemical bonding.
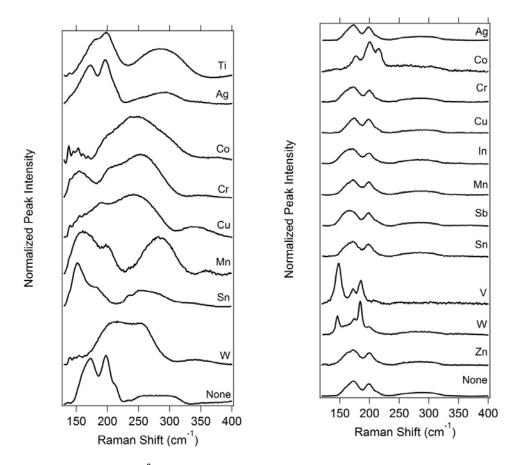
Figure 34. 300 Å thin film (left) and bulk Raman spectra for metal doped (3 at% in bulk; 5-9% in film) Ge$_2$Se$_3$

4.1.1.2   UV-Vis

The %Transmission and %Reflection was measured for every metal-cosputtered film. Analysis is underway for elucidating the transitions and energy band information (for future publication). Spectra are shown in Figures 35 and 36. Note that the cosputtered metal is listed in the graph with a subscript that corresponds to the power used for deposition. For example Cr$_{12}$ denotes that 12 W was used on the Cr target (***not*** to be confused with the chemical notation for which Cr$_{12}$ would denote 12 Cr atoms). The film thickness is approximately 300 Å in each case.
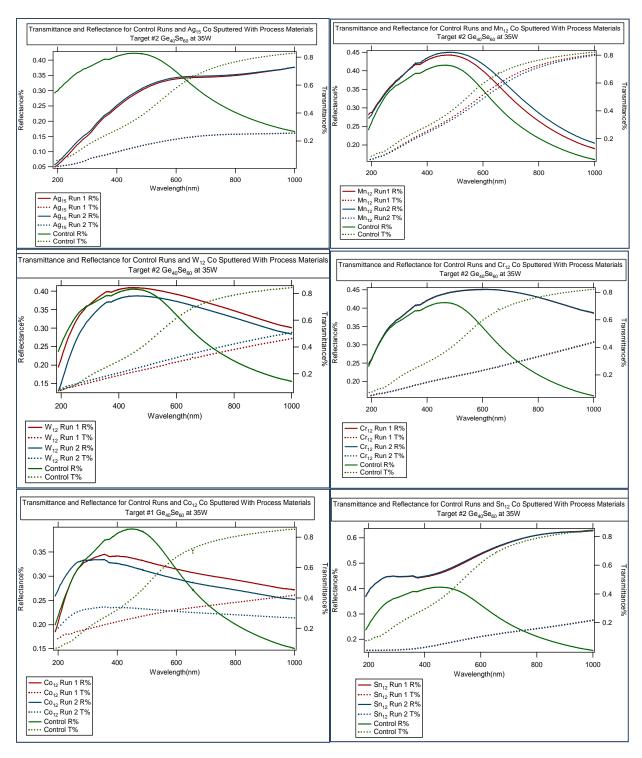
Figure 35. UV-Vis reflection and transmission spectra for cosputtered metal-Ge₂Se₃ films, 300 Å thick. Note the metal subscript corresponds to deposition target power
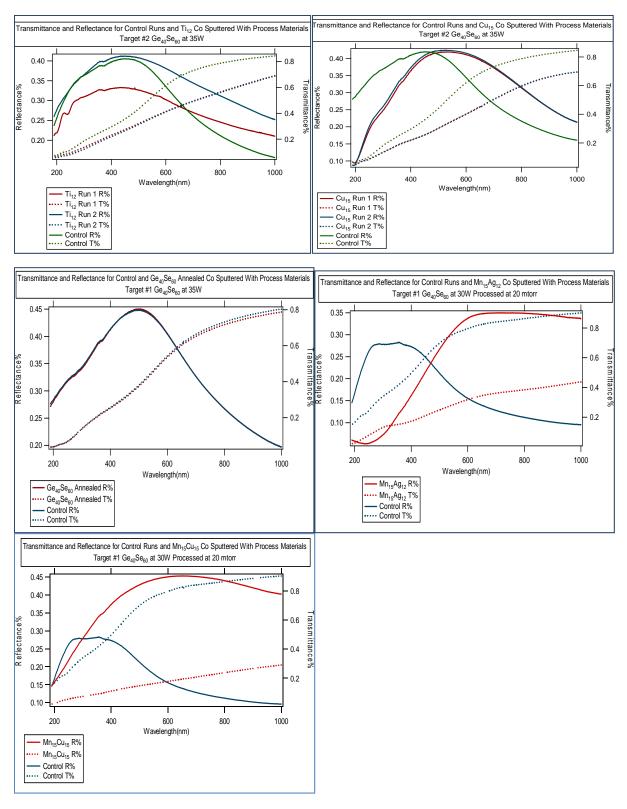
Figure 36. UV-Vis reflection and transmission spectra for cosputtered metal-Ge$_2$Se$_3$ films. Note the metal subscript corresponds to deposition target power

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4.1.1.3   EPR of Thin Films and Bulk

The EPR data for some bulk materials was previously collected in collaboration with AFOSR (FA9550-07-1-0546). Thin films, 300 Å, of all cosputtered materials have been deposited on strips from mylar sheets and packed into EPR tubes (20 strips), Figure 37. Initial measurements on the films did not show any detectable EPR signals. Trials with thicker films (1000-1500 Å) are recommended for the next test.

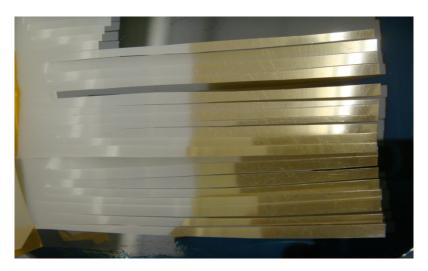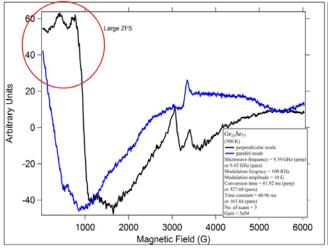**Figure 37. Mylar strips with thin films deposited on them. These strips are then stacked and placed in an EPR tube**

Additional bulk material measurements were performed for Se-rich (no Ge-Ge bonds) $Ge_{23}Se_{77}$ and metal doped $Ge_{23}Se_{77}$. These doped glasses differ significantly from each other and the $Ge_{40}Se_{60}$ glasses in their EPR spectra (to be published). It was found that the $Ge_{23}Se_{77}$ glass exhibited a ZFS at room temperature, Figure 38, shown for both the parallel and perpendicular cavity modes. Under illumination, the spectrum was unchanged in each mode.

EPR spectra were collected for a $Ge_{23}Se_{77}$ bulk sample at temperatures of 300 K and 77 K, Figures 38 and 39. Both samples were measured under dark or illuminated conditions. The perpendicular mode (standard) cavity magnetic field orientation was used for the measurements. The 77 K measurements were made by filling a finger dewar containing the EPR sample with liquid nitrogen.

Figure 38 shows parallel and perpendicular mode spectra for $Ge_{23}Se_{77}$ at T= 300 K. Note the large ZFS signal in both detection modes (circled). When the sample was illuminated at 300 K, there was no change in the EPR spectrum for either detection mode (not shown).

When the sample temperature was reduced to 77 K, the ZFS peak was greatly reduced, as shown in Figure 39. Figure 39 shows the perpendicular mode spectra of a light and dark sample. At this temperature, the sample displays a half-field transition (near 1500 G), typical of a transition for an S= 1 for two coupled electrons [31].   Under illumination, this peak decreases in amplitude and a peak near 3000 G grows in. Interestingly, the peak that is present at around 3000 G in the perpendicular mode spectrum at 300 K, is absent at 77 K, until illumination.
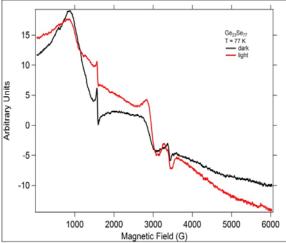
Figure 38. EPR spectra of Ge$_{23}$Se$_{77}$ bulk glass at T = 300 under parallel and perpendicular mode magnetic field within the microwave cavity

Figure 39. EPR spectra of Ge$_{23}$Se$_{77}$ at 77 K (illuminated and dark); perpendicular mode

4.1.1.4 Electrical Characterization

Figure 40 shows a wafer map of the regions tested during electrical characterization of the metal doped devices. DC sweeps and when possible CW tests were performed on each device fabricated with cosputtered materials. Unless otherwise indicated, all devices were fabricated with the IC stack structure, with the active Ge$_2$Se$_3$ layer replaced by the metal cosputtered layer.
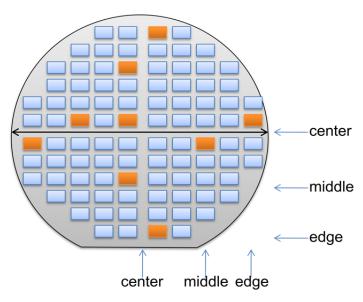
Figure 40. Wafer map for typical electrical characterization. Die in orange were tested with DC sweeps

Table 3. Devices fabricated and tested with co-sputtered metal-Ge$_2$Se$_3$ films

Wafer ID	Co-sputtered Metal with Ge$_2$Se$_3$	Contains SnSe Layer?	Electrical DC Characterization Summary
1207021-5	Cu	Yes	Devices appeared very low resistance
1202091-17	Ti	Yes	Many devices appeared to have a 'forming' erase for the first erase. This is unusual as ReRAM devices typically have a 'forming' write.
1202091-18	Ti	Yes	Same as Wafer 17 except more devices exhibiting the erase forming.
1202091-19	Ti	No	Without the SnSe layer, device function started to degrade after only a few cycles. All writes showed evidence for space-charge limited conduction.
1202091-20	Ti	No	Same as Wafer 19.
1202091-21	Ag	No	Devices very low resistance, no switching.
1202091-22	Co	No	Devices very low resistance, no switching
1202092_08	Cr	Yes	Higher On resistances (lower erase currents); many devices show a tendency to conduct current at negative potentials (as the potential is swept towards - 1V).
1202092_15	Sn	Yes	Inconsistent and poor, unreliable switching.
1202092-20	Co	Yes	Inconsistent switching.
1202092-23	Cr	No	Devices very low resistance, no switching

Typical IV curves for selected device types are provided in the following figures. A DC sweep of control IC stack is shown in Figure 28. IV curves for the metal doped devices are compared to the ideal IC stack curve for a comparison of operation.

Cu cosputtered device: The Cu-cosputtered devices had a low resistance initially. Despite high voltage and high current tests, the device could not be switched like a typical ion-conductor. The IV sweep observed with this device type is shown in Figure 41. Note that the compliance current for the 'write' sweep is 20 uA and for the erase it is 1 mA. The compliance is rapidly achieved in both cases due to the low resistance. This is indicative of a high concentration of Cu in the cosputtered film. Efforts to reduce the amount of cosputtered Cu were not successful.
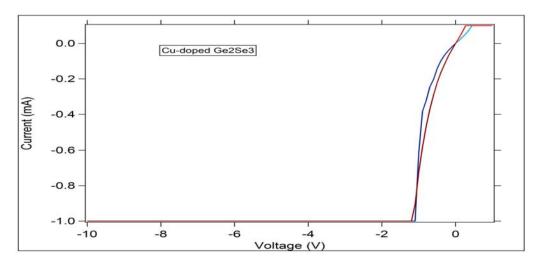
Figure 41. IV curve of Cu-cosputtered device. Note that the device did not switch resistance.

Ti cosputtered device: A typical Ti-cosputtered Ge_2Se_3 active layer in an IC stack configuration requires electroforming before the device will operate consistently as an IC memristor. This forming requirement can be seen in the IV curve shown in Figure 42. The first erase trace in the IV curve (labeled E1) shows that the device did not latch on the first write (W1) since there is no erase spike present in the E1 curve. However, after the erase sweep, the second (and subsequent) write latches the state of the device and the second erase does exhibit the erase spike. The 'forming' for this system is thus done through an erase sweep. Interestingly, a 'forming' erase sweep is also required for the devices fabricated with PECVD Ti doped Ge_2Se_3 films (see Section 4.1.8).
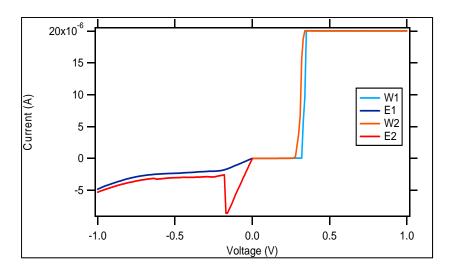
Figure 42. IV curve for a device with a Ti-cosputtered Ge₂Se₃

A modification of the Ti-cosputtered Ge_2Se_3 active layer device removed the SnSe layer from the IC stack configuration. In this case, the device did not appear to require the SnSe layer in order to switch. The 'write' threshold voltage is not sharp like it is in the IC stack case, however, the device does retain its state. The devices still appear to need the forming erase sweep, Figure 43.
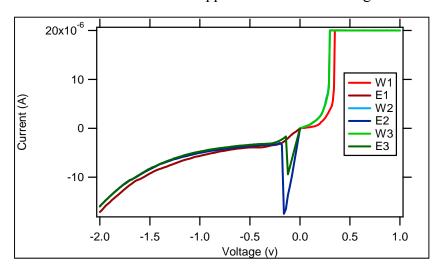
Figure 43. IV curve of a device containing a Ti-cosputtered Ge₂Se₃ active layer in an IC stack configuration without the SnSe layer

Cr cosputtered device: The IV curve of a device with a Cr-cosputtered Ge_2Se_3 active layer in an IC stack configuration is shown in Figure 44. The device functions as an ion-conductor, but the IV characteristics indicate a more conductive active layer (the large currents as the erase sweep increases towards – 1V).
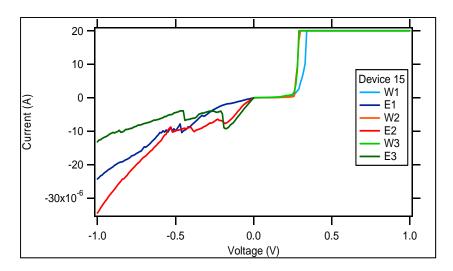
Figure 44. IV curve of a Cr-cosputtered Ge₂Se₃ device

<u>Sn cosputtered device:</u> The operation of the Sn cosputtered devices in an IC stack was mixed across the wafer between non-functional and exhibiting normal IC stack operation. An example of a device that appeared to operate like a normal IC stack is shown in Figure 45. Note that in this figure, a small read sweep from 0 to 20 mV was added to investigate data retention after a device was written.
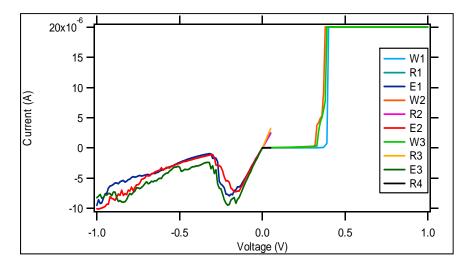
Figure 45. IV curve of a Sn-cosputtered Ge₂Se₃ device that appears operational

The majority of the devices tested did not switch, and appeared more like they were saturated with Sn metal (based on the conductivity). A typical set of IV curves showing this response is given in Figure 46.

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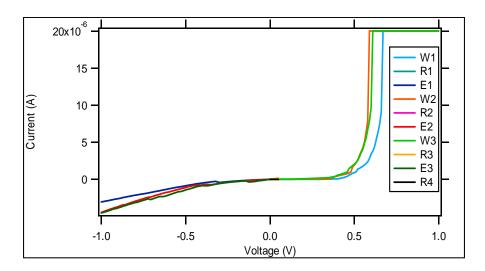
Figure 46. IV curve of Sn-cosputtered Ge₂Se₃ device that is non-functional

4.1.2   Cu vs Ag Devices

The electrical response of IC stack devices that use Ag or Cu were fabricated and tested as a function of temperature (DC sweep) and pulse width programming. Due to the unexpected and unusual behavior of the devices as a function of temperature, the measurements were repeated three times over the course of a year. With between three to ten devices measured in a given experiment, the trends and behaviors observed for each device type at each temperature were similar between experiment repeat trials.

Representative DC write IV curves for the Ag-based IC stack and the Cu-based IC stack for the temperature range of 5 to 350 K are provided in Figures 47 through 50.

The Ag-based IC stack devices breakdown at temperatures below 160 K. One representative device IV curve is shown at each temperature in Figure 47. The IV curves for the low temperature measurements (below 160 K) are misleading in that it appears that the devices switched at lower temperatures, but with a higher threshold voltage. In fact, the devices were actually damaged as evidenced by their erase sweeps, shown in Figure 49. The low temperature devices typically reach compliance current on the erase sweep and they do not reset, even for voltage sweeps out to -20 V (not shown).

In addition to the breakdown at temperatures below 160 K, the temperature region between 200 K and 150 K corresponds to a region where the device switches, but does not retain the written resistance. It is a region where the device does not get irreversibly damaged during operation, but it does not work properly either.
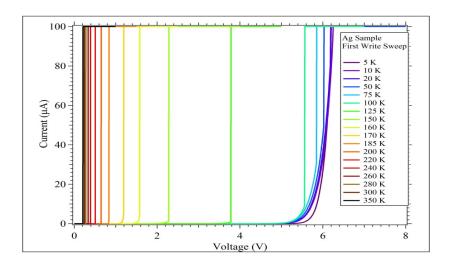
Figure 47. First write sweep as a function of temperature for Ag-based IC stack devices
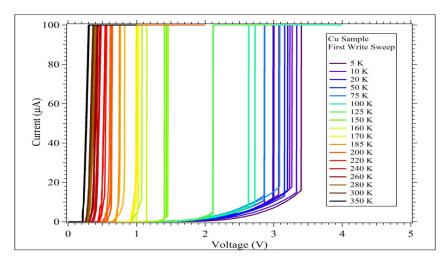
Figure 48. First write sweep as a function of temperature for Cu-based IC stack devices

One feature of interest in the erase sweeps is the shape of the erase IV curves around 150 K. At temperatures around 150 K, the Ag-based devices begin to show erratic erase responses, Figure 49. While this trace could mistakenly be taken for a noisy spectrum, every device tested at this temperature exhibited similar erase sweep IV curves and is thus a real phenomenon. This erratic response is at a temperature corresponding to the cusp of the irreversible device damage temperature and may be directly related to the permanent structural damage that occurs to the device when it is tested at these temperatures. Devices at temperatures greater than 200 K exhibited normal erase curves, as well as normal write curves, Figure 47.
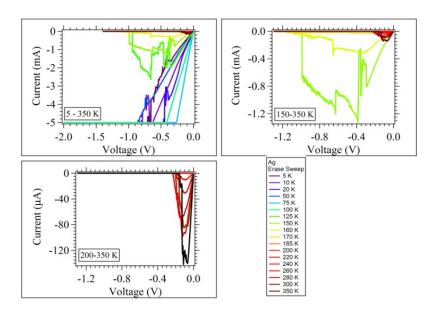
Figure 49. IV erase sweeps for Ag-based IC stack devices per temperature. Clockwise from upper left: all temperatures; 150 to 350 K; and 200 to 350 K

The Cu-based IC stack write IV curves, Figure 48, are much different than those for the Ag-based IC stack. There is more of an exponential shape to the IV curves as the temperature is reduced. The devices appear to switch between 2 to 3.5 V below 150 K. The erase sweeps, Figure 50, show that the low temperature writes are in fact real and the device is writing and retaining its state through the entire temperature range. At higher temperatures, the devices show an erase curve that resembles a smooth differential negative resistance curve, lower left plot of Figure 50.
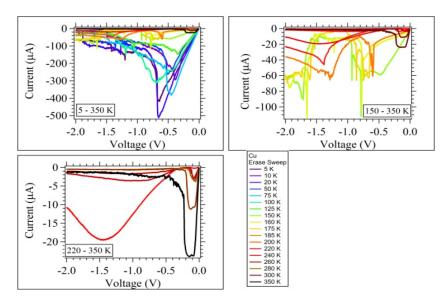

Figure 50. IV erase sweeps for Cu-based IC stack devices per temperature. Clockwise from upper left: all temperatures; 150 to 350 K; and 200 to 350 K

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The initial resistances of the Ag- and Cu-based IC stacks are similar except above 240 K, Figure 51. At this temperature, it appears that the Cu-based IC stack initial resistance gets small with an increase in temperature due to Cu diffusion into the Ge_2Se_3/SnSe layers.
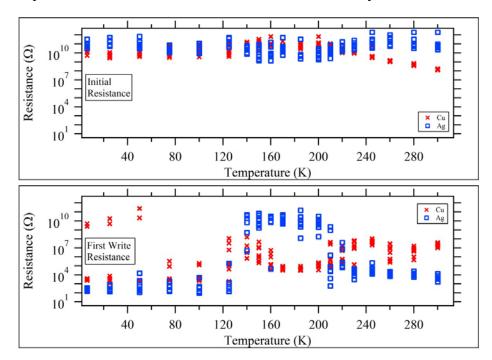
Figure 51. Initial and first write resistances for the Ag- and Cu-based IC stack devices as a function of temperature

The first write threshold voltage for each device is plotted versus temperature in Figure 52.
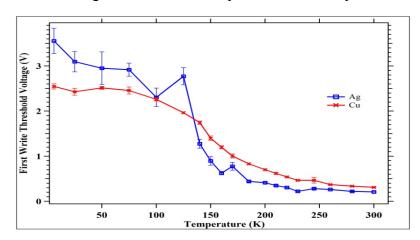
Figure 52. First write threshold voltages as a function of temperature for the Ag- and Cu-based IC stack devices

The pulsed switching characteristics of the Ag- and Cu-based devices differ significantly. The Ag-based devices switch easily in the ns timescale (the limits of the measuring tools available for these measurements), whereas the Cu-based devices switch much slower, preferring the μs timescale. The pulsed response of a typical Cu-based IC stack device (with a device size of 0.25

44

µm diameter) is shown in Figure 53. The voltage applied to the device is given by the black trace. The current (red trace) is measured simultaneously as the voltage pulse is applied (within a 10 ns resolution) and due to the way the system makes this measurement, it has a negative polarity (it is just measured in the opposite direction, through a separate electrode). The pulsing sequence is a read, erase, read, write, and read. The Erase pulse width is approximately 0.88 µs and the write pulse width is 3.33 µs. There is a visible delay between application of the write pulse and the device response (noted in Figure 53). Note the high voltage pulse amplitude required on the erase and write pulses to achieve a device response in this case.

In contrast, a typical pulsed switching response of an Ag-based IC stack device is shown in Figure 54. The write and erase pulse widths are each 100 ns. The overall time window on the Ag-based IC stack pulsed data graph is the same as the Cu-based device graph, Figure 53, yet there are 9 reads, 3 writes, and 3 erases within the time window for the Ag device. The Cu device has 3 reads, 1 write, and 1 erase within the window.

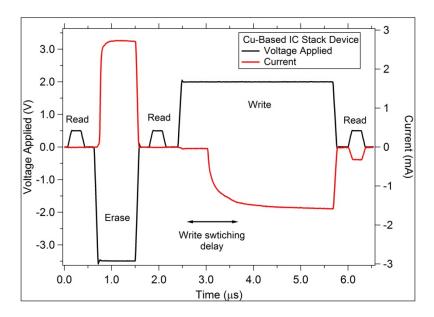**Figure 53. Pulsed programming response of a typical Cu-based IC stack device at room temperature**

In Figure 54, note that the erase pulse reduces the current through the device, increasing the resistance (compare the read pulse following the erase with the read pulse following the write). The write pulse increases the current through the device. This device is cycling between 600 and 4000 Ohms.
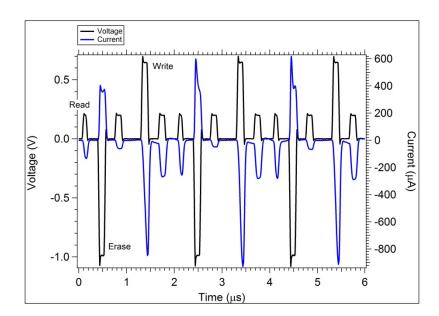
Figure 54. Pulsed programming response of a typical Ag-based IC stack device at room temperature.

The addition of a SnO layer above the SnSe layers in the Cu and Ag-based IC stack [45] produces a device that displays tunable variable resistance switching (manuscript in preparation).

4.1.3   S vs Se Devices

Four different device types were fabricated to compare the performance of a S-based versus a Se-based chalcogenide component in the IC-type stack. In this experiment, the IC stack was the basis for the chemical modification of the layers. The Ge_2Se_3 or the SnSe (or both) active layer was replaced with S-based layer. In one device type, the Ge_2Se_3 active layer was replaced with the other chalcogenide type, Te, through replacement with a GeTe layer.

Experiments performed on these devices include a comparison of device sizes, 0.13 um and 0.25 um, and on the compliance current used to program the device during a DC sweep. The DC sweep for this study was performed with an HP 4156A using a double sweep (meaning that a 0 to 1 V sweep actually sweeps from 0 to 1 V and reverses direction and does the measurement again from 1 to 0).

The experiment consisted of DC testing devices comprised of the following layers (read from bottom electrode to top):

- W/Ge_2Se_3/SnSe/Ag-GeSe/W (the control IC stack)
- W/ Ge_2Se_3/Sn**S**/Ag-GeSe/W
- W/**Ge₄₈S₅₂**/Sn**S**/Ag-GeSe/W
- W/Ge**Te**/SnSe/Ag-GeSe/W

The atoms denoted in red indicate key atomic changes in the IC stack structure. The $Ge_{48}S_{52}$ material was selected due to the presence of Ge-Ge homopolar bonds. These bonds were expected to be beneficial to device switching in the layered structure.

Five devices of each device size were measured at each compliance current. The compliance current range was 100 nA to 100 μA. The DC sweep consisted of a write (0 V to 1 V to 0 V) → erase (0 V to − 1V to 0 V) → write (0 V to 1 V to 0 V) sweep sequence.

The initial resistance (Ri) of a device was measured during the first write sweep, at 20 mV. This potential is below the write threshold of the devices and gives a measure of the resistance of an unperturbed (never previously switched) device. The first write resistance (R1) is measured at -20 mV on the +1 to 0 return path of the write sweep. The erased resistance (RE) is measured at 20 mV on the second write sweep. The second write resistance is measured at 20 mV on the +1 to 0 return path of the write sweep.

In the Ge_2Se_3 sample, the IC stack control is compared with the stack with SnS instead of SnSe. The results show very similar IV curves, as expected if the active glass layer is the same, and a source of Sn ions are available during switching (from SnS and SnSe, respectively). Interestingly, the initial resistance of the IC stack (Ge_2Se_3/SnSe) is lower than the case with SnS (~100 ΩW instead of 10^{10} Ω). However, the erase resistance of the IC stack returns to the range of values shared with SnS.

The measured resistances for each device are shown in Figures 55– 66. The average resistance of all five devices for each material set and device size is given if Figures 63-66. The error bars in Figures 63-66 correspond to one standard deviation.
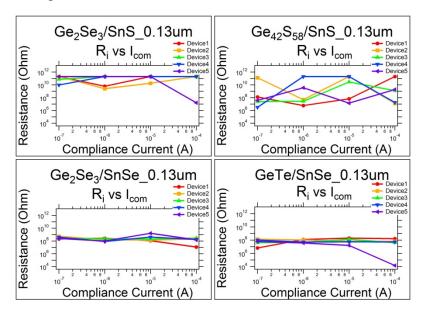
Figure 55. Initial resistance (Ri) for the 0.13 um Se vs S device DC Sweeps
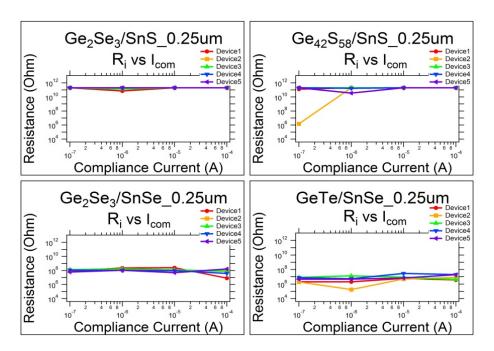
Figure 56. Initial resistance (Ri) for the 0.25 um Se vs S device DC Sweeps
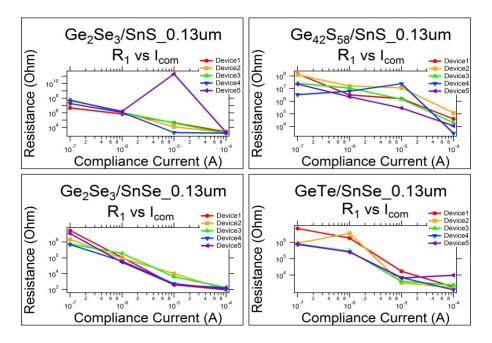
Figure 57. First write resistance (R1) for the 0.13 um Se vs S device DC Sweeps
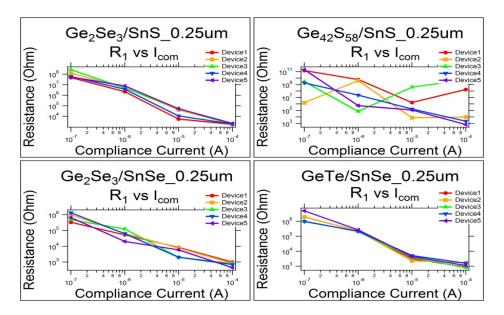
Figure 58. First write resistance (R1) for the 0.25 um Se vs S device DC Sweeps
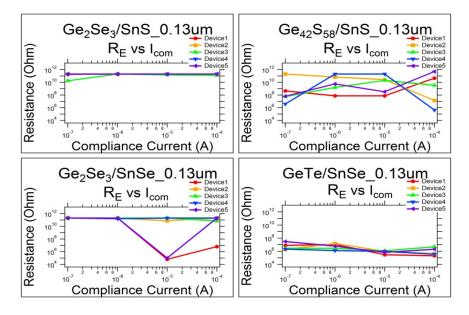
Figure 59. Erase resistance (RE) for the 0.13 um Se vs S device DC Sweeps
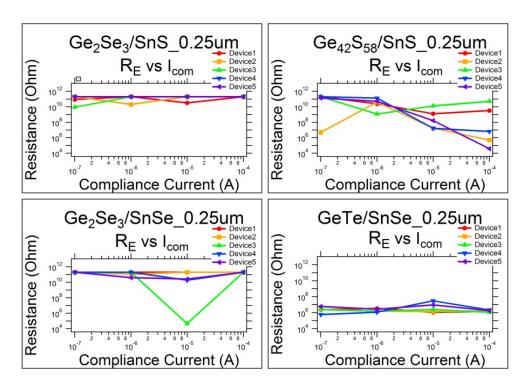
Figure 60. Erase resistance (RE) for the 0.25 um Se vs S device DC Sweeps
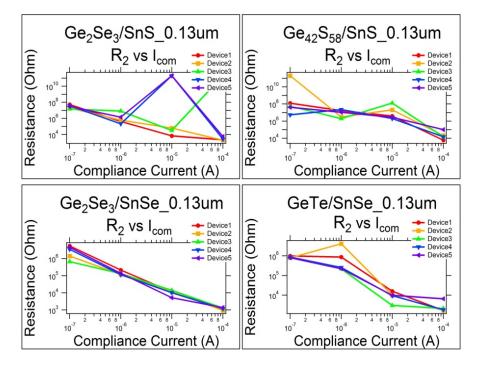
Figure 61. Second write resistance (R2) for the 0.13 um Se vs S device DC Sweeps

50
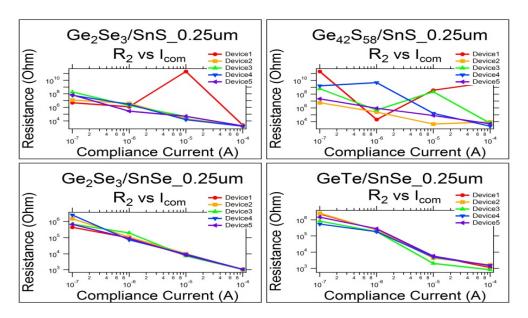
Figure 62. Second write resistance (R2) for the 0.25 um Se vs S device DC Sweeps
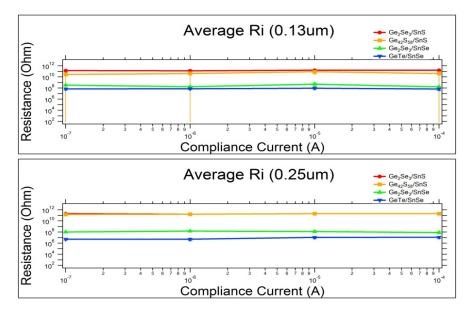
Figure 63. Average initial resistance for each device type and size. Error bars represent one standard deviation
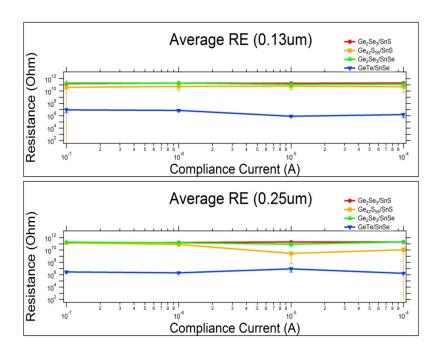
Figure 64. Average erased resistance for each device type and size. Error bars represent one standard deviation
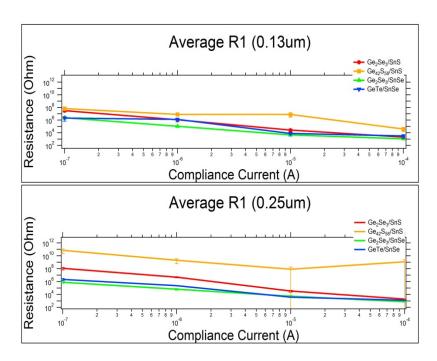
Figure 65. Average first write resistance for each device type and size. Error bars represent one standard deviation
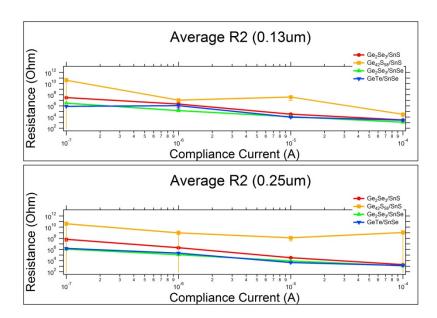
Figure 66. Average second write resistance for each device type and size. Error bars represent one standard deviation

The IV curves for the first write for the $Ge_{48}S_{52}/SnS$ and Ge_2Se_3/SnS samples are given in Figure 67. The S-based system has switching voltages that are very erratic, not only from device-to-device, but also within a single device. Notice the switching voltage threshold region circled in Figure 67 for the $Ge_{48}S_{52}/SnS$ sample. The Ge_2Se_3/SnS sample exhibits stable switching, like all IC stack configurations with Ge_2Se_3 as the active layer. In the case of the Ge_2Se_3/SnS, the Sn ions generated during the first write sweep enter the Ge_2Se_3 and assist in switching. It is unlikely that S is entering this glass. As evident from the erratic IV curves for the $Ge_{48}S_{52}/SnS$ sample, it is unlikely that Sn enters the S-based glass with the same positive impact that it does for the Se-based glass.
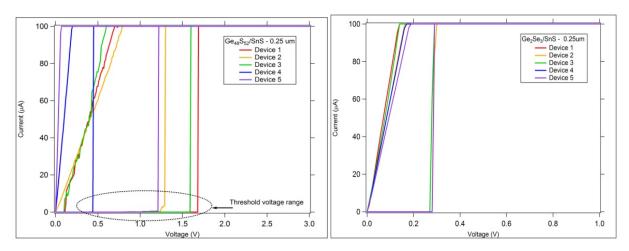
Figure 67. IV curve for the first write sweep of devices with the $Ge_{48}S_{52}/SnS$ stack (left) and the Ge_2Se_3/SnS stack (right).

The average write threshold voltage, which is the voltage where the devices starts to switch resistance is for each device type for the first write in Figure 68 and for the second write in Figure 69.
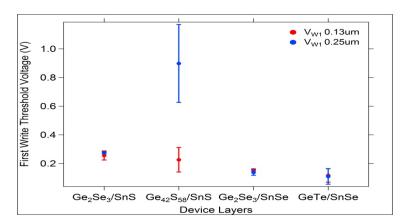
Figure 68. Average first write threshold voltage for each device type and size. Error bars represent one standard deviation
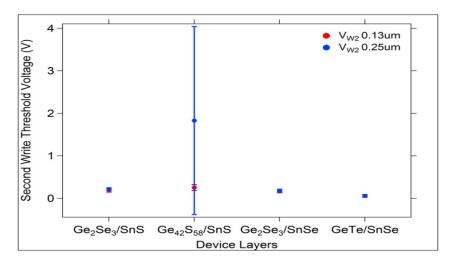
Figure 69.Average second write threshold voltage for each device type and size. Error bars represent one standard deviation

4.1.4   Differential Negative Resistance Testing

IC stack devices can exhibit negative differential resistance. This operating mode produces a continuously variable resistance device. Studies were conducting to determine the stability of the programming conditions on the device electrical parameters as a function of pulse conditions and temperature. This work is being prepared for publication.

4.1.5   Constant Current Source Testing

IC stack devices have the ability to be placed into an operating mode in which they behave as 'constant current sources', meaning that over a voltage range of approximately 0.1 to 0.9 V the current measured through the device is constant. This property was studied, and preliminary test

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circuits developed to explore the stability of this programmable constant current property in an actual application. This work is being prepared for publication.

4.1.6   Spike-Timing-Dependent-Plasticity Testing

IC stack devices operate well in a spike-timing-dependent-plasticity (STDP) experiment.   When a neural network uses spikes as the signals for operation, the learning usually follows a Spike STDP process. STDP uses the relative timing of the pre- relative to the post-synaptic spikes to both raise and lower the synapse weights. It can be seen as the Hebbian learning rule adapted to a spike-based network. IC stack devices have been shown to operate within the ns through the ms timescale. This work is being prepared for publication.

4.1.7   High Frequency Electrical Testing as a Function of Temperature

The frequency response from DC to 40 GHz of the IC stack was measured as a function of temperature. Six total devices were measured at each temperature (50 K, 150 K, 200 K, 300 K). The devices tested consisted of one device of each size (9 μm, 12 μm, 15 μm) and two different compliance currents (500 nA, 20 μA). The preliminary data for this study is provided here. This data represents the first trial at measuring the frequency response of the IC devices as a function of temperature. The data is preliminary and needs to be interpreted and further experiments done to verify the results.

Each device was programmed at room temperature. The high frequency measurements were performed at room temperature and the temperature reduced to the next temperature and the measurements were repeated. The excitation signal from the PNA was set at the lowest power setting in order to prevent device perturbation (-27 dBm) which corresponded to a signal amplitude of approximately 68 mV peak. A control measurement at room temperature verified that the device state was unperturbed when excited.

Table 4. Programmed device resistance for IC stack device frequency tests

	500nA			
	50 K	**150 K**	**200 K**	**300 K**
9μm	640.0E+3	659.9E+3	639.9E+3	360.0E+3
12μm	660.0E+3	659.9E+3	660.0E+3	500.0E+3
15μm	620.0E+3	640.0E+3	639.9E+3	340.0E+3
	20μA			
	50 K	**150 K**	**200 K**	**300 K**
9μm	16.0E+3	16.5E+3	16.5E+3	16.0E+3
12μm	16.0E+3	16.5E+3	16.0E+3	16.5E+3
15μm	16.0E+3	16.0E+3	27.0E+3	16.0E+3

The S21 parameter was measured and converted to impedance using:

$$Z = 50 * \frac{2*(1-S_{21})}{S_{21}} \tag{6}$$

The corresponding magnitude and phase plots for each temperature follow, Figures 70-78.
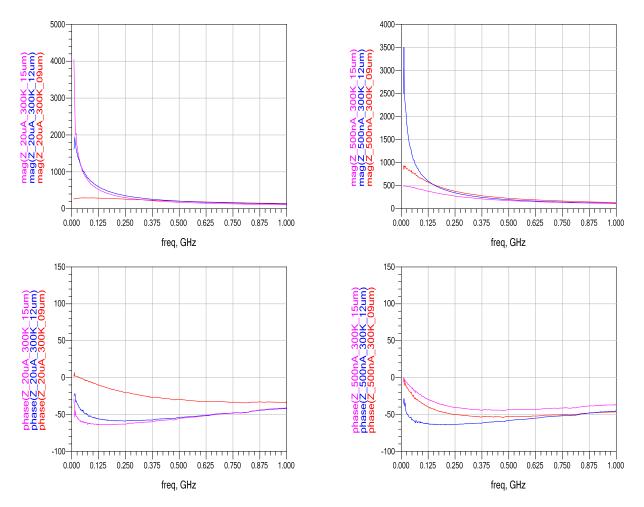
Figure 70. The magnitude (top) and phase (bottom) plots for each device size. (left column) 20 uA compliance current; (right) 500 nA compliance. T=300 K
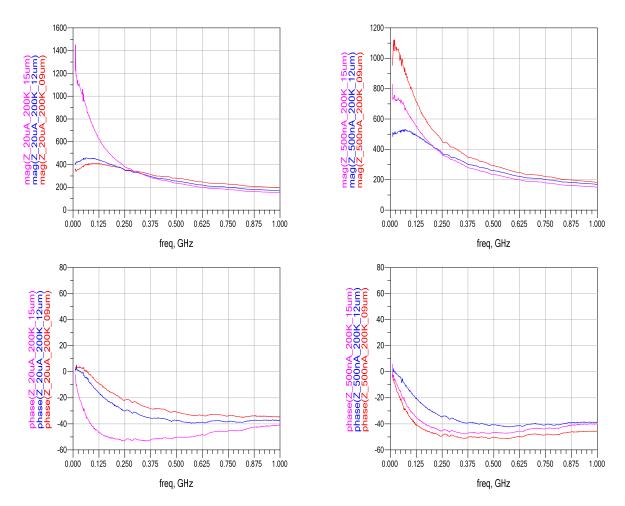
Figure 71. The magnitude (top) and phase (bottom) plots for each device size. (left column) 20 uA compliance current; (right) 500 nA compliance. T=200 K
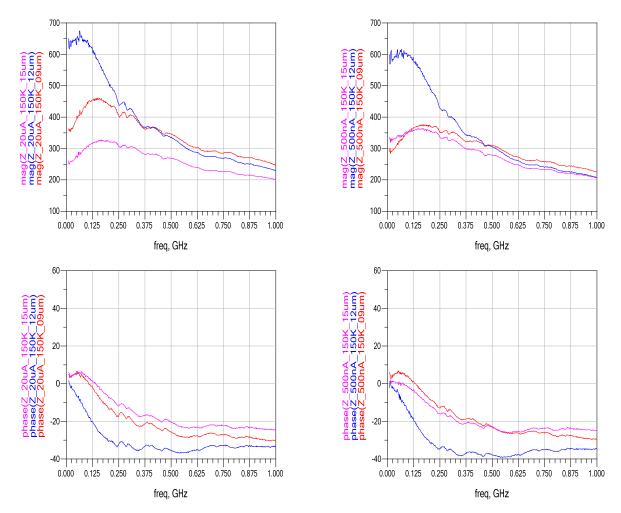
Figure 72. The magnitude (top) and phase (bottom) plots for each device size. (left column) 20 uA compliance current; (right) 500 nA compliance. T=150 K
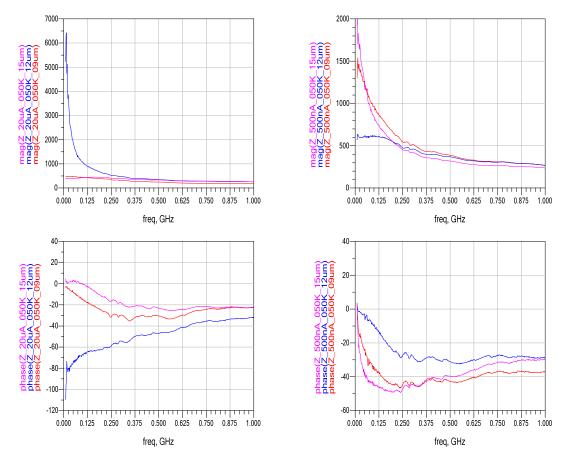
Figure 73. The magnitude (top) and phase (bottom) plots for each device size. (left column) 20 uA compliance current; (right) 500 nA compliance. T=50 K

The data are grouped by compliance current and device size, Figures 74 and 75, to help identify differences between the temperature responses more easily. It should be stressed that these measurements are preliminary and serve to develop the experimental protocol needed for this type of measurement.
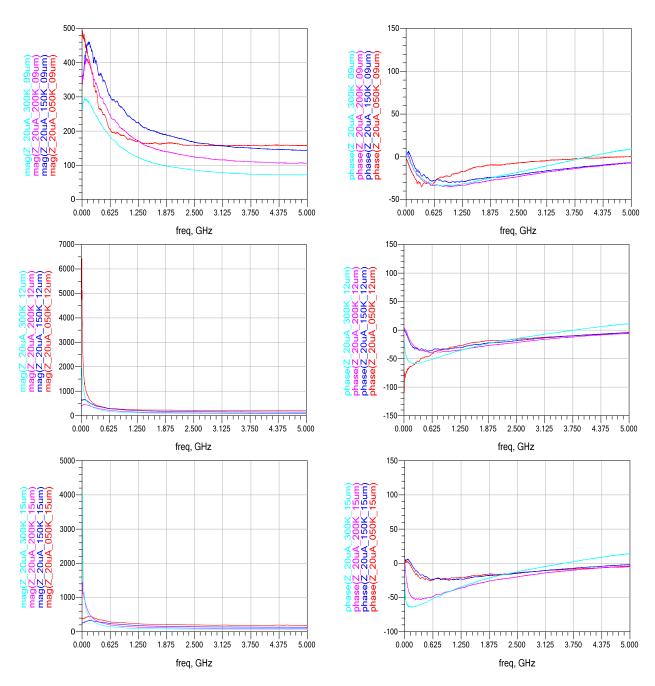
Figure 74. A comparison of all 20 uA programmed magnitude and phase device data, at each temperature. (top) 9 um device; (mid) 12 um; (bottom) 15 um.
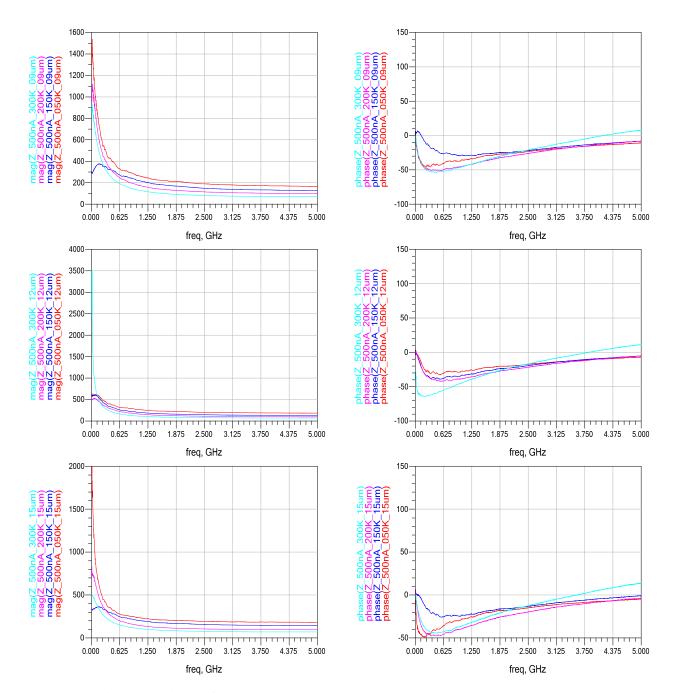
Figure 75. A comparison of all 500 nA programmed magnitude and phase device data, at each temperature. (top) 9 um device; (mid) 12 um; (bottom) 15 um.

4.1.8   PECVD Deposition of Ti-doped Ge_xSe_y Films

A collaboration with Prof. Rene Rodriguez, Idaho State University, was initiated in order to develop a PECVD metal-Ge_2Se_3 film deposition process [46-51]. After investigating blanket films for stoichiometries, an optimum set of film deposition conditions was determined and the film was deposited on wafers fabricated at Boise State that were processed to the bottom

electrode via opening level. Once the films were deposited at Idaho State University, the wafers were returned to Boise State for completed processing. The device structure is shown in Figure 76. The top electrode was Ag instead of W.
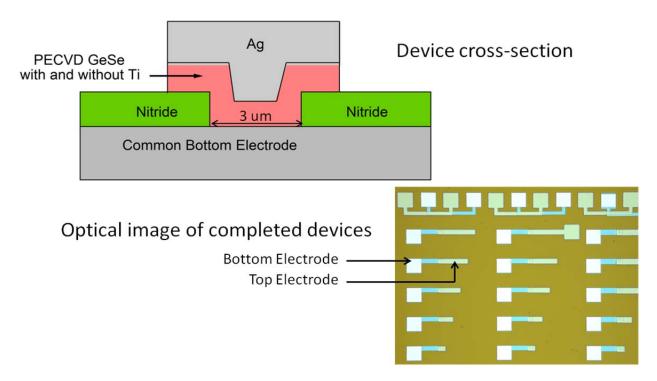
Figure 76. The device structure used for the PECVD film tests (top) and an optical image of a completed wafer

Electrical characterization consisted of DC sweeps. An IV curve of a device fabricated with only a PECVD Ge_2Se_3 layer and an Ag top electrode is shown in Figure 77. It is clear from this curve that the device does not switch in the case of Ge_2Se_3/Ag when no SnSe layer is included. This result is also seen in sputtered and evaporated Ge_2Se_3/Ag devices; without the SnSe layer, Ag penetrates the Ge_2Se_3 layer and eliminates switching action. The region around -1 to 1 V is expanded and shown in Figure 78. From this figure it is clear that the applied potential does not alter the device state.

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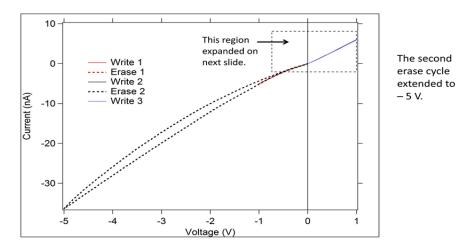
Figure 77. IV curve of Ge$_2$Se$_3$/Ag. No Ti doping
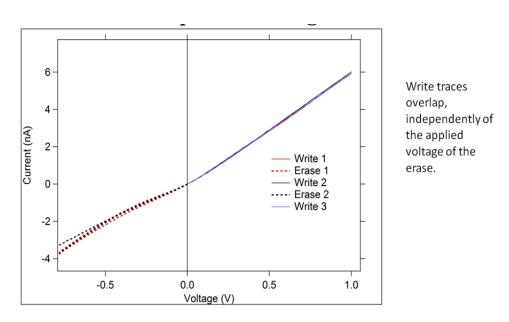
Figure 78. The expanded region of the IV curve in the Figure 77

In the case of Ti doping, the device exhibits bipolar switching. This switching is volatile (see Write 1 and Erase 1 in Figure 79) until the device is 'conditioned' with a large negative voltage sweep. In Figure 79, this conditioning sweep occurs during Erase 2. All write sweeps after this erase appear normal.

An example of a conditioning sweep is shown in Figure 80. During the conditioning sweep, the device appears to hit the compliance current of 1 mA twice, around -3.8 and -4.5 V. After the device has done this, it begins to write and erase similarly to an IC stack device.

A comparison of the Ti-doped device IV characteristics before and after the condition sweep is shown in Figure 81. While the pre-conditioning sweep looks like it has a write threshold voltage

of approximately 0.7 V, it actually does not retain a changed resistance state and is considered volatile. After conditioning, the device retains its state and is non-volatile.

The write 'repeat' traces were applied after the given 'write' in order to measure how well the device retained its written state.
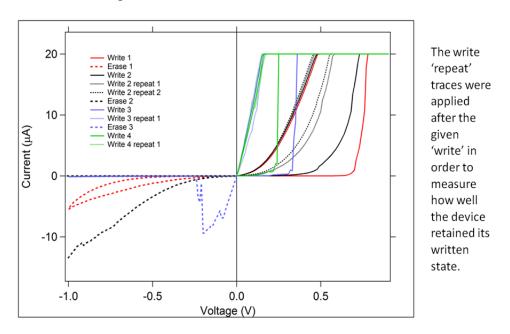
Figure 79. IV curve of a device with PECVD Ti-Ge$_2$Se$_3$

Sweep to – 5 V conditions the device.
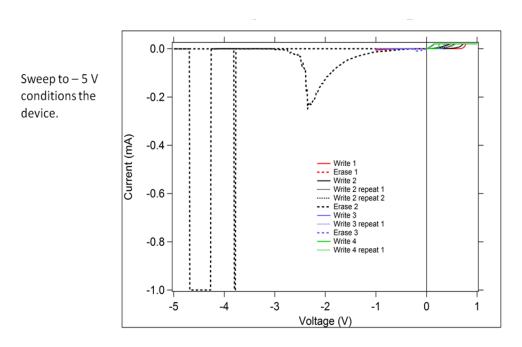
Figure 80. IV curve of the required negative potential conditioning sweep used to 'form' the device
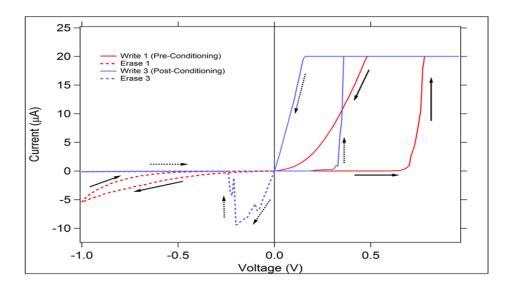
Figure 81. IV curve of Ti-doped PECVD device pre and post conditioning to form the channel. Before channel formation, the device was volatile

In summary, the PECVD deposited Ge_2Se_3 wafers with Ag (no SnSe) layer, do not exhibit bipolar switching. This is also true for sputtered and evaporated Ge_2Se_3 films. Interestingly, addition of Ti to the Ge_2Se_3 film during PECVD deposition results in a device capable of bipolar switching. The switching is inconsistent however, and does require a very large forming voltage (in the negative potential range).

These results are consistent with the cosputtered Ti Ge_2Se_3 devices. Thus, the PECVD method provides a viable way to deposit metal-doped Ge_2Se_3 films [46-51].

4.1.9   Device Fabrication on 300 mm Wafers
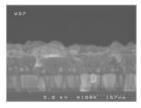
Boise State and Micron Technology entered into a collaboration to process IC stack memristor materials on their 300 mm test part. Boise State received two 300 mm wafers from Micron which had all of the underlying electrodes and circuitry already completed. Boise state deposited the IC stack on the wafers using thermal evaporation of the films since the evaporator is the only film deposition tool at Boise State capable of processing 300 mm wafers, and returned them to Micron for top electrode deposition, photolithography and etching.

Micron noted that they had some issues processing the wafers that may have damaged them. Upon return to Boise State, the wafers were visibly damaged and the devices were non-functional. The visible wafer damage is shown in Figure 82. This experiment will be attempted again at a future time.

Industry Collaboration on 300 mm Wafers

Micron 4Mb Part, ion conducting devices
Lot 8085243.043, wafers 08 and 09
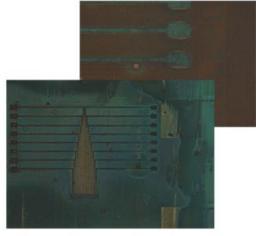
- Film Stack Deposited on BEC:
  - Wafer 08: 300Å Ge_2Se_3/500Å SnSe/300Å Ge_2Se_3/1000Å Ag/100Å Ge_2Se_3
  - Wafer 09: 300Å Ge_2Se_3/500Å SnSe/150Å Ge_2Se_3/500Å Ag/100Å Ge_2Se_3
  - Processing completed at Micron Technology
- Devices appear to be damaged
  - No functioning devices found

Wafer ready for evaporation

SEM crossection image of 5 layer ion conducting stack plus tungsten top electrode deposit

Photos of completed wafer 09

Figure 82. 300 mm wafers processed at Micron with visible damage.

4.1.10 BEOL Development for ASU IC Test Chip

ASU delivered to Boise State five die fabricated at a foundry, and ready for memristor BEOL processing with passivation openings to metal pads which would serve as the bottom electrode. The BEOL mask levels, process flow, and fabrication were completed at Boise State. The fabrication process used the BEOL process for memristor device integration with CMOS that has previously been established [42].

The mask images for the BEOL process developed at Boise State follow, Figures 83-91.
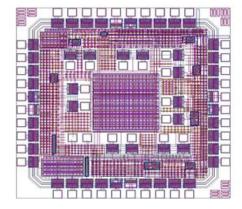
Figure 83. Incoming die layout. The BEOL masks must align to this existing die
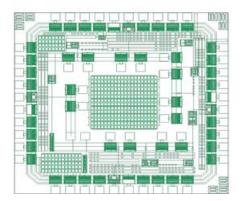
Figure 84. Incoming die top most metal layer. This is the memristor bottom electrode
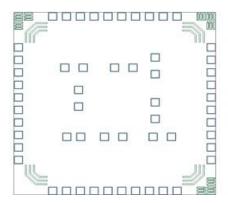
Figure 85. Incoming die passivation openings and alignment marks
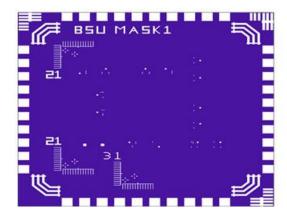
Figure 86. BEOL mask 1, opens metal and device vias
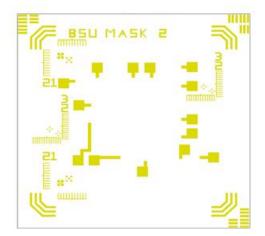
Figure 87. BEOL mask 2, bottom electrode bond pad definition
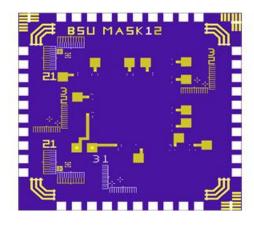
Figure 88. BEOL overlay of mask 1 and 2

Figure 89. BEOL mask 3 opening bottom electrode contact and via

Figure 90. BEOL mask 4, top electrode definition
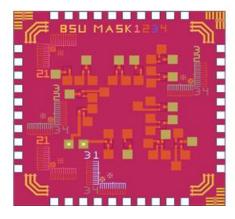
Figure 91. Overlay of all four BEOL mask layers

Table 5 lists the die and wafers processed with the BEOL mask set designed for ASU's test chip. A control wafer (labeled 'Test Wafer') was processed along with the die in order to verify the process in the event that the die was non-functional. The control wafer, which was processed without the die, but with the entire mask set, showed that the devices functioned as expected for an IC stack memristor, Figure 92.

Table 5. Summary of wafers and die (ASU Chips) processed

Item	Substrate Material is Metal	T.E. to other T.E. short	T.E. to B.E. short	Edge Pads short
Unprocessed ASU Chip	No	N/A	N/A	No
ASU Chip 2	No	Yes	Yes	No
ASU Chip 4	Yes	Yes	Yes	No
Test Wafer 4	Yes	No	No	N/A
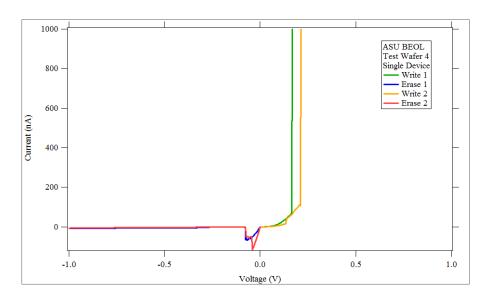
Figure 92. IV curve of control wafer processed with the BEOL mask design for ASU's test chip. The memristor fabrication process using the BEOL mask set was successful

Both of the processed chips exhibited shorting between the top and bottom electrodes. While the exact cause is unknown, the high aspect ratios of some of the features on the die may have caused poor film coverage during BEOL processing, resulting in metal shorting, Figure 93.

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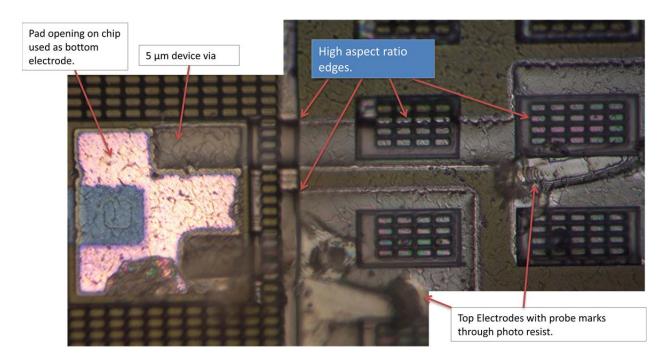
Figure 93. Image of a die post BEOL processing

After attempting to fabricate on three die, this effort was abandoned.

4.1.11 Theoretical Calculations

Dr. Arthur Edwards performed theoretical calculations on Ge_2Se_3. The results predicted that there was single and paired electron self-trapping in Ge_2Se_3, with the paired electron self-trapping preferred energetically [43]. It was found that two electrons prefer to trap around the same Ge-Ge dimer, thus rupturing a neighboring Ge-Se bond. The results showed that single electron trapping was not present around the Ge-Ge pair.

This work also estimated 'freeze-in' temperatures of 81 K and 186 K, which may allow for observation of hyperfine coupling associated with single self-trapped electrons in Ge_2Se_3. A conclusion from this work was that there is an important role for localized, self-trapped electrons in metal incorporation into the Ge_2Se_3 material. There is one stable isotope with a nuclear spin that is nonzero, ^{73}Ge (I=9/2), and an abundance of approximately 7%. If hyperfine coupling were observed between one electron and Ge, one could expect to see 10 hyperfine coupling lines in the EPR spectrum. Preliminary EPR data collected on the Ge_2Se_3 bulk before this prediction was made shows a fairly noisy hyperfine coupling interaction around g2 appearing in the 77 K spectrum, Figure 94. It is hard to say if there are 10 lines in this spectrum; better signal to noise ratio is needed. It is recommended that a study of the Ge_2Se_3 material be completed to verify the theoretical finds, given the promising initial EPR results.
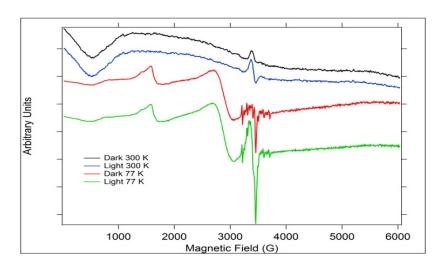
Figure 94. Ge₂Se₃ EPR spectra at 300 and 77 K under dark and light conditions

Further density functional theory calculations show that Ag and Sn will autoionize upon entering the Ge_2Se_3, becoming Ag^+ and Sn^{2+} [44]. The freed electrons self-trap at the lowest energy site. Both Ag and Sn can substitute for Ge. Calculations show that Sn can substantially alter the incorporation of Ag into the Ge_2Se_3 network. This is a result that is supported by experiment, where it has been shown that devices fabricated with Ag above Ge_2Se_3 and no SnSe layer will not function consistently or with any cycling endurance. This theoretical prediction also supports the work investigating the metal cosputtered Ge_2Se_3 films and the device electrical response of these devices.

4.2 Atomic or Molecular Memory Based on ZFS

Samples of PCMO films, deposited at Boise State (using RF sputtering) were analyzed and characterized with EPR spectroscopy, XPS (in collaboration with Micron Technology), XRD, Raman, and SEM. Films were then deposited on a blanket electrode and tested electrically for both the DC conductivity and microwave absorption. No microwave absorption could be detected in the sample at zero magnetic field, with or without light, with applied voltage, without applied voltage, and with/without Ag added to the top of the film (for Ag movement).

The device stack materials layers are shown in Figure 95. PCMO films for most analyses were deposited directly on nitride.
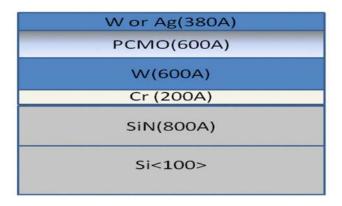
Figure 95. PCMO device testing material stack. Films for some analysis (such as SEM) placed PCMO on nitride directly

XPS data show a small amount of Mn^{2+} in the film, with Mn^{3+} being the dominant Mn species, Figure 96. XRD data shows that the PCMO film is amorphous as deposited, Figure 97(a). EPR spectra was collected in the both parallel and perpendicular mode due to the significant presence of Mn^{3+} in the PCMO. Figure 97(b) shows the EPR spectra for the room temperature parallel mode PCMO film, blank EPR tube, and mylar sheet (the substrate for the thin film deposition).
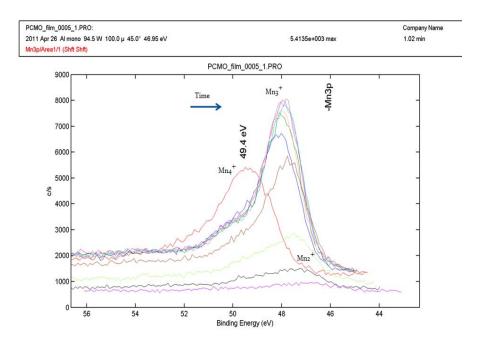
Figure 96. XPS spectra binding energy of Mn in PCMO film
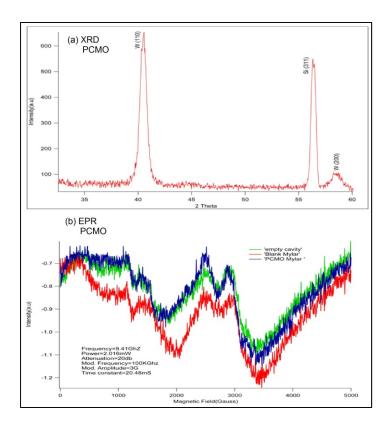
Figure 97. XRD (a) and EPR (b) of PCMO thin films. The EPR spectra was collected in the parallel mode because of the predominant Mn^{3+} species in PCMO

4.3   Phase-Change Multi-State Memory

4.3.1   RIT Collaboration

In collaboration with Prof. Santosh Kurinec, time resolved x-ray diffraction measurements were used to investigate Sn migration into Ge$_2$Se$_3$ and GeTe from the layered structure films [39, 40]. Sn migration was observed explicitly in the Ge$_2$Se$_3$/SnTe structure and determined to be due to a separation of an SnSe phase. The Ge$_2$Se$_3$ thin film was found to crystallize at a lower temperature than predicted (300 °C instead of 350 °C) [41]. This work showed that inclusion of Sn may offer a way to tailor phase transitions in Ge-chalcogenide thin films for phase change memory applications.

4.3.2   EXAFS Collaboration

The collection of this data was in partial collaboration with an AFOSR grant (FA9550-07-1-0546) and was also reported in the final report for that grant. To summarize, samples were prepared with the 150 x 150 array masks. The phase change material, GST, was deposited by Prof. Craig Taylor's group at Colo. School of Mines and given back to Boise State for continued processing. This included the development of a planarization process so that GST was localized in a via instead of as a blanket film across the wafer. Some devices were switched to a low resistance state, while others remained in a high resistance state. EXAFS measurements were performed to try and observe structural differences between the two states. The EXAFS results

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were identical for all samples tested, and appeared to be dominated by GeO_x. Without the ability to planarize the GST without exposure to oxygen, this effort was abandoned.

4.3.3 Electrical characterization of layered devices

Figure 98 shows IV curves of the well-studied GST ($Ge_2Sb_2Te_5$) material compared to a layered GST/SnTe device in which a clear improvement in the programming current requirements for the layered structure compared to the GST-only structure are observed (compare the current measured at the 'snapback' voltage). This may be due to the improved electrical contact between the chalcogenide material and the electrode, or it could be due to Sn incorporation into the GST material during operation which subsequently optimizes the alloy properties for phase change operation.

As shown in Figure 98 (right graph), altering the metal in the metal-chalcogenide layer allows the threshold voltage of the memory to be changed. In the case shown, devices using ZnTe and SnTe were fabricated and tested. The device with the Zn-Chalcogenide layer results in a threshold voltage more than twice as high as the Sn-Chalcogenide device. This layering technique thus provides a method of tuning materials to specific application needs. The GeTe/ZnTe stack structure also exhibits at least two 'snap-back' regions. The DSC data for a Zn doped Ge_2Se_3 glass showed three crystallization temperatures. Interestingly, the IV curves for the stacked device may indicate that multiple crystalline forms may exist.
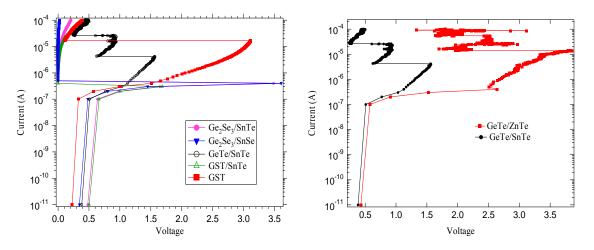
Figure 98. IV curves for phase-change memory stack structures

4.3.4 Micron Technology 300 mm Wafer Tests

Three wafers from Micron lot 8118483.013 were processed on their XP50 49C flow through the 49 contact TiN CMP and then given to Boise State University for the deposition of chalcogenide materials by evaporation. This process flow used two device structure types: planar and pillar structures. The planar structure has a flat bottom electrode contact, Figure 99. The pillar structure (also called the confined structure) is the via structure normally used for device fabrication at BSU, Figure 100.
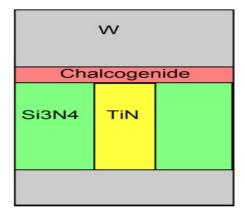
Figure 99. Planar structure. Bottom electrode contact (TiN) is 40 nm in diameter

The wafers were processed at Boise State University according to the following splits:

- Wafer ID 8483-03 - SnTe 500A on top of 300A GeTe
- Wafer ID 8483-04 - SnTe 400A on top of 275A GeTe
- Wafer ID 8483-05 - GeTe only, 300A

After film deposition at Boise State, and returning the wafers to Micron, the wafers were topped with W top electrode and processed on the 3-reticle flow (top electrode patterning and dry etch) and then sent through Micron's inline param for initial electrical measurement.

The test condition for each wafer is to force 200 mV on top electrode and sense current. This is to determine if die are 'live'. In total for each wafer:

- 46 sites (all odd die) are tested
- 92 devices per each site for a total of 4232
- 27 planar cells for 1242 possible data points
- 23 pillar cells for 1058 possible data points

The test results from both the planar and pillar structures show that the die are live and warrant further testing.
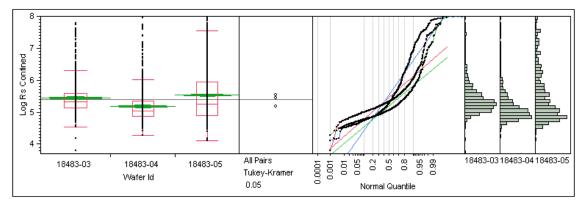
Figure 100. Inline probe data for planar cell structure devices with 40 nm diameter

The probing statistics for the planar cells are shown in Table 6.

Table 6. Statistical analysis for the 300 mm wafer planar structure data

	Means for Oneway Anova				# of	# of Sites	%
Wafer ID	Mean	Std Error	Lower 95%	Upper 95%	Live Sites	Tested	Yield
8483-03	5.44	0.02	5.40	5.48	978	1242	78.74
8483-04	5.18	0.02	5.14	5.22	907	1242	73.03
8483-05	5.53	0.02	5.49	5.58	890	1242	71.66

Std Error uses a pooled estimate of error variance
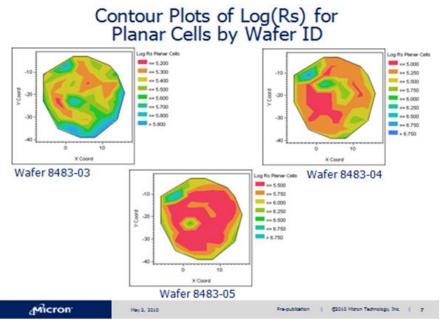
Figure 101. Wafer maps showing resistance for each wafer of planar structure devices

For the pillar cells, Figure 102:
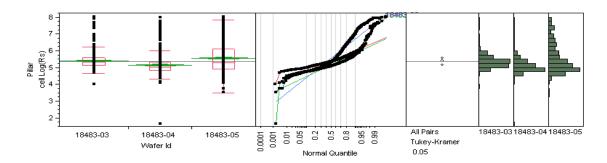
Figure 102. Micron inline testing data for the pillar cell structure devices

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Table 7. Statistical analysis for the 300 mm wafer pillar cell structure data

	Means for Oneway Anova				# of	# of Sites	%
Wafer ID	Mean	Std Error	Lower 95%	Upper 95%	Live Sites	Tested	Yield
8483-03	5.40	0.03	5.35	5.45	653	1058	61.72
8483-04	5.15	0.03	5.10	5.21	597	1058	56.43
8483-05	5.56	0.03	5.51	5.61	602	1058	56.90

Std Error uses a pooled estimate of error variance
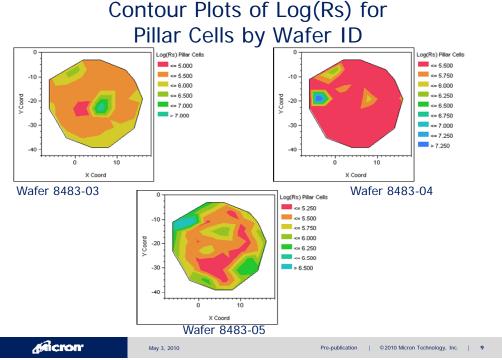
Figure 103. Wafer maps showing resistance for each wafer of pillar structure devices

Initial param data shows that the cells are "live." Micron's conclusion was that the wafers warrant additional electrical measurement and analysis.

5 CONCLUSION

Much of the data generated during this research is preserved for publication, and thus not included in this report. This includes electrical data for devices exhibiting variable resistance programmability as well as analysis of device conduction mechanisms through the use of temperature dependence conduction studies.

During the course of this research, the capabilities to fabricate and electrically test devices were developed at Boise State. This was a large effort, which required a significant investment in time and capital that would not have been accomplished without the grant funding. During this time, basic research was taking place on the three device types discussed in this report. A clear winner in terms of ease of fabrication and superior performance was the ion-conducting device type.

The ion-conducting devices showed the most flexibility in terms of achieving a reconfigurable operating mode. Several device types were fabricated and tested under both DC, and pulsed conditions. The type of metal dopant significantly alters the electrical and thermal properties of the device. Devices were developed and tested that operate continuously at > 140 °C. Devices could be programmed incrementally in both the write and erase directions (higher to lower resistance continuously). Devices could operate with potentials below 0.6 V and pulse widths less than 100 ns. Device resistance ranges could be adjusted to operate in the higher range, 100 kOhm and greater.

It should be stressed that the DC sweeps are useful for determining whether a device fabrication process was successful, but not in understanding the device's operating characteristics. To understand how the devices will operate, test conditions need to be applied that are similar to how the device will be used in application. Typically, the ion-conducting device operation depends significantly on the history of its use. If a device has previously been stressed, it will operate differently than if it has never been stressed. It is recommended that to futher study devices of this nature, they be targeted for a specific application and tested in circuits related to that application. The actual device operation in the circuit (power, speed, endurance) can best be determined under the specific conditions. Following prototype testing, the next step is integrating and testing the devices using a BEOL process on an underlying CMOS circuit. The steps from a prototype (with memristor chips) to an integrated IC with memristors deposited as a BEOL step can be a large challenge. With the processes developed at Boise State under the work supported by this grant, BEOL integration of memristors on ICs is possible.

It is recommended that further work be performed in the area of electron paramagnetic resonance spectroscopy to further the theoretical understanding of how the basic Ge_xSe_y glass system interacts with metals and oxygen. The work on thin film characterization needs further study with the direction being that thicker films must be deposited to increase the signal to noise ratio of the sample in the EPR cavity. Additionally, the EPR spectra of $Ge_{40}Se_{60}$ needs to be better studied as a function of temperature. This is work that could validate or at least help with the theoretical simulations concerning electron pairing and energy.

The ZFS devices will require much more theoretical analysis and basic research before this concept can be implemented. Basic questions are still unanswered. Specifically, determination of whether or not the spin concentration will ever be high enough to enable high density arrays. If this research area is ever pursued, methods of signal detection need to be further explored.

The phase change memory devices have inherently higher power requirements than the ion-conducting devices. The layered structures appear to scale well to at least 40 nm device sizes. Initial tests on Micron's 300 mm wafers show promising electrical yield and warrant further testing. Similar wafers with IC-stacks did not process properly through Micron's processing steps post device material deposition. This experiment should be performed again.

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LIST OF SYMBOLS, ABBREVIATIONS, AND ACRONYMNS

Alq3	tri(8-hydroxyquinolinato)aluminum
BEOL	Back-End-Of-Line
CuPC	copper pthalocyanine
CW	Continuous Wave
DFT	Density Functional Theory
DSC	Differential Scanning Calorimetry
EPR	Electron Paramagnetic Resonance
EXAFS	Extended X-Ray Absorption Fine Structure
FPGA	Field-Programmable Gate Array
ICP-MS	Inductively Coupled Plasma – Mass Spectroscopy
IML	Idaho Microfabrication Laboratory
MRAM	Magnetic Random Access Memory
NMR	Nuclear Magnetic Resonance
NVM	Non-Volatile Memory
PCMO	$Pr_{0.7}Ca_{0.3}MnO_3$
PECVD	Plasma Enhanced Chemical Vapor Deposition
RSU	Remote-sense and Switch Units
SMU	Semiconductor Measurement Units
TiOPC	titanyl pthalocyanine
WGFMU	Waveform Generator/Fast Measurement Unit
XANES	X-Ray Absorption Near Edge Structure
XPS	X-Ray Photoelectron Spectroscopy
XRD	X-Ray Diffraction
ZFS	Zero-Field Splitting

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