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NANOSCALE SEMICONDUCTOR ELECTRONICS

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14. ABSTRACT
The top-down fabrication of a semiconductor on insulator (SOI) in-plane GaAs nanowire (NW) metal-oxide-semiconductor field effect transistor fabricated by ion-beam direct etching has been demonstrated. For the gate oxide, a ~15 nm-thick liquid-phase chemically-enhanced oxide has been employed. In-plane NWs with ~200 nm channel width are reported. With the NW channel having cross section ~70 nm × 220 nm and the length 2 μm, the device has V_T ~0.2 V and peak g_m ~24 μS with SS ~ 110-150 mV/dec, which are similar to results achieved with bottom-up GaAs NW devices. Radiation studies with x-ray sources do not show measureable degradation of device performance. Additionally, we demonstrate the growth of III-Sb buffers on GaAs and silicon substrates for both n- and p-channels through the use of an epitaxial array of interfacial misfit dislocations formed between the III-Sb alloy and the substrate. The interfacial misfit array results in the spontaneous relaxation of the highly mismatched III-Sb semiconductor and provides a platform for the realization of high mobility channels on GaAs and Si.

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1. INTRODUCTION

The continuing reduction in the dimensions of silicon transistor channels is leading to an intensive search for alternate semiconconductor channel materials. The III-V semiconductors including GaAs, InAs and InGaAs are leading candidates. The transition to III-V channel regions poses significant issues for fabrication and for radiation hardness of future electronics generations. Two approaches were investigated in this project. One approach was directed at the fabrication of nanowire transistors using either top-down fabrication (by focused ion beam lithography) or bottom-up selective-area nanoscale epitaxial growth. A insulator to isolate the channel from the substrate, enhancing the radiation hardness was incorporated by oxidation of an AlGaAs layer. In-plane NWs with ~200 nm channel width are reported. With the NW channel having cross section ~70 nm × 220 nm and the length 2 μm, the device has V_T ~0.2 V and peak g_m ~24 μS with SS ~ 110-150 mV/dec, which are similar to results achieved with bottom-up GaAs NW MESFETs. Radiation studies with x-ray sources do not show measureable degradation of device performance. Therefore, top-down NW process by FIB is a promising fabrication technology for nanoscale electronic devices.

The second approach demonstrated the growth of III-Sb buffers on GaAs and Silicon substrates through the use of an epitaxial technique involving the formation of interfacial misfit dislocation arrays formed between the III-Sb alloy and the substrate. The interfacial misfit array results in the spontaneous relaxation of the highly mismatched III-Sb semiconductor and provides a platform for the realization of high mobility channels on GaAs and Silicon. We make use of InAs type – II confinement structures for n-type and pseudomorphic InGaSb type – I structures for p-type channels.

2. TOP-DOWN FABRICATION OF NANOWIRE TRANSISTORS

2.1. Summary of nanowire transistor fabrication

The top-down fabrication of an SOI in-plane GaAs nanowire (NW) metal-oxide-semiconductor field effect transistor fabricated by ion-beam direct etching has been demonstrated. For the gate oxide, a ~15 nm-thick liquid-phase chemically-enhanced oxide has been employed. In-plane NWs with ~200 nm channel width are reported. With the NW channel having cross section ~70 nm × 220 nm and the length 2 μm, the device has V_T ~0.2 V and peak g_m ~24 μS with SS ~ 110-150 mV/dec, which are similar to results achieved with bottom-up GaAs NW devices. Radiation studies with x-ray sources do not show measureable degradation of device performance.

2.2 Introduction to nanowire transistor fabrication

Recently, III-V semiconductor in-plane nanowire (NW) field-effect transistors (FETs) have been reported by several research groups. For their high mobility with scalable size, various process technologies such as vapor-liquid-solid (VLS) growth and anisotropic wet etching have

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been examined for their fabrication [1] - [4]. For smaller III-V NWs, bottom up fabrication relying on VLS mechanism is preferentially used rather than top-down process. In the accommodation with Si microelectronics, however, top-down fabrication of in-plane NWs is particularly attractive for its non-synthetic, catalyst-free, orientation-independent processing that is directly related to high yield and compatibility with versatile applications. Furthermore, metal-oxide-semiconductor (MOS) FETs have a larger voltage swing than metal-semiconductor (MES) FETs that suffer from low forward gate bias by its Schottky barrier limiting the maximum drain current, and thus are more favorable in digital integrated circuits. In this project, top-down fabrication of an in-plane gallium-arsenide (GaAs) NW MOSFET by focused ion beam (FIB) milling is investigated with a gate oxide formed by liquid phase chemical-enhanced oxidation (LPCEO) [5].

FIB is an easily accessible nanoscale processing technique by direct etching without sophisticate lithographies but leaves damage on etched surfaces such as amorphorization and implanation effects that may not be suitable for NW fabrication. To relieve these undesirable effects on the NW surface, FIB milling and LPCEO is employed in this project. LPCEO is a low-temperature chemical oxidation process for III-V semiconductors and can keep the current channel at the inside of an NW from the damaged surface with an oxide film. Also, this oxide film can be used as gate oxide and makes it possible to fabricate III-V MOSFETs. For III-V compound semiconductors, unlike Si technology, finding materials for the gate oxide is an inherent issue that must be resolved for high performance MOSFETs. LPCEO is known for micro-scale planar III-V FETs, but has not been examined in nanoscale regime with 3-dimensional faceted NW structures. While there are a lot of articles discussing LPCEO, it has not been examined in NW MOSFETs that require an extremely thin gate oxide film.

One of the critical tasks is therefore to implement a gate oxide film for NW (nanowire) MOSFETs with LPCEO. In this project, it has been successfully applied for the first time to top-down-processed NWs that have a non-planar crystal shape resulting from FIB milling. As mentioned earlier, LPCEO has several advantages for GaAs while some issues on material quality related to breakdown and leakage requires further study for NW FETs that operate with a very thin gate oxide film

The device of this project is located on Al_2O_3 forming a semiconductor on insulator (SOI) structure that is transformed from $Al_{0.98}Ga_{0.02}As$ by lateral hydrolyzation oxidation (LHO) [6]. In spite of this top-down fabrication process, the nm-scale channel fabricated by FIB is electronically regarded as an in-plane NW with the suppression of current leakage to the substrate by SOI. Also, SOI allows use of micro-scale ohmic pads directly connected to NWs for planar devices in a single epitaxial layer. The minimal effective channel cross section and length of the GaAs NW in the device is approximately 70 nm × 220 nm and 2 μm respectively. This project reports the top-down fabrication of GaAs in-plane NW MOSFET by FIB milling and its characteristics associated with the NW channel surrounded by ~15 nm thick gate oxide from

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LPCEO. Merging LPCEO with FIB can create a brand-new process technology for the nano-fabrication of III-V devices. The radiation effects on these devices has been tested in AFRL.

2.3. Methods, Assumptions, and Procedures

2.3.1. LHO of $Al_xGa_{1-x}As$

LHO of $Al_{0.98}Ga_{0.02}As$ is performed in a furnace with hot water vapor carried by nitrogen gas. Figure 1 shows a schematic diagram of the apparatus employed for LHO in this work. The major parameters for this process are furnace temperature, bubbler temperature, and hot water

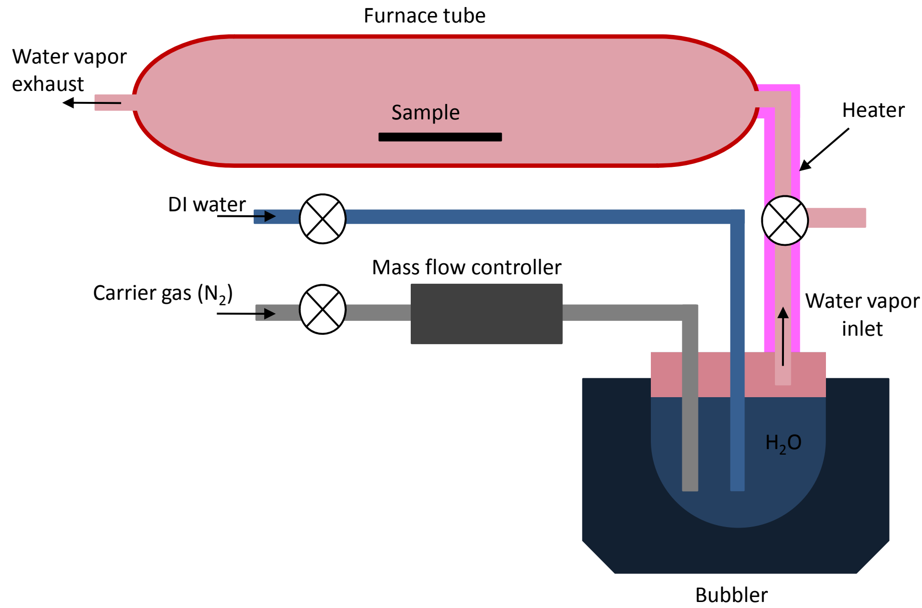

Figure 1. A schematic diagram of LHO apparatus.

vapor flow rate that are optimally set to 460°C, 90°C, and 4.5 *l*/min respectively.

Under this condition, LHO has been examined with the access of water vapor to the $Al_{0.98}Ga_{0.02}As$ layer laterally by exposing its side surface with mesa- and trench-type etching. Figure 2 shows a plot of t versus d_{ox} measured from trench-type surface profile. Figure 3(a) shows a top view microscope image of a mesa treated by LHO with schematic cross sectional diagram. As expected, the oxidation length, d_{ox}, measured from the trench is increased with t but ultimately shows a saturation behavior as t increases further. The averaged LHO rate is defined with d_{ox}/t and is indicated in Figure 2(a) (right y-axis). The averaged LHO rate increases quickly at the very beginning and has the peak of ~3.3 μm/min around t = 10 min but slowly decreases with increasing t beyond 10 min and is reduced to ~ 2 μm/min for t ~ 50 min. The differential LHO rate defined as $\Delta d_{ox}/\Delta t$ in Figure 2(b) reveals its time dependence more accurately. It has the maximum value of ~ 4 μm/min around t = 10 min but rapidly decreases to ~ 1μm/min near t = 50 min. Thus, at least 25 and 50 min LHO is necessary for a mesa- and a trench-type surface

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profile respectively to obtain ~100 μm-wide Al_2O_3 under NW FET for electrical device isolation from the substrate. The lines following data points in Figure 2 are for eye-guiding, not the results of curve fitting.

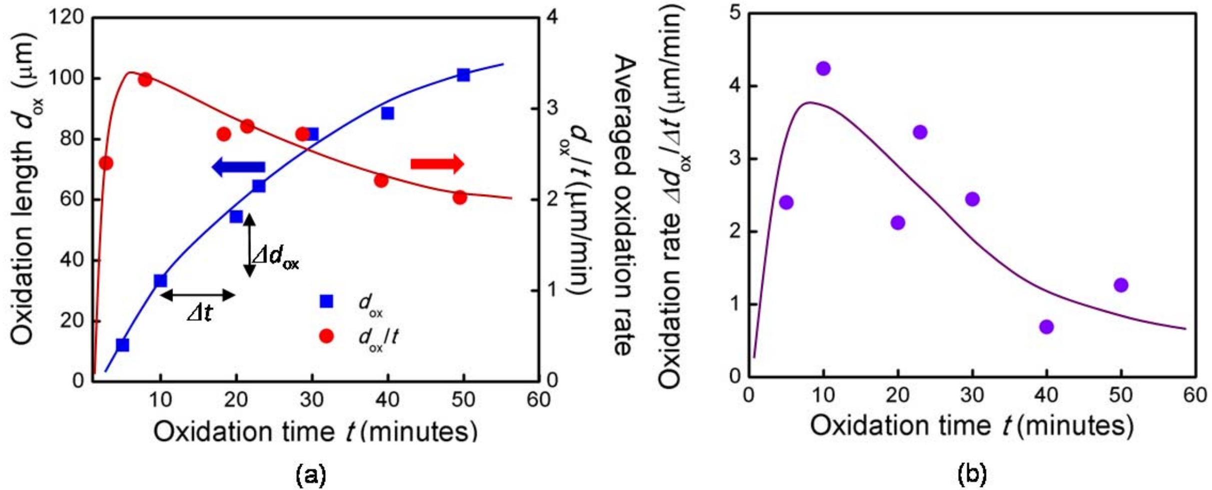

Figure 2. (a) A plot of oxidation time versus oxidation length (left y-axis) and averaged oxidation rate (right y-axis). (b) A plot of oxidation time versus differential oxidation rate

Another important phenomenon observed in the scanning tunneling electron microscopy (STEM) image in Figure 3(b) is the vertical oxidation proceeding into GaAs capping layer from the GaAs/$Al_{0.98}Ga_{0.02}As$ interface that changes GaAs into Ga_2O_3. Compared with LHO along the $Al_{0.98}Ga_{0.02}As$ layer, however, the vertical oxidation into the GaAs capping is very slow. Its rate is about 4 nm/min. A similar vertical oxidation occurs on the other side of $Al_{0.98}Ga_{0.02}As$ layer but the rate is only about 1 nm/min, considerably lower than that of the upper side. This is because the Si dopant concentration of the GaAs capping (~2 × 10^{18} cm^{-3}) is different from that of the GaAs underneath the $Al_{0.98}Ga_{0.02}As$ layer (~1 × 10^{17} cm^{-3}). It is not clear whether vertical oxidation of GaAs depends on dopant concentration in GaAs. Further research to understand the role of dopant in vertical oxidation of GaAs is presently under way.

Both LHO of $Al_{0.98}Ga_{0.02}As$ and vertical oxidation of GaAs result in porous type oxides. In Figure 3(b), the oxidized $Al_{0.98}Ga_{0.02}As$ is spatially uniform without noticeable contrast fluctuation over the cross section in STEM image. On the other hand, the oxidized GaAs has large contrast variation along the oxidation direction vertical to the GaAs/$Al_{0.98}Ga_{0.02}As$ interface as well as along the interface which implies considerable density fluctuation. Most of the fluctuation is due to the formation of voids resulting from the loss of As atoms like $Al_{0.98}Ga_{0.02}As$, but GaAs has the melting point lower than $Al_{0.98}Ga_{0.02}As$ (1238°C < 1740°C) and is thus thermally less stable in crystalline structure under the same thermal process. This is one of the reasons why oxidized GaAs has poor quality compared with oxidized $Al_{0.98}Ga_{0.02}As$ in

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Figure 3(b). Unlike LHO, LPCEO keeps most of As atoms for better oxide quality. Further study is required to confirm its role in device performance.

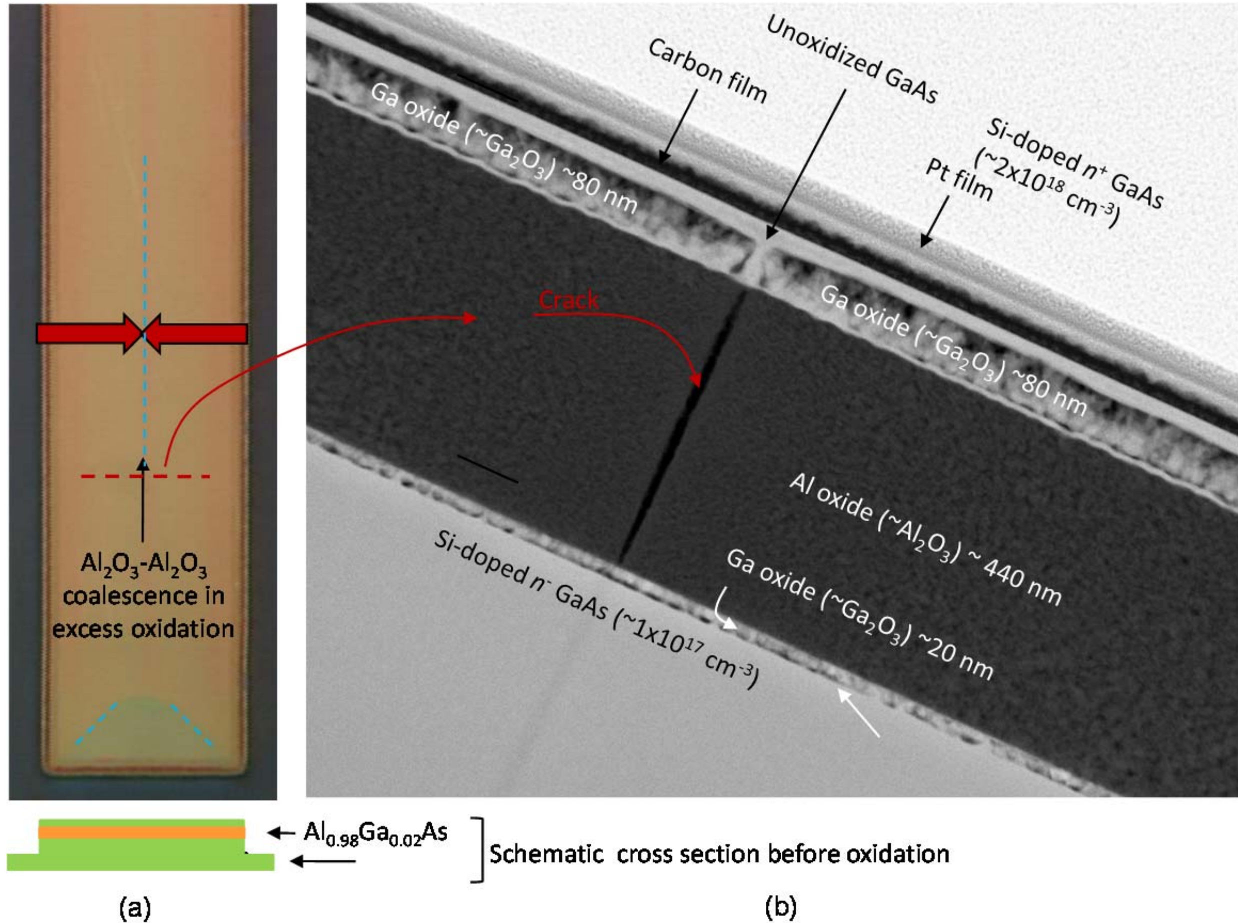
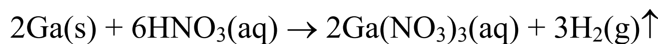


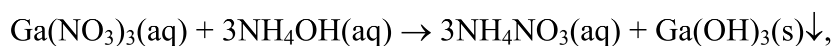
Figure 3. (a) A top-view optical microscope image of a fully oxidized, ~40 µm-wide, $Al_{0.98}Ga_{0.02}As$ mesa (top) and a schematic cross section (bottom) by LHO. (b) A STEM image of the cross section along the red dashed line indicated in (a).

2.3.2. Liquid-Phase Chemically Enhanced Oxidation (LPCEO) of GaAs

The chemical etchant is made with 6N Ga, HNO_3, and NH_4OH. The basic chemical reactions are



$$2Ga(s) + 6HNO_3(aq) \rightarrow 2Ga(NO_3)_3(aq) + 3H_2(g)\uparrow$$



$$Ga(NO_3)_3(aq) + 3NH_4OH(aq) \rightarrow 3NH_4NO_3(aq) + Ga(OH)_3(s)\downarrow,$$

where the $Ga(OH)_3(s)$ is removed by filtering. Then, NH_4NO_3 reacts with GaAs and results in Ga_2O_3 and As_2O_3. The oxidation rate is critically affected by pH and temperature. A high oxidation rate is achieved at pH ~4 - 4.5 and high refractive index film is available at low pH. In

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this project, pH and temperature were set to 4.9 and 70°C, respectively, to provide an oxidation speed of ~100 nm/hr that is appropriate for nanoscale devices. A slight increase of volume by the incorporation of oxygen into GaAs was observed by LPCEO. This is similar to the results of LHO but with less reduction. The oxide film from LPCEO has been confirmed with GaAs MOSFETs at large scale that work with several hundred nm-thick gate oxide films. At this scale, leakage through a gate oxide prepared by LPCEO has not been reported. In this project, the oxide film thickness must be comparable to or less than the NW channel dimension and the material properties should be examined at nm-scale.

Figure 4 shows the calibration results of LPCEO critically important for the gate oxide of GaAs NW MOSFETs. The FIB-reduced channel was processed with LPCEO immediately after the removal of native oxide by diluted NH_4OH. Oxidation speed by LPCEO was calibrated with the conductance of GaAs channels. Three 20 μm-long, 600 nm-wide, 500 nm-thick n^+-GaAs channels which have the channel cross section more than 10 × the NW channel were fabricated and the change of their current was measured by taking the ratio of channel current before and after LPCEO ($I_{d,a}/I_{d,b}$, where a and b in subscript mean after and before FIB etching.) with etching time, t_e, varied up to 90 minutes. The dashed lines are merely as a guide to the eye. Figure 4(b) is a plot of current versus bias for t_e = 90 minutes before and after LPCEO. Figure 4(a) (left axis) presents a plot of $I_{d,a}/I_{d,b}$ versus t_e. As expected, I_d decreases and a slight deceleration of the oxidation speed is noticed as t_e increases. In Figure 4(a) (right axis), oxidation depth (or oxide film thickness) estimated from $I_{d,a}/I_{d,b}$ is shown under the assumption of uniform

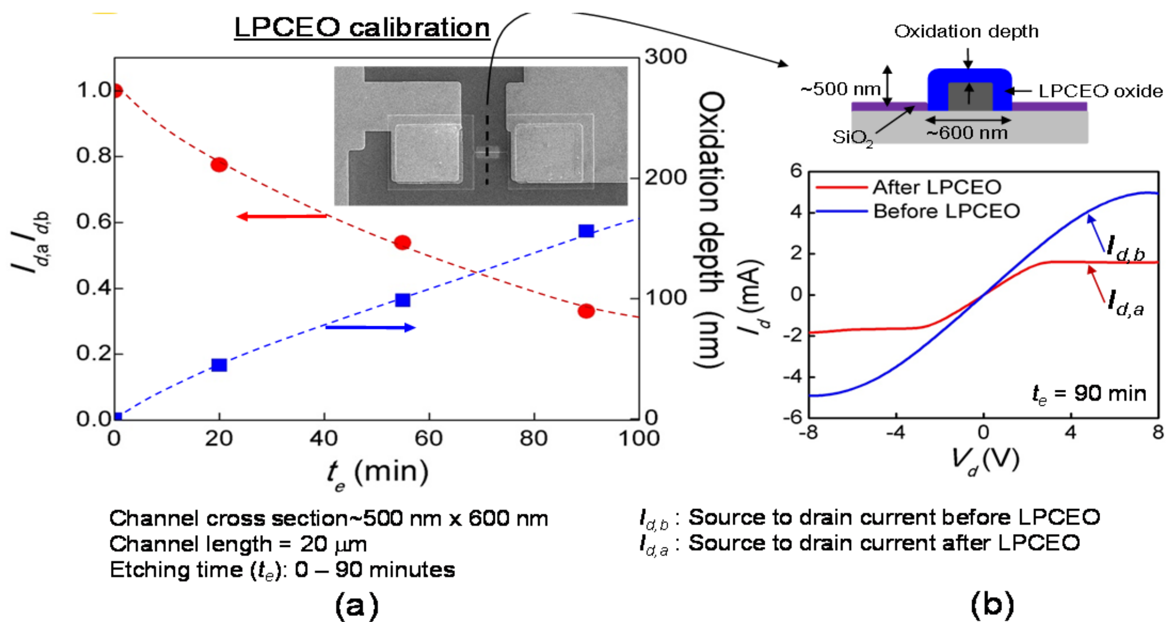

Figure 4. (a) A plot of current ratio (left axis) and corresponding oxidation depth (right axis) versus oxidation time. (b) A plot of source to drain current versus in-plane NW channel bias before LPCEO and after t_e = 90 minutes.

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oxidation from all three sides inward to the channels and the consideration of their cross section close to a rectangle, as illustrated in the inset of Figure 4(b).

2.3.3. Device process

The device process for in-plane SOI NW GaAs MOSFETs fabricated with FIB milling and LPCEO is summarized in Figure 5. The initial layer structure is shown at the top left. The ultimate layer structure of an NW channel from this process is schematically shown in Figure 6. It was grown on a semi-insulating GaAs(001) substrate by molecular beam epitaxy. The Si-doped (~2×10^{18} cm^{-3}), 100 nm-thick GaAs layer at the top is for an NW channel. LHO for SOI established in previous section has been applied together with FIB milling for an in-plane NW and LPCEO for gate oxide surrounding it. The first step is the transformation of the $Al_{0.98}Ga_{0.02}As$ layer underneath the conducting layer to Al_2O_x (x~3) by LHO. Then, as seen in Figure 5, the resulting cross section of the NW MOSFET on the Al_2O_3 film forms SOI that minimized the current leakage through the substrate. During LHO, the top surface of the layer structure was passivated by an SiO_2 film but the n^+-GaAs layer was also slightly oxidized along

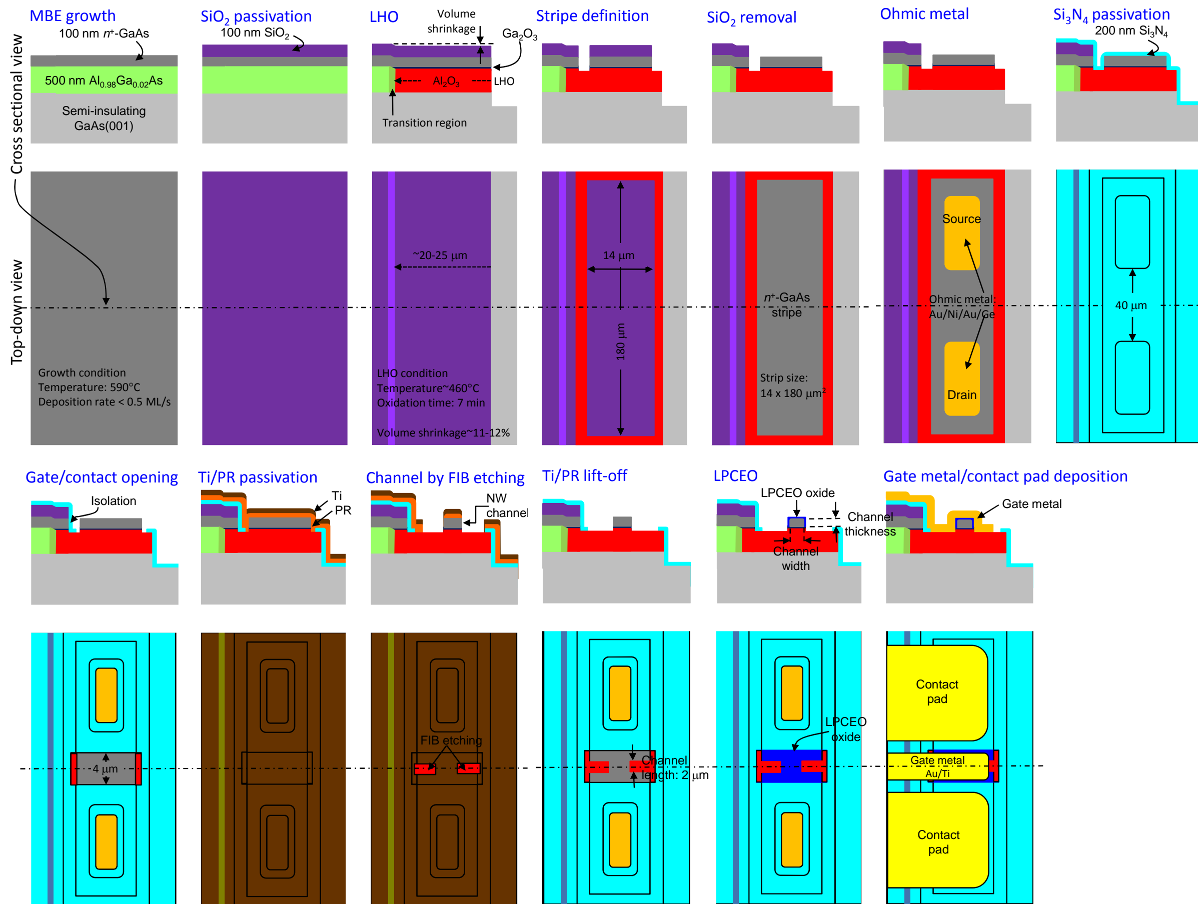

Figure 5. Diagram of the process flow of FIB- and LPCEO-assisted NW GaAs MOSFET.

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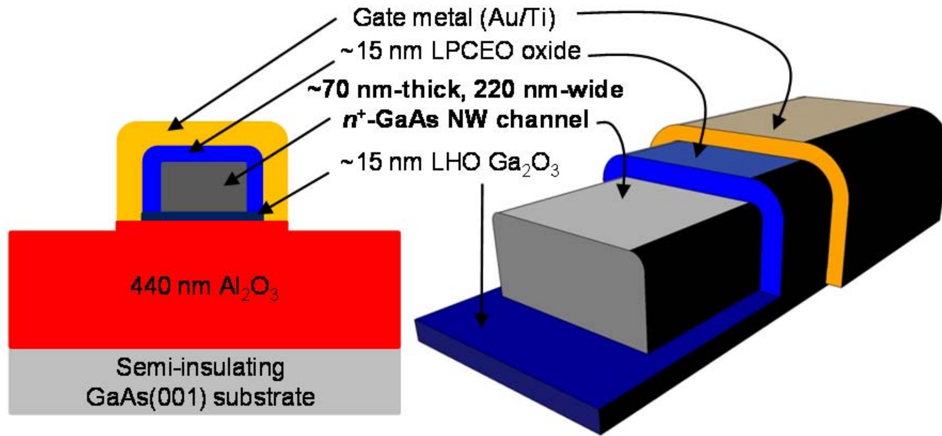

Figure 6. The structure of the channel used for an in-plane NW GaAs MOSFET.

the GaAs/Al_2O_3 interface and its bottom region (~15 nm in thickness) was changed into Ga_2O_y (y~3). Then, the actual thickness of the channel is reduced to ~85 nm by LHO.

After LHO, the layer structure underwent standard FET process and FIB etching. The n^+-GaAs conducting layer in SOI was processed into a 14 µm-wide, 180 µm-long stripe with photolithography and chlorine-based plasma etching, as illustrated in Figure 6. Its long side is parallel to the trench for LHO so that the whole stripe can be located on the 25 µm-wide Al_2O_3 film. Two 10 µm × 60 µm ohmic metals were deposited at both ends for source and drain contacts. Owing to SOI, these micro-scale ohmic contact areas do not cause any measurable leakage current through the Al_2O_3 layer. The stripe was then passivated by a 200 nm-thick Si_3N_4 film for the channel fabrication with FIB. A 4 µm-wide opening across it was fabricated into this film by CF_4 plasma etching at the middle of the stripe. Figure 7 present the ion-beam images of the stripe before and after FIB milling. As seen in Figure 7 (left), the stripe in the Si_3N_4 opening area was narrowed by FIB milling. In the right of Figure 7 and its inset, two rectangular regions in the opening were directly etched out to leave a 250 nm-wide, 2 µm-long channel between them. The etch depth was controlled to touch down the Al_2O_3 layer. As illustrated in Figure 6, the channel in Figure 7 behaves like an in-plane NW that is electronically isolated from the substrate by SOI and directly connected to ohmic pads in a single epitaxial layer for a planar MOSFET. To keep the channel from any damage by FIB, its top surface was passivated by a Ti/photoresist film stack. After FIB milling, the Ti film was simply removed by a lift-off process.

The last step for NW MOSFET was LPCEO to form a gate oxide surrounding the in-plane NW channel. Since a ~15 nm-thick Ga_2O_3 film is already embedded between the NW channel and the Al_2O_3 film as a byproduct of LHO, as explained earlier, the pH of the etchant was set to ~4.9 to increase Ga/As ratio in the oxide film so that the in-plane NW can be surrounded by similar materials. LPCEO proceeded only at the Si_3N_4 opening shown in Figure 7. Also, the etching time was adjusted to proceed oxidation into the channel for ~15 nm from the

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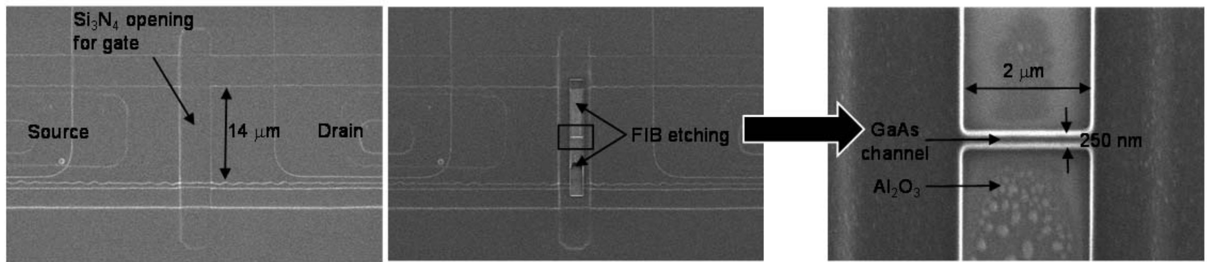

Figure 7. Ion-beam images of a ~2 μm-long, 250 nm-wide channel, in-plane NW GaAs MOSFET before (left) and after (middle and right with magnification) FIB milling.

surface that is similar to the thickness of the Ga_2O_3 at the bottom. Then, the effective cross section of the conducting channel for NW MOSFET is reduced further to ~70 nm × 220 nm, its length is 2 μm, and the thickness of the oxide film surrounding it as gate oxide is ~15 nm, as illustrated in Figure 10. As ohmic and gate metals, conventional Au/Ni/Au/Ge and Au/Ti film stacks were used.

2.4. Results and Discussion

2.4.1. Radiation effects on LHO-grown Al_2O_3

A simple capacitor made of large-area, Al_2O_3 was fabricated to examine radiation hardness of Al_2O_3 generated by hydrolyzation oxidation (HO). To implement such a wide-area Al_2O_3 avoiding delamination during and after oxidation, top-down HO initiated from the surface of an $Al_{0.98}Ga_{0.02}As$ layer was employed instead of lateral oxidation. First, a GaAs capping layer was removed by selective etching and the $Al_{0.98}Ga_{0.02}As$ layer of which the whole surface is

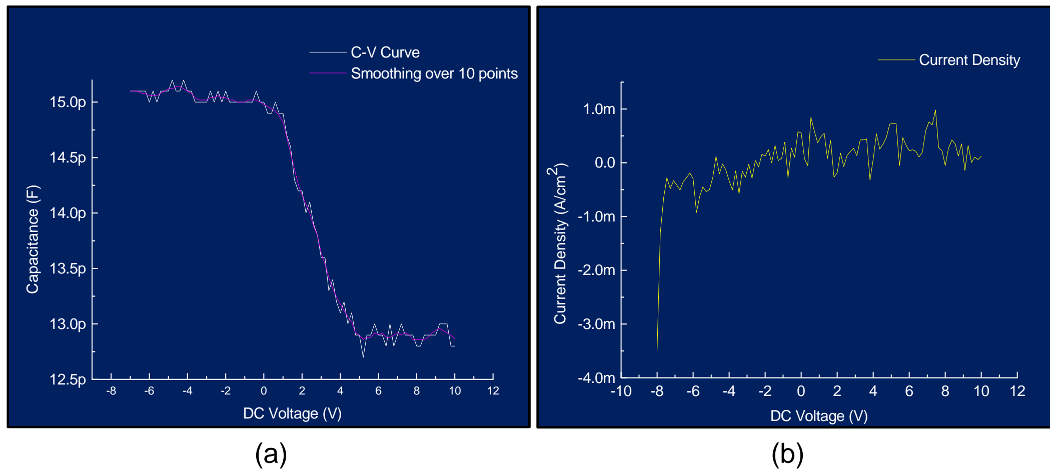

Figure 8. (a) C-V curve and (b) I-V curve of a 330 × 330 μm² capacitor with a HO-generated $Al_{0.98}Ga_{0.02}As$ layer.

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immediately exposed to hot water vapor was oxidized for 5 minutes in the furnace. On the HO-generated Al_2O_3, a 250 nm-thick Al film was deposited with electron-beam evaporation as an electrode. The smallest dimension of the capacitors determined by electrode size is 330 μm × 330 μm. Figure 8 shows capacitance-voltage (C-V) (a) and current-voltage (I-V) (b) relation of the capacitor. Figure 8(a) exhibits a typical capacitance variation decreasing with the formation of inversion layer as bias changes. Also, Figure 8(b) presents a conventional I-V characteristic revealing a breakdown at high bias. The dielectric constant estimated from the curve with the thickness of Al_2O_3 ~ 440 nm and the given area is ~8, which is similar to the reported data ~7. This is lower than that of alumina which is known as ~9.

The capacitors were irradiated by an x-ray source, ARACOR 4100 operating at 45 kV/20 mA onto a tungsten target. Radiation rate was set to 4.7 x 10^3 rad(Si)/minute. Figure 9 presents C-V curves of the capacitor similar to that used in Figure 8 which was measured after the irradiation with the dose increased up to 1.3 Mrad(Si). In Figures 9(a) and 9(b), the capacitor was not biased (V_b = 0) and biased at V_b = 20 V during x-ray irradiation, respectively before C-V measurement. When V_b = 0, the overall variation of capacitance up to 1.2 Mrad(Si) in Figure 9(a) is not changed much and thus not very different from that of SiO_2. For V_b = 20 V, the C-V curves in Figure 9(b) exhibits slight breakdown as the radiation dose reaches 1.2 Mrad(Si).

2.4.2. Basic characteristics of top-down processed GaAs NW conducting channel

Figure 10 shows a photo image of the conducting channel prepared by chlorine-based plasma etching of which the physical dimension (thickness, width, length) is nominally 100 nm, 900 nm, and 8 μm, respectively. The channel in Figure 10 is on an Al_2O_x (x ~ 3) layer which was transformed from the 500 nm-thick $Al_{0.98}Ga_{0.02}As$ layer underneath it by LHO initiated from the trench indicated with a black dashed line. LHO proceeded up to the red dashed line which fully covers the device so that it can be located on Al_2O_3. However, LHO induces not only lateral

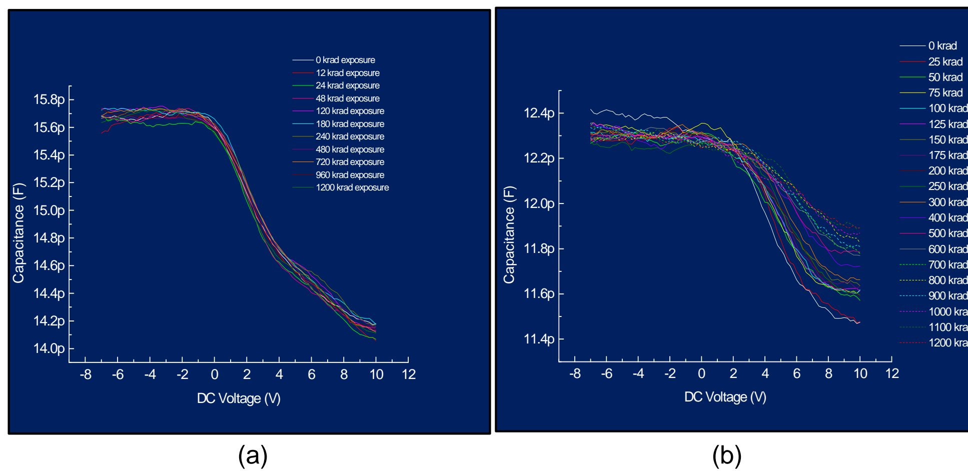

Figure 9. C-V curves of a 330 × 330 μm^2 capacitor with a HO-generated $Al_{0.98}Ga_{0.02}As$ layer after x-ray irradiation under (a) V_b = 0 and (b) V_b = 20 V.

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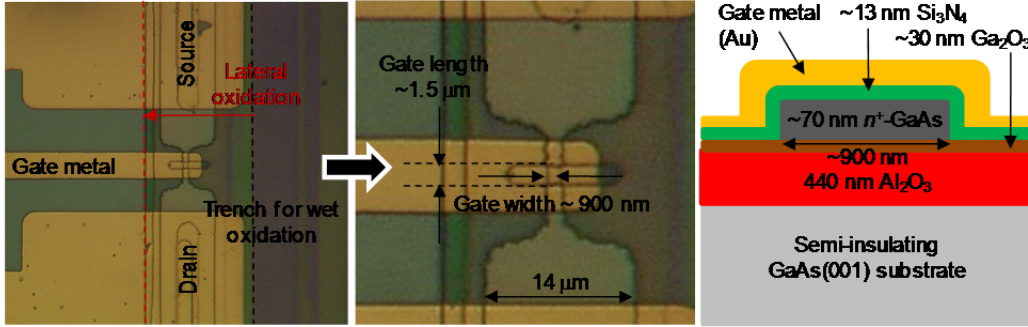

Figure 10. An optical micrograph of a top-down, 900 nm-wide SOI NW GaAs MOSFET (left) processed with chlorine-based plasma etching, with a magnification in a dashed rectangle at left (middle) and a schematic cross sectional view of the channel (right) .

oxidation of $Al_{0.98}Ga_{0.02}As$ but also vertical oxidation into the GaAs layers sandwiching it during oxidation process in a furnace as observed in Figure 3(b). As seen earlier, it has been confirmed that this vertical oxidation is critically affected by the doping in GaAs and is ~4 nm/min for ~2 × 10^{18} cm^{-3} Si doping. It should be noted that the thickness of the GaAs conducting layer is only ~100 nm and it can be fully oxidized, providing no current channel if the LHO time exceeds 25 minutes. Beside the cumulative stress at GaAs/Al_2O_3 interface due to the volume shrinkage in LHO, the vertical oxidation is another limitation on LHO time in top-down SOI GaAs MOSFETs. In this project, LHO time is limited to 7 minutes to have a conducting thickness of at least ~70 nm with ~30 nm vertical oxidation. It has been observed that LHO proceeds at most 20 µm from the trench for 7 minutes. That is considerably smaller than the lateral dimension of the whole device = 80 µm. To locate the device on Al_2O_x for SOI, another mask set having a lateral device size smaller than 20 µm was implemented. This explains the device size in Figure 10 that is reduced to 14 µm, to fit into the requirement for SOI in 7-minute LHO with keeping the conduction channel thickness ~ 70 nm. Therefore, the channel of top-down SOI GaAs MOSFET in Figure 6 is actually ~70 nm thick, ~900 nm in width, 8 µm in length after LHO, and is located on ~30 nm Ga_2O_y (y ~ 3)/440 nm Al_2O_x (x ~ 3)/semi-insulating GaAs substrate. A ~13 nm-thick Si_3N_z (z ~ 4) film deposited by PECVD was used as a gate oxide, as illustrated in the figure (right). The gate length was set to 1.5 µm by opening Si_3N_4.

Figure 11(a) presents the I_d-V_d curves measured from the device in Figure 6. This top-down SOI GaAs MOSFET is 'normally on'. However, I_d at $V_g = 0$ is extremely low. The channel thickness of this device (~70 nm) is considerably small and the electrons could be partially depleted by surface and interface states surrounding the channel. Besides, there remains some uncertainty in doping levels as a result of the different growth processes.

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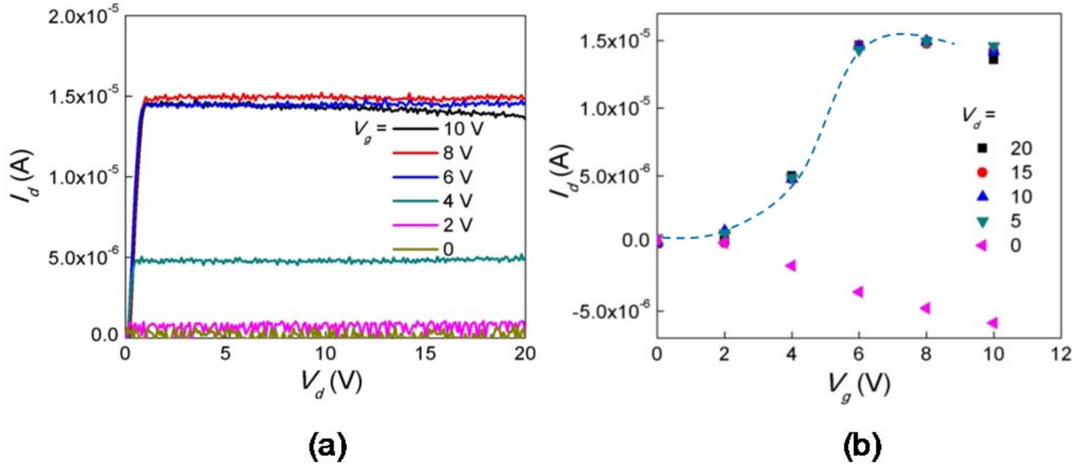

Figure 11. (a) A plot of I_d-V_d measured from a top-down, 900 nm-wide, single SOI NW GaAs MOSFET with the variation of V_g from 0 to 10 V. The gate length is 1.5 μm. (b) A plot of the transconductance I_d vs. V_g obtained from (a).

Device performance becomes clear by applying finite V_g. In Figure 11(a), I_d-V_d relation shows conventional enhancement mode FET characteristics as V_g varies from 0 to 10 V with 2 V step increment. In Figure 7(a), I_d for V_d = 10 V at saturation region is increased from ~9.5 × 10^{-7} A to ~1.5 × 10^{-5} A as V_g changes from 2 to 8 V. It corresponds to enhancement mode, as expected. Figure 11(b) is a plot of I_d versus V_g at different V_d's where I_d is rapidly increased with V_g up to 6 V and slightly decreased with increasing it beyond 6 V. The transconductance, g_m (= dI_d/dV_d), therefore increases with V_g and the peak g_m is approximately ~5 μS.

2.4.3. Device characteristics

For the NW MOSFET, as mentioned earlier, t_e was controlled from Figure 4(a) so that its channel was surrounded by a ~15 nm-thick oxide film. First, the channel width of the in-plane SOI NW GaAs MOSFET was varied from 2 μm down to 250 nm by FIB with keeping the channel length to 2 μm. Source-drain bias, V_d, and the gate voltage, V_g, were varied at the ranges of 0 - 2.5 V and -0.2 - 0.5 V, respectively. Figure 12 shows their I-V characteristics measured at room temperature. They show the saturation of source-drain current, I_d, but the saturation voltage is decreased from ~1.5 V to ~0.5 V as the channel width is changed from 2 μm to 250 nm. Also, I_d at saturation region is reduced from ~150 μA to ~4 μA for V_g = 0.5 A, that is not directly proportional to channel width variation. Since LPCEO provides almost the same thickness gate oxide, the actual channel width affected by it could be more critical to the smallest channel width device.

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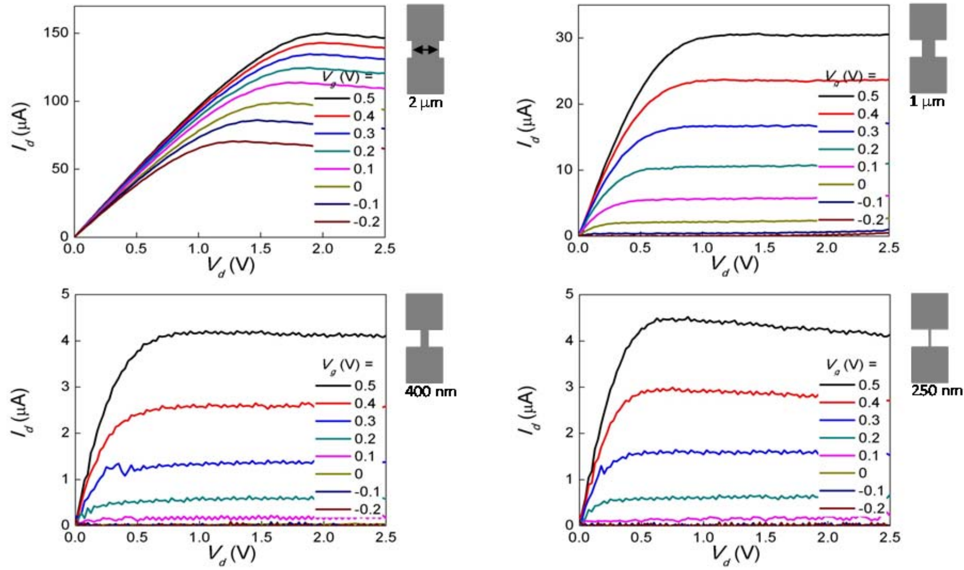

Figure 12. I-V characteristics of in-plane, SOI NW GaAs MOSFETs with channel width variation.

In this section, we focus on the MOSFET with channel width of 250 nm (bottom right in Figure 12). The inset of Figure 13(a) shows the change of I_d of the NW MOSFET before FIB, before and after LPCEO. It reveals the details near the zero bias. Likewise, the current after LPCEO also keeps ohmic behavior with saturation region but is about 20 - 30% of that before it. This is noticeably different from the expectation based on the NW cross section in the inset of Figure 4(b). This difference could be due to the different physical dimension; the smaller NW may have more anisotropic oxidation speed and profile resulting from its shape and stress associated with layer structure than the larger ones used in calibration. For this reason, the 70 nm × 220 nm channel size can be assumed as the upper limit of the NW channel cross section. Further research is required to understand LPCEO at nanoscale regime for better applications.

From Figures 10 and 11, it can be noticed that the NW MOSFET in this project is very different from conventional FETs. First, it doesn't have any junctions between source, drain, and channel used in conventional device analysis. Also, it may have series resistance from the NW channel to source and drain. Figure 13(a) provides good evidence for ohmic contact to the stripe. In Figure 13(a), the NW width after FIB, 250 nm, is 1.8 % of the original channel width, 14 μm. On the other hand, the current reduction by channel narrowing is dramatic; the current of the stripe through the NW channel is only ~1 % of that before FIB etching. This means the presence of the NW channel dominates the current in the stripe and implies the series resistance is not significant in device performance. The inset in the figure reveals the details near zero bias.

In Figure 12, a linear region is clearly defined together with a saturation region for the device having channel width less than or equal to 1 μm. This also implies an ohmic contact to the stripe and as a result to the NW. Because the ohmic pads are kept away from both ends of the

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NW by the distance more than 5 × NW length, no enhancement of the drain current, I_d, at high drain bias, V_d, due to the channel shortening from the depletion region of the drain is expected in the saturation region. Instead, I_d in saturation region slightly decreases with increasing V_d for the range of bias examined in this work. This becomes clearer at larger V_g. This could be electron scattering by the GaAs/oxide interface along the NW that becomes more significant among the carriers highly confined in the inversion state at larger bias. In Figure 12, I_d at V_g = 0 is only about 0.15 μA at saturation region for the channel width of 250 nm even though the NW is heavily doped by Si. While the MW MOSFET can perform both enhancement and depletion modes at the given doping level, this implies the NW channel completely surrounded by the oxide films is mostly depleted probably by the GaAs/oxide interface states and works in enhancement mode rather than depletion mode.

Figure 13(b) is a plot of I_d versus V_{gs} revealing the transferconducting characteristics of the device. The threshold voltage V_T, is ~0.2 V. The I_{on}/I_{off} ratio is ~10^3 and the subthreshold swing is conservatively measured as ~110 - 150 mV/dec from the inset. The peak g_m is ~ 24 μS at V_d = 0.9 V and its value normalized by channel width is ~109 mS/mm. Although direct comparison may not be available for their different channel length, this is a significant improvement from the device shown in Figure 11 where it has transconductance of ~5 μS with 8 μm channel width. Such enhancement of transconductance could be partly due the narrow channel width accompanying 3-side facet channel effects. These are comparable to those reported with GaAs NW MESFETs fabricated by bottom-up process except for positive V_T that is feasible in MOSFET structures. The reported MESFET performance is summarized in Table 1.

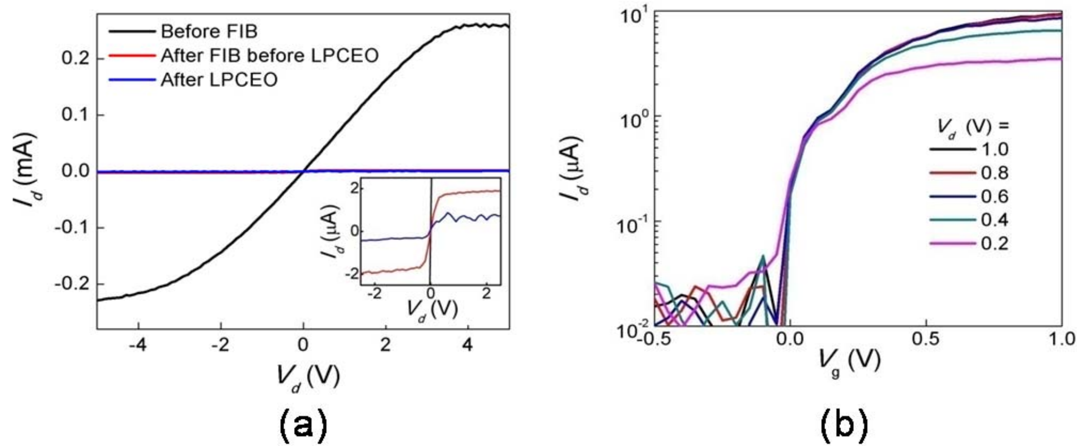

Figure 13. (a) A plot of source to drain current versus bias of the in-plane NW channel before FIB, after FIB but before LPCEO, and after LPCEO with no gate. (b) A plot of I_d versus V_g for transconductance.

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Table 1. Summary of recent in-plane NW GaAs FET results.

Ref/Fabrication	Channel Size (nm)/Substrate	Gate & Type	g_m (mS/mm)	SS (mV/dec)	I_{on}/I_{off}
[1]/VLS	~ 250/ SI GaAs (001)	Au/Ti MESFET	23	150	240
[2]/VLS	<250/ SI GaAs (001)	AlGaAs/Ti/Au HEMT	83	181	~10^4
[3] Etch, pick and place	~200/Plastic	Au/Ti MESFET	7	<150	<10^7
[4]/VLS	~250/ GaAs(110)	Au/Ti MESFET	76	169	850
This work/ MBE, FIB	~70x220/ Al_2O_3	Au/Ti/Ga_2O_3 MOSFET	109	110-150	10^3

A couple of issues related to fabrication should be addressed. One is whether the surface damage at the sidewall of the NW by Ga ion beam during FIB etching is properly relieved by an LPCEO oxide. The other is the material properties of the LPCEO oxide used for gate oxide of the NW MOSFET. LPCEO was employed to minimize the FIB damage but its material quality is not clearly analyzed. Also, its thickness uniformity along the NW that is critical in surface or interface scattering of the carriers along the NW must be investigated. Further research is presently under way to understand the role of LPCEP oxide in FIB-processed GaAs NW MOSFETs.

2.4.4. Radiation effects

Figure 14 shows the radiation effects on (a) leakage current to gate, (b) I-V characteristics, and (c) transconductance of the device in Figure 1. Radiation source was ARACOR 4100 operating at 45 kV/20 mA onto a tungsten target. Radiation rate was set to 4.7 x 103 rad(Si)/minute. As seen in Figure 14(a), leakage current to the gate is almost invariant. Figure 14(b) reveals that I-V curves show conventional FET characteristics up to 1.0 Mrad and are similar to those before radiation within experimental fluctuation. In Figure 14(c), slight decrease of Id around VT is observed at 1.0 Mrad. Conclusively, no significant x-ray damage has been observed up to 1.0 Mrad(Si) at zero bias.

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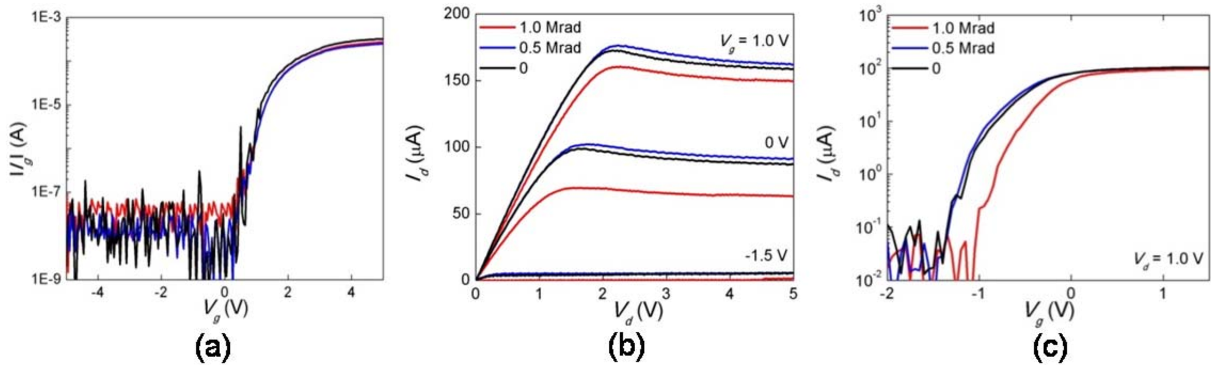

Figure 14. (a) Leakage current to gate, (b) I-V characteristics, and (c) transconductance of a ~2 μm-long, 250 nm-wide channel, in-plane NW GaAs MOSFET before (black) and after 0.5 (blue) and 1.0 (red) Mrad.

2.5. Conclusions

The top-down fabrication of an SOI in-plane GaAs NW MOSFET by FIB etching has been demonstrated. For gate oxide, ~15 nm thick LPCEO oxide has been employed. FIB fabricates in-plane NWs by direct etching and reaches ~200 nm channel width with no lithographies. With the NW channel having cross section ~70 nm × 220 nm and the length 2 μm, the device has V_T ~0.2 V and peak g_m ~24 μS with SS ~ 110-150 mV/dec, which are similar to those from bottom-up GaAs NW MESFETs. Radiation effect examined with x-ray sources doesn't show noticeable degradation of device performance. Therefore, top-down NW process by FIB can be another promising fabrication technology for nanoscale electronic devices.

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3. HETEROEPITAXIAL GROWTH FOR HETEROGENEOUS TRANSISTORS

3.1. Summary of heteroepitaxial growth for heterogeneous transistors

We demonstrate the growth of III-Sb buffers on GaAs and silicon substrates for both n- and p-channels through the use of an epitaxial array of interfacial misfit dislocations formed between the III-Sb alloy and the substrate. The interfacial misfit array results in the spontaneous relaxation of the highly mismatched III-Sb semiconductor and provides a platform for the realization of high mobility channels on GaAs and Si.

3.2 Introduction to heteroepitaxial growth for heterogeneous transistors

The performance and complexity of silicon microchips has doubled every 18-24 months in accordance with Moore's law. The ability to realize this rate of scaling has been achieved largely through the use of the Complementary Metal-Oxide Semiconductor (CMOS) technology. The consistent innovation in the field of silicon CMOS technology and more specifically the ability to reduce the gate length of the field effect transistor has resulted in such performance improvements. However, despite significant achievements in scaling transistors, the technology will soon reach a point where integration of non-CMOS materials such as III-Vs with Silicon is perhaps required to achieve faster transistors.

The predominant schemes for the integration of III-V material with silicon consist of either - monolithic or hybrid integration. Monolithic integration implies the epitaxial growth of the III-V alloy on a silicon wafer while hybrid integration usually involves growing the III-V device separately and then achieving subsequent integration through other measures. The III-V/Si integration through hybrid methods includes conventional wafer bonding [6, 7], novel methods like recess mounting of devices, and newer variations in wafer bonding that incorporate an intermediate layer such as polymers or spin on glass to bond the III-Vs to the Si [8]. While these methods allow independent optimization of both device and circuitry, monolithic growth offers better utilization of the integrating platform, lack of complex assembly and better heat dissipation. The majority of the early work done in this field was focused on monolithically integrating GaAs with Si. A wide variety of GaAs heteroepitaxial growth techniques and procedures were investigated, with different programs targeting different applications. The primary goal was the growth of a continuous, thin GaAs crystalline material covering the entire surface of a silicon wafer, thus taking advantage of silicon's low cost and large surface area. However, the lattice mismatch and thermal expansion coefficient mismatch between the silicon and GaAs crystals results in stress-relaxation imperfections in the large area epitaxy a major problem. An alternative to this approach is to grow the GaAs in small, isolated regions using an oxide/nitride layer as a mask with exposed Si regions where the growth occurs. This mode of growth is called "selective area epitaxy" (SAE).

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In this report we explore the growth of highly mismatched III-Sb semiconductors as a possible material system for the growth of high mobility channels on Silicon and GaAs [9]. The intermediate buffer used will be GaSb due to the fact that we can then realize lattice-matched n-type InAs channels [10] and p-type InGaAs pseudomorphic channels [11] on this platform thus offering a set of complementary transistor technologies. We make use of a growth mode involving the formation of interfacial misfit dislocation arrays at the III-Sb/ Si interface that allows us to realize large area growth of III-Sb alloys without the need for a specialized growth process such as SAE or wafer bonding.

3.3. Methods, Assumptions, and Procedures.

3.3.1 Interfacial misfit dislocation array based growth of GaSb on GaAs.

While the theory of strained growth states that a critical thickness has to be achieved prior to the onset of misfit dislocations, in certain materials systems such as GaSb on GaAs, a two-dimensional (2D) array of misfit dislocations is present at the interface of the GaSb on GaAs growth [12]. This is a fundamentally different growth mode that results in low-defect epitaxial material in which strain energy is solely relieved by laterally propagating (90˚ or Lomer) misfit dislocations confined to the epi-substrate interface [13].

The formation of an interfacial misfit array (IMF) does not proceed through the critical thickness route, but instead makes use of atomic arrangements on the substrate surface to spontaneously relax. However, if the growth conditions are not conducive to forming this atomic arrangement on the substrate the growth then turns pseudomorphic. The highly periodic nature of the array, its long range order and the fact that this arrangement can be picked up by in-situ measurements like reflective high energy electron diffraction (RHEED) indicates that the process may be one of self-assembly.

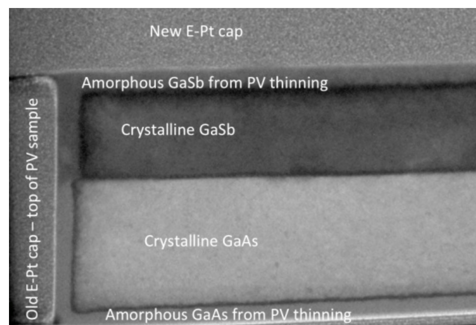

Figure 15. Cross sectional TEM image of GaSb on GaAs sectioned using a focused ion beam miller.

The growth of thick GaSb layers on GaAs starts as islands and with further growth then coalesce into a uniform layer. In previous demonstrations, both 90° and 60° misfit dislocations were present in these islands [14]. While the predominant strain relief mechanism was believed to be the 90° misfits, the minority 60° misfits were shown to cause threading dislocations in the

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GaSb upon coalescence. The source of the 60° misfits is still unclear but attributed to one or more of the following factors - island coalescence, growth temperature and the degree of the mismatch. Island coalescence, in which the {111} planes of adjacent islands merge, has been shown to cause 60° misfits. Supporting data includes a strong correlation between island coalescence and the location of the 60° misfits. The growth temperature has been shown to be a strong factor in determining which type of misfit is produced, with GaSb grown at ~ 520 ºC favoring 90˚ misfits and at ~560 ºC favoring 60˚ misfits [15]. Some researchers have stated that the lattice mismatch is of critical importance in the formation of 90˚ misfits. Low strain systems (< 2 %) have resulted in 60˚ misfits, moderate strain (3 - 4 %) in mixed 90˚ and 60˚ misfits and high strain (> 6 %) in pure 90˚ misfits [16].

Under optimized growth conditions, we have realized a highly periodic array of 90˚ dislocations in the growth of GaSb on GaAs to yield a completely (99.5 %) relaxed and low-defect density GaSb buffer on GaAs. Such a growth is shown in Fig. 15. The growth of the GaSb bulk on GaAs is performed using the V80 molecular beam epitaxy (MBE) reactor and the presence of the two valved crackers for As and Sb sources allows us to exercise a great deal of control in the growth of the structures. The GaAs substrate is de-oxidized at 630 ˚C prior to the growth of 100 nm of GaAs at 580˚C to obtain a smooth surface. Before the Sb growth is initiated, the As valve is closed allowing As ad-atoms to desorb leaving a Ga-rich surface. This process, confirmed by reflection high electron energy diffraction (RHEED) transition from an As-rich (2 x 4) to Ga-rich (4 x 2) surface, reduces As/Sb intermixing. At this point an Sb flux is introduced on the (4 x 2) GaAs surface resulting is an instant transformation to a (2 x 8) reconstructed surface. The Sb over-pressure is stopped and the substrate temperature is reduced to 510 ˚C. The GaSb growth is now commenced at a nominal growth rate (0.2 – 0.8 μm/hr) and the, the RHEED pattern assumes a 1 x 3 indicating that a thin film of GaSb has formed on the surface. The pattern is difficult to analyze during the first few GaSb MLs. But, under optimized growth conditions, a clear 1 x 3 reconstruction pattern appears within the first 3-5 MLs indicating a planar growth mode of relaxed bulk material. Non-optimized parameters yield a spotty RHEED pattern with continued deposition that indicates a defective growth mode.

Figure 16 shows high-resolution and atomic-resolution transmission electron microscope (TEM) bright-field images of a strain-relaxed GaSb on GaAs. The periodic spots in both images correspond to misfit dislocation sites [17]. Figure 16(b) shows that the highly periodic misfit array is localized at the GaSb/GaAs interface and no misfit dislocations at any other location. Careful examination of the image allows for the identification of misfits and analysis of strain relief. Completing a Burger's circuit around one misfit dislocation indicates that the Burger's vector lies along the interface and identifies the misfit as 90˚ type. Measurement of the GaAs substrate and GaSb bulk lattice constants within several MLs of the interface yield a_o= 5.65 Å and a_o= 6.09 Å respectively, indicating complete strain relaxation in the GaSb. The misfit separation, measured to be ~ 56 Å, corresponds to exactly 13 GaSb lattice sites and 14 GaAs

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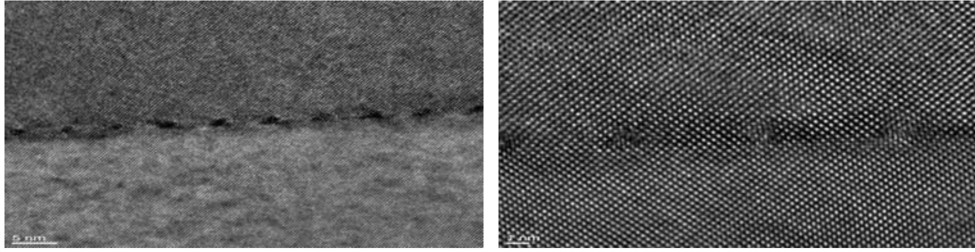

Figure 16. Cross sectional TEM image of the GaSb/GaAs interface.

lattice sites. Thus, every 14th Ga atom has a pair of dangling bonds (one going into and out of the image plane) to accommodate the larger Sb atom in the next (001) plane.

3.3.2. InAs and InGaSb channels on GaAs.

The GaSb buffer layer on the SI-GaAs now forms the platform for the realization of the n and p channels. The two channel materials chosen are InAs and InGaSb respectively for the n and p types. These are both pseudomorphic channels, with the InAs being tensile strained and the InGaSb compressively strained on GaSb. The InAs channel has a type II band offset with respect to the GaSb matrix and thus confines electrons very well. The InGaSb channels are type-I in GaSb and have very poor confinement for holes. Hence using AlSb barriers increases the barrier height and allows for the formation of a channel for holes in InGaSb. The two channel designs are shown in Figure 17. In both designs the channel is within 500 nm of the highly mismatched GaSb/GaAs interface.

Figure 17. Growth structures for InAs based *n*-channel and InGaSb based *p*-channel on GaAs substrates.

While the IMF growth method mitigates the effect of the mismatch and results in reduced threading dislocation density, there are still substantial residual threading dislocations in the channel ($1 \times 10^7 – 1 \times 10^8$ defects/cm^2). In Figure 18 we can observe the InGaSb channel with several threading dislocations intersecting the layer. A higher resolution image captures a clear section of the channel showing the precise interfaces. The threading dislocation density is both samples with InAs and InGaSb channels are in the range of 1×10^7 to 1×10^8 dislocations per

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cm^2. The dislocation density is dependent on the quality of the IMF layer and this can vary depending upon the growth parameters used.

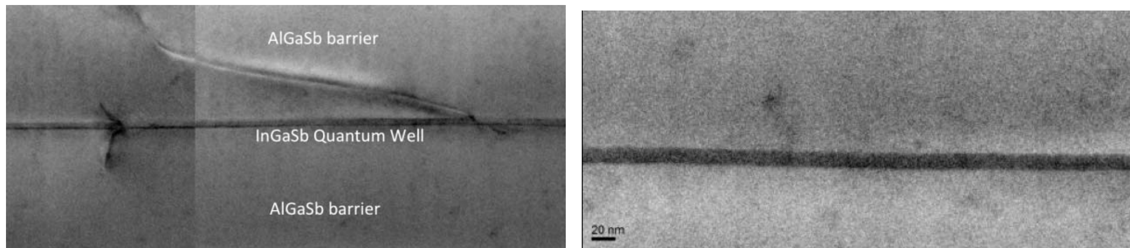

Figure 18. Cross-section TEM image of the InGaSb channels in GaSb barrier.

The channel mobility is measured using Hall measurement using the Van der Pauw method. The samples have Indium contacts that are annealed at 280 ºC in nitrogen ambient. The sample size in both cases is 1 cm x 1cm. The results for the InAs channel is shown in Figure 19. Figure 19 shows the electron mobility and the carrier concentration for the InAs channels as a function of temperature. The mobility for the electrons peaks at 77K at a value of ~ 32,000 cm^2/V.sec. The room temperature mobility of the channel is ~ 13,000 cm^2/V.sec. These results can further be improved with the optimization of the delta-doped layer grown above the channel.

3.3.3. GaSb on silicon substrate.

In this section growth and characterization of low defect-density GaSb on Si (001) substrates using a monolithic self-assembled AlSb nucleation layer is discussed. During the first few monolayers of AlSb growth on Si, highly crystalline islands form. With continued growth, the islands coalesce into a planar material with no detectable islands. The nucleation layer facilitates a completely relaxed AlSb within ~100 ML of deposition according to X-Ray diffraction. The success of AlSb growth on Si is attributed to the interfacial misfit dislocation array formed at the interface between Si and AlSb and the excellent thermal expansion coefficient match between Si and AlSb.

Prior to growth, the Si substrate surface is hydrogen-passivated through an HF treatment. The HF is usually diluted to a 1:10 ratio and the Si wafer is dipped in it. The HF reacts with the SiO_2 and leaves behind a clean Si surface with the dangling bonds passivated by hydrogen atoms. The hydrogen passivation is removed by heating the substrate at 500 °C in vacuum. A thermal cycle at 700 °C ensures the removal of oxide remnants. This is verified by reflection high-energy electron diffraction (RHEED). The substrate temperature is reduced and stabilized at 500 °C and the AlSb is then grown at the same temperature.

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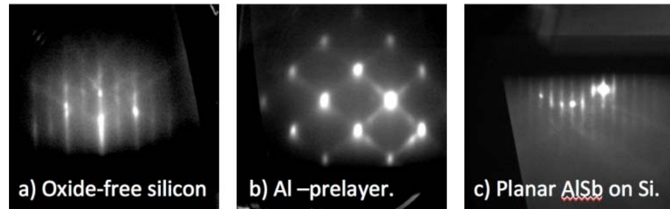

Figure 19. RHEED pattern showing various stages of growth of AlSb on silicon substrate.

Figure 19 shows the evolution of the RHEED pattern during the growth of AlSb on silicon. Part (a) shows the oxide free silicon surface. With the growth of AlSb the surface begins to show island formation. This is shown in part (b). The interconnected dots on the RHEED pattern are typical of relaxed AlSb islands nucleating on Silicon substrates. With substantial growth of AlSb on the silicon, the islands coalesce resulting in a smooth RHEED pattern indicating a planar surface.

Substrate preparation is extremely critical in achieving a good III-V surface. The V80 reactor used for performing the growths in its present configuration cannot be used for Si homoepitaxy due to the substrate heater being limited to ~850 ºC in temperature. Therefore, the atomic level smoothness of the Si wafer achieved during its polishing has to be preserved. This means that the HF etch has to be brief and the material transferred into vacuum within five to ten minutes of the etch. The longer a wafer is exposed to the atmosphere prior to growth the higher the chances of the oxide forming again. While a variety of other etch and wash procedures have been recommended for Si wafers prior to the epitaxial process, we have observed that a single immersion of the wafer in HF for a few seconds is sufficient to remove the oxide [18].

The use of the AlSb interfacial layer is key to the growth of high quality III-Sb alloys on silicon. The use of alternate interfacial layers such as GaSb on Silicon leads to the formation of very large islands and thus very poor coalescence. This leads to extensive threading dislocations and epitaxial layers that cannot be used for any practical purposes. This can be seen in Figure 20 where the similar structures comprising of an AlGaSb barrier and an InGaSb channel are grown on Silicon. In the first image the nucleation is done using a GaSb layer and in the second we make use of an AlSb nucleation layer. It can be seen very clearly that in the GaSb nucleation structure the threading dislocations are extensive while in the AlSb based nucleation the dislocation density is about the same as in GaSb on GaAs.

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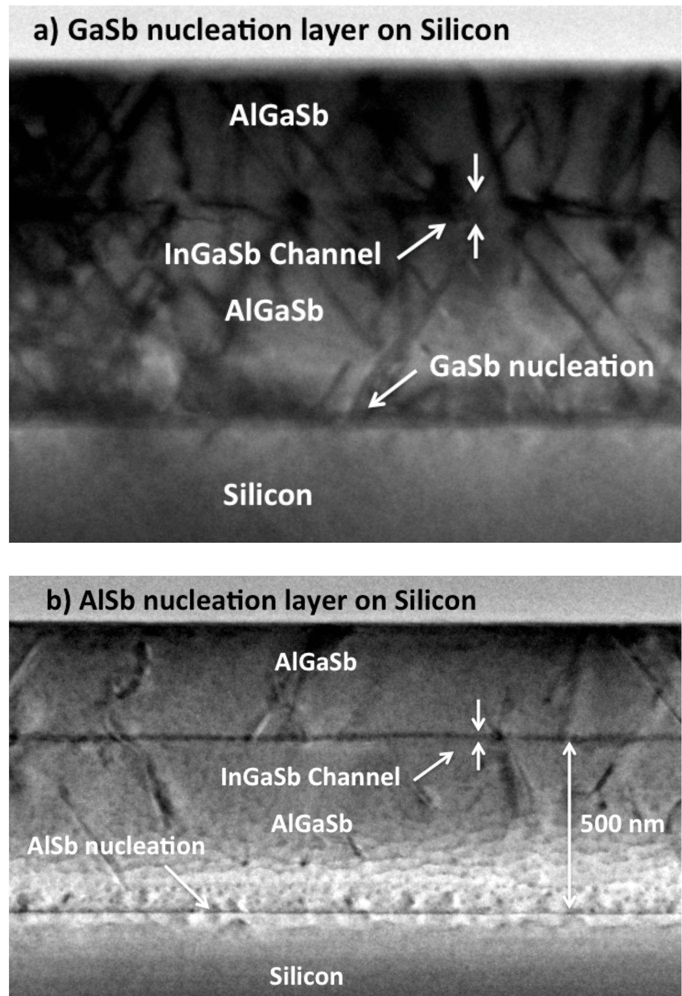

Figure 20. Comparison of threading dislocations in III-Sb epitaxial layers grown on GaSb based (a) and AlSb based (b) nucleation layers on silicon.

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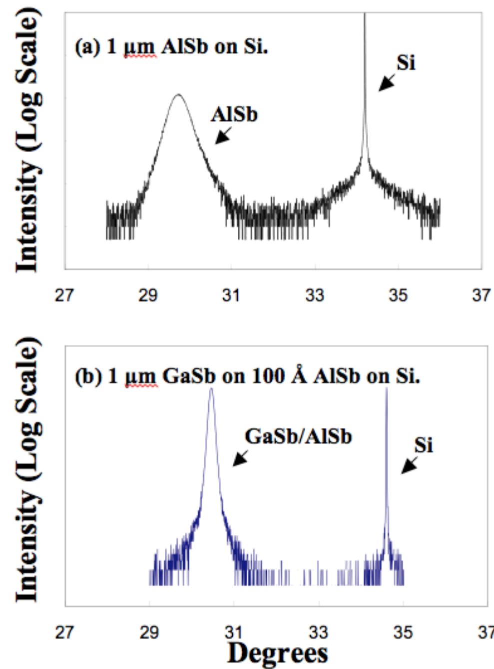

Figure 21. Comparison of GaSb epilayer quality based on AlSb nucleation layer thickness.

While the nucleation of AlSb on Silicon is a critical step in the growth of III-Sb alloys on silicon, the use of thick AlSb nucleation layers can also be detrimental to the epi-layer. Figure 21 shows the X-Ray diffraction spectrum of AlSb grown directly on Silicon and in the second case where AlSb is only used as a 100 Å nucleation layer followed by a thick layer of GaSb. When used as a nucleation layer the X-Ray diffraction full width at half maximum is the narrowest indicating better epitaxial quality. Other groups have seen this result as well.

The growth of the InGaSb channels on silicon can be characterized by studying the photoluminescence from the channels. In Figure 22 we demonstrate the growth of the channel on both Silicon (100) and on Silicon on Insulator (SOI). The photoluminescence is measured from structures similar to those shown in Figure 20. The room temperature photoluminescence from the channels is clearly visible and the intensity is approximately one fifth of the lattice-matched structure on GaSb. The SOI sample shows significantly reduced photoluminescence intensity. The difference in the PL intensity can be attributed to the surface roughness of the samples with the SOI samples being rougher than the Silicon substrate.

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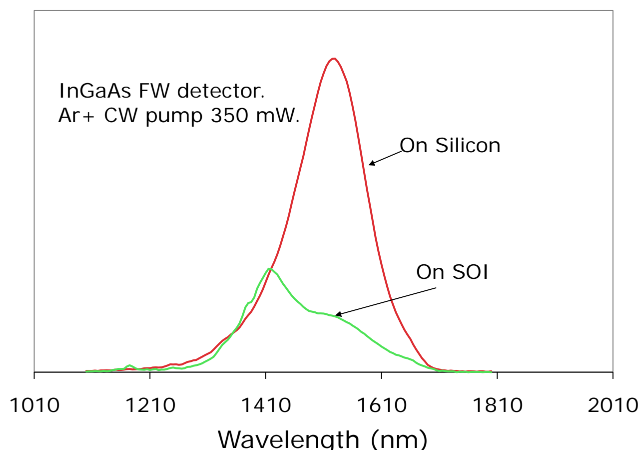

Figure 22. Photoluminescence from InGaSb channels growth on Silicon and SOI.

The Silicon (100) surface typically has single atomic steps and this leads to the formation of extensive anti-phase domains (APD) in the III-Sb semiconductors grown on the Silicon. The formation of the APDs on a 1μm thick AlSb layer on Silicon is seen in Figure 23. The anti-phase domains lead to issues with electrical characterization studies such as Hall measurements making it difficult to determine the mobility of the channels. The suppression of APDs is straightforward and involves the growth of the III-Sb semiconductors on miscut Silicon.

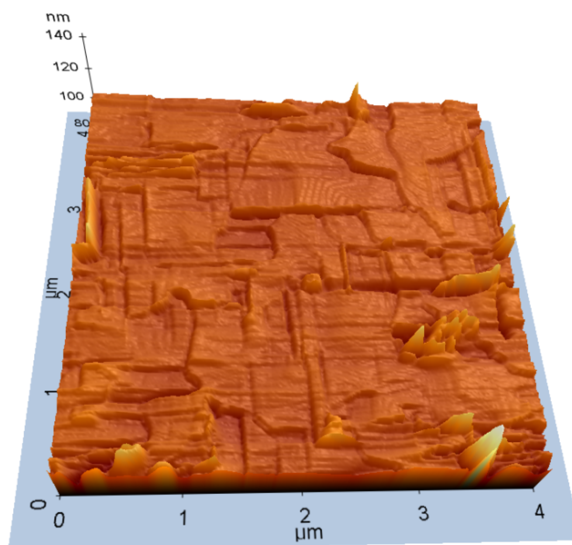

Figure 23. Presence of anti-phase domains on AlSb grown on Silicon.

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3.4. Results and Discussion

A comparison of the values for the InAs and the InGaSb channels is shown in Figure 24, Tables 2 and 3. As expected the n-type channel has significantly higher electron mobility at both 77K and 300K compared to the p-type InGaSb channel. These are expected values for InGaSb and can also be improved by increasing the strain in the channel. The channel used for this study has 20% Indium, however this can be increased to as much as 45% without significant deterioration of the semiconductor. The increased pseudomorphic compressive strain also leads to the splitting of the heavy hole –light hole bands and results in increased hole mobility.

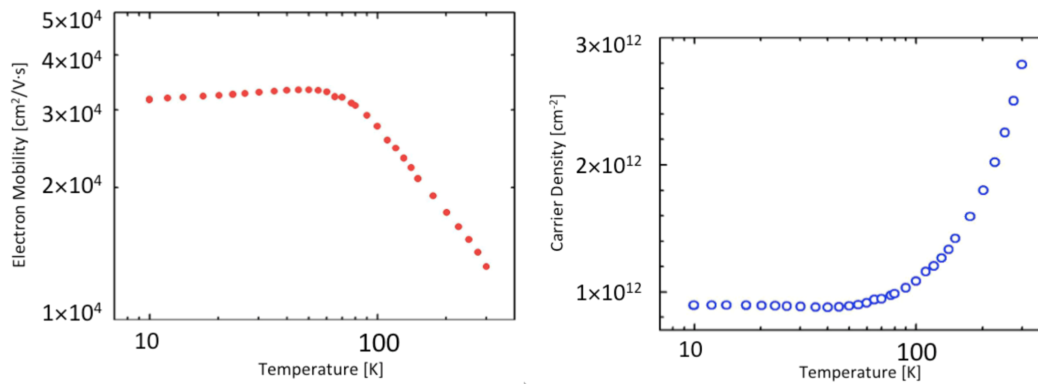

Figure 24. Plots showing electron mobility and the carrier density as a function of temperature for the InAs *n*-type channel.

Table 2. Mobility and Carrier density for *n*-type InAs channel.

T (K)	Carrier Density [cm^{-2}]	Mobility [cm^2/Vs]
300 K	2.79×10^{12}	13230
77 K	9.74×10^{11}	31130

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Table 3. Mobility and Carrier density for *p*-type InGaSb channel.

T (K)	Carrier Density [cm^{-2}]	Mobility [cm^2/Vs]
300 K	1.5×10^{12}	595
77 K	8×10^{11}	2850

3.5. Conclusion

We have demonstrated the growth of low-defect density and high quality III-Sb epi-layers on GaAs and Silicon substrates. The growth of these highly mismatched layers is based on the formation of interfacial misfit dislocation arrays which results in spontaneously relaxed III-Sb growth on GaAs and Si. On GaAs we have made use of InAs channels for electron transport and InGaSb pseudomorphic channels for hole transport. The mobility for the electrons peaks at 77K at a value of ~ 32,000 cm^2/V.sec with a room temperature mobility of ~ 13,000 cm^2/V.sec. The mobility for the holes at 77K is ~ 2850 cm^2/V.sec with a room temperature mobility of ~ 595 cm^2/V.sec.

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List of Acronyms

2D	two-dimensional
AFRL	Air Force Research Laboratory
Al	aluminum
Al_2O_3	aluminum oxide
AlGaSb	aluminum gallium antimonide
AlSb	aluminum antimonide
APD	anti-phase domains
Au	gold
CMOS	complementary metal-oxide semiconductor
C-V	capacitance-voltage
FET	field-effect transistor
FIB	focused ion beam
GaAs	gallium arsenide
GaSb	gallium antimonide
Ge	germanium
HF	hydrogen fluoride
HO	hydrolyzation oxidation
III	element from column III of the periodic table
IMF	interfacial misfit array
In	indium
InAs	indium arsenide
InGaAs	indium gallium arsenide
InGaSb	indium gallium antimonide
IV	element from column V of the periodic table
I-V	current - voltage
I_d	source-drain current
LHO	lateral hydrolyzation oxidation
LPCEO	liquid phase chemical-enhanced oxidation
MBE	molecular beam epitaxy
MESFET	metal-semiconductor field effect transistor
MLs	monlayers
MOSFET	metal-oxide semiconductor field effect transistor
Ni	nickel
NW	nanowire
PECVD	plasma-enhanced chemical vapor deposition
RHEED	reflective high energy electron diffraction
SAE	selective-area epitaxy
Si	silicon

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Si_3N_4	silicon nitride
SOI	semiconductor on insulator
STEM	scanning tunneling electron microscopy
TEM	transmission electron microscope
Ti	titanium
VLS	vapor-liquid-solid
V_d	drain voltage
V_g	gate voltage

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