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Alessandro De Gloria
Editor

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Preface

This is the sixth edition of the Apple pies Conference, held in Rome, Italy on 21–22 September 2017. The conference aims at offering a wide and reasoned overview of Electronic applications in several domains, demonstrating how Electronics has become pervasive and ever more embedded in everyday objects and processes.

The computational, storage and communication power of current electronic systems is such that we may really say that their applications are limited only by the designer's fantasy. This represents a great challenge for practitioners, managers and academicians in ICT Engineering. The challenge also stresses the importance of multidisciplinary knowledge, expertise and collaboration, in order to support a virtuous iterative cycle from user needs to new products and services. The cycle goes through the whole system engineering process, which typically encompasses requirement elicitation, specification management, software and hardware design, lab and user testing and verification, maintenance management.

For either an Embedded or Cyberphysical System to be successful in the current globalized market competition, at least one of the following features must be provided: innovation, high performance, good cost/performance ratio. Designing and implementing each one of such features requires a deep knowledge of both the system's target application and domain, and of the technologies that are potentially able to fulfill the expected goals.

One of the most important factors for the success of a project consists in the adoption of a suited design flow and related tools. Only seldom are simple top-down or bottom-up methods able to meet the time and cost-related challenges of nowadays market scenarios. Even if every application stems from recognizing one or more key user needs, a proper design, implementation and maintenance require mastering the most suited technologies and tools in order to support efficient and effective development and life-cycle management of electronics applications. Support tools must also be able to capture and share a team's experience in the design and implementation process, as it allows anticipating possible problems that may not appear on the paper.

All these challenging aspects call for the importance of the role of the University as a place where new generation designers can learn and practice with cutting-the-edge technological tools and are stimulated to devise solutions for challenges coming from a variety of application domains, such as health care, transportation, education, tourism, entertainment, cultural heritage, energy.

This conference wants to report and discuss several examples of designs and become a reference point in the field of electronics systems design, trying to fill at scientific and technological R&D level a gap that the most farsighted industries have already indicated and are striving to cover.

Genoa, Italy Alessandro De Gloria

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A Wireless Sensor Node for Acoustic Emission Non-destructive Testing

Gian Carlo Cardarilli, Luca Di Nunzio, Federico Massimi, Rocco Fazzolari, Carlo De Petris, Giuseppe Augugliaro and Canio Mennuti

Abstract In this paper a wireless sensor node for Acoustic Emission (AE) analysis has been proposed. This node can be used to simplify the in-force procedures for the structural integrity verification of pressure tanks. This procedure is currently based on periodic checks and consequently does not allow a real-time monitoring. The proposed wireless sensor node is compatible with commonly used AE sensors available on market and can be integrated in a wireless sensor network for real time monitoring increasing the security of the plant.

Keywords Acoustic Emission · Non-Destructive testing · WSN

1 Introduction

The Acoustic Emission (AE) method is a commonly applied Non-Destructive (ND) technique used to detect faults in mechanically loaded structures and components. If a structure is subjected to mechanical load or stress, the presence of discontinuity releases energy as acoustic emissions. The AE method allows to check the integrity of a wide variety of structures analyzing data coming from piezoelectric sensors. One of the most common application field is the check of structural integrity of pressure tanks. In some countries (for example in Italy), the current legislation provides for the use of this technique. The current AE method protocol is based on periodic checks that do not allow a continuous monitoring and it uses a very unwieldy instrumentation. For this reason, authors propose a new approach based on the use of a

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Wireless Sensor Network (WSN) [1]. A WSN is a wireless network consisting of spatially distributed autonomous devices using sensors for monitoring physical or environmental conditions. WSNs are used in different applications as health care, utilities, and remote monitoring [2–4]. The use of WSN allows two main advantages: the first one is the possibility to have a real-time monitoring and the second one is the use of a less bulky equipment. A traditional WSN architecture (see Fig. 1) is composed of wireless sensor nodes, one or more gateways and a server. In case of WSN for AE, the wireless sensor nodes detect the presence of an acoustic emission and provide information about the emissions to the nearest gateway.

The gateway collects information by the wireless sensor node and sends them to a web server accessible from outside using a common web browser. If the size of the network, in terms of number of nodes, is small, a single device can be used as gateway and server. The wireless sensor nodes could be located in places where a wired power supply is not available. The impossibility to be reached by power supply implies two possible solutions: the use of batteries or the use of energy harvesting techniques [5]. In any case considering these energy issues, it is necessary to optimize the node in order to consume the minimum possible quantity of energy. For this reason, the sensor node represents the critical element of the entire WSN. In this paper, authors present a wireless sensor node for the AE diagnostic method. The node allows the real-time monitoring and detection of faults and the wireless transmission of AE signal features.

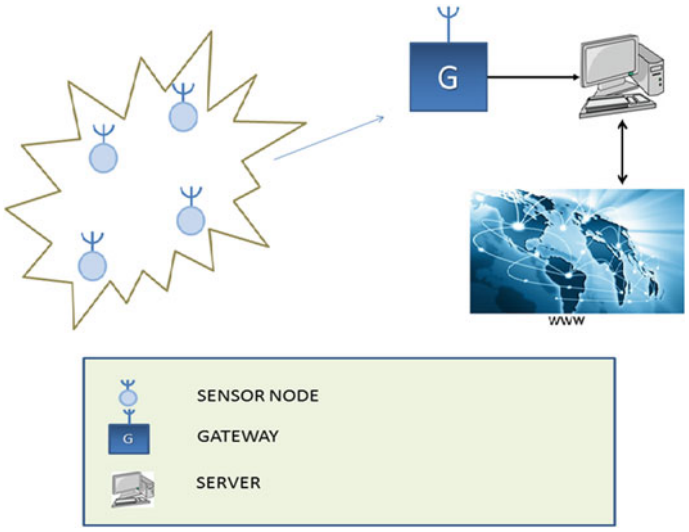

Fig. 1 Wireless sensor networks architecture

2 Acoustic Emission: Wireless Consideration

AE refers to the generation of transient elastic waves generated by a sudden redistribution of stress in a material (see Fig. 2). The analysis of these AE waves allows to both detect and locate damage on structures. This method uses specific piezoelectric sensors for the AE detection and electronic systems for the signal processing. AE signal analysis is performed considering four basic parameters of AE waves: Amplitude, Duration, Energy, Zero Crossing [6]. As introduced above, the current AE protocol is based on manual periodic checks that do not allow a continuous monitoring and uses a very unwieldy instrumentation (see Fig. 3).

The periodic checks are based on the installation of AE sensors on the structure that must be monitored. These sensors are wired connected with an electronic system that analyzes data coming from different sensors in terms of Amplitude, Duration, Energy, Zero Crossing. This approach does not allow the possibility to have a real-time monitoring on the structure since all tasks are manually done by specialized operators. For this reason, the use of a WSN allows a real-time system monitoring. The critical aspect in the realization of the WSN is the design of the sensor node. This is because it can be located in places where the wired power supply is not available and consequently it is necessary the use of batteries. For this reason, the sensor node must be optimized in terms of power consumption.

The wireless transmission heavily impacts on the power consumption. Wideband protocols allow the transmission of a big amount of data but require lots of power [7]. For this reason, it is very important to use a low energy protocol. However, the currents ultra-low-power protocols allow the transmission of few Kbit/s and this data rate does not consent the transmission of the entire AE wave in real time. This problem can be overcome providing the sensor node of a signal processing element that extracts from the signal the features useful for the AE analysis. In this way the transceiver will transmit only the signal features. For what concern the server, in this specific application no particular energy saving strategy should be used considering the limited quantity of data to process [8, 9].

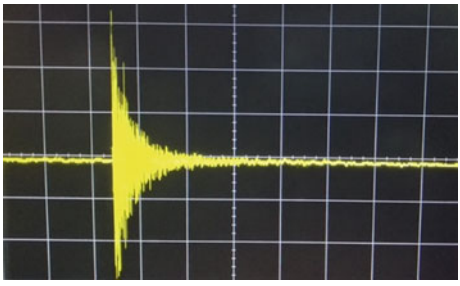

Fig. 2 Time trend of an AE wave

Fig. 3 AE method on a tank

3 Wireless Sensor Node Architecture

The wireless sensor node is composed of following subsystems:

- AE sensors
- An analog conditionig circuit
- A digital signal processing system
- A wireless transceiver

The proposed node is compatible with commercial AE sensors. Experiments has been performed on VALLEN 75S and 150S sensors [10]. The analog conditioning circuit (Fig. 4) is composed of three different sub-circuits. A variable gain amplifier, an active filter and a voltage translator. The algorithms for features extraction have been implemented on a STM32L476 by STMicroelectronics. This is an ultra-low-power microcontroller based on the high-performance ARM Cortex-M4 32-bit RISC core operating at a frequency up to 80 MHz equipped with 128 Kbyte of SRAM and three fast 12-bit ADCs working up to 5 MSPS.
The microcontroller performs the following operations:

- Analog to digital conversion of the AE signals using the microprocessor ADC.
- When signal reaches a level upon a certain threshold it begins to store it in the RAM.
- When signal reaches a level under a certain threshold the AE signal is finished, and it stops the storing operation.
- The energy, the duration, the hits count, and the max value of the stored signals are estimated.
- Results are sent to the digital transceiver using the SPI interface.

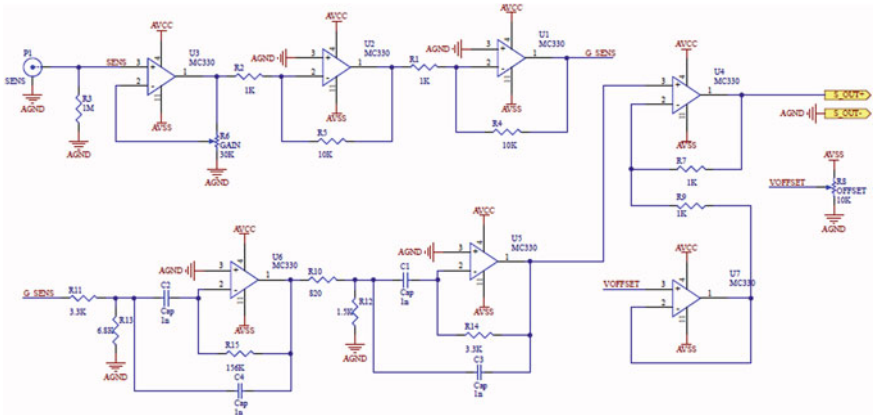

Fig. 4 Analog conditioning circuit

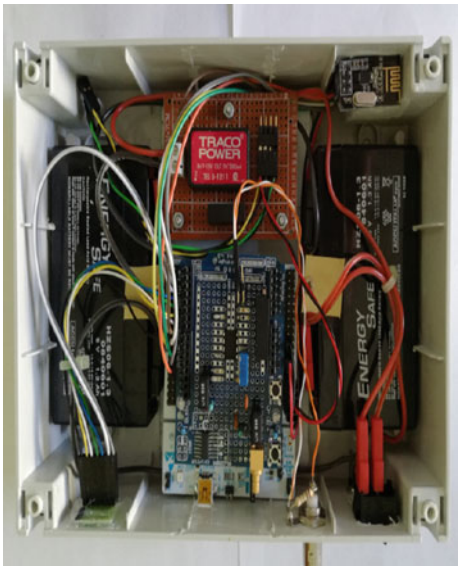

Fig. 5 The proposed AE wireless sensor node

Wireless transmission is performed by the NRF24L01 digital transceiver by Nordic Semiconductor. It is a 2,4 GHz transceiver characterized by up to 2 Mbps data-rate and an SPI interface. The complete wireless sensor node is shown in Fig. 5. Experiments have been performed using the pencil-lead break [11] method on a steel plate where the VALLEN sensors was located. The node is able to detect in real time the signal coming from the AE sensors and extract the features for the AE analysis. These features are finally transmitted to a server able to provide results on a web page Fig. 6.

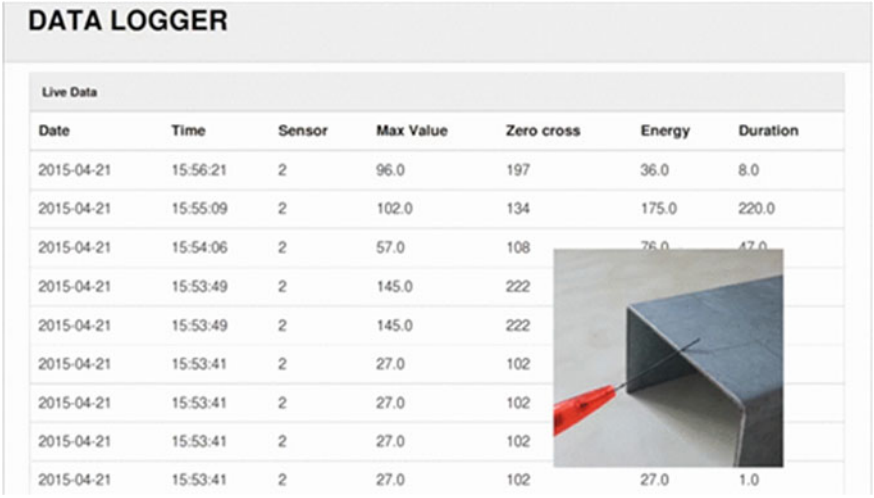

Fig. 6 AE data received from the sensor

4 Conclusions

In this paper a wireless sensor node for AE diagnostic methods has been presented. This node can be used to substitute the current manual periodic checks that do not allow a continuous monitoring and use a very unwieldy instrumentation. Authors are working to provide the sensor of the ability to localize the AE sources. This feature is very important for big structures: in case of big tanks the substitution could be difficult to realize (especially for underground tanks with length more than 100 m). For this reason, the localization of damage source circumscribes the intervention area of repair operators. A possible optimization to further reduce power consumption can be done using hardware accelerators that allow the reduction of clock frequency [12–19].

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FPGA Implementation of a Low-Power QRS Extractor

Francesca Silvestri, Simone Acciarito, Gian Carlo Cardarilli, Gaurav Mani Khanal, Luca Di Nunzio, Rocco Fazzolari and Marco Re

Abstract Among the bio-signals, the ECG is the most important waveform used for health analysis. It provides information about the heart rate, rhythm, and morphology of heart. Today, thanks to the development of advanced wearable devices, it is possible to track patient conditions outside hospital setting for several days. In such a context, the low power consumption becomes one of the crucial challenges in the development of wearable systems. In this paper, a low power implementation of Pan and Tompkins algorithm for QRS extraction is proposed. Results show that an appropriate hardware implementation significantly reduces the DSP portion power consumption of the algorithm compared with other implementation proposed in literature.

Keywords ECG QRS detection · Pan and Tompkins algorithm
Wearable computing

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1 Introduction

The electrocardiographic (ECG) signal is one of the most important bio-signals used for the analysis and monitoring of health conditions. In Fig. 1 a normal ECG signal is shown. It consists of P wave, QRS complex and T wave. Among these, the QRS complex is the most important waveform and represents the electrical activity of the heart during the ventricular contraction.

Heart disease became one of the leading causes of death worldwide [1]. Today advanced patient monitoring techniques are developed for tracking patient conditions [2, 3]. However, patients must often return to the hospital for regular check-ups. This creates considerable distress for patients and additional cost for hospitals. For this reason, in the last decade, the development of wearable devices opened several opportunities oriented to prevent the risk of occurrence of particular events [4] and monitoring health outside the hospital [5]. Since these devices are often powered using batteries, one of the most important features must be to guarantee a long service life. In the last few years, there are lots of works in literature focused on the reduction of power consumption in embedded systems [6]. Wearable systems usually are realized using dedicated hardware (ASIC) or reprogrammable devices such as microprocessors or FPGA. In this context, ASICs and FPGAs play an important role in terms of reduction of power consumption. In fact, their use allows parallel computing and consequently offers the possibility to reduce the power consumption with respect to a software solution. This is because the software is executed by microprocessors which are characterized by serial architectures.

In the automated wearable ECG monitoring systems, QRS complex is the principle wave used. The focus of this paper is the power optimization of a system implementing the QRS detection based on the Pan and Tompkins algorithm. We performed our experiments on FPGA. Many works presented in literature show a FPGA implementation of QRS systems without any information about the optimization of power consumption [7–9].

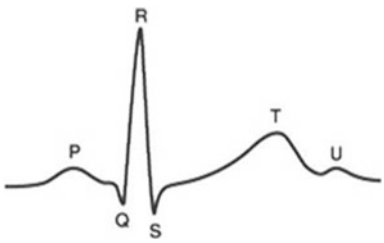

Fig. 1 ECG signal

2 Pan and Tompkins Algorithm

The Pan and Tompkins algorithm for the QRS detection is composed of a Digital Signal Processing (DSP) section and a decision circuit. The critical part, in terms of computation and consequently of power consumption, is the DSP blocks that involve the use of arithmetic circuits [10].

The first two operations of the DSP algorithm consist in the application of two IIR filters, 15 Hz low-pass filter (Eq. 1) followed by a 5 Hz high-pass filter (Eq. 2) [10].

$$y(n) = 2y(n-1) - y(n-2) + x(n) - 2x(n-6) + x(n-12) \tag{1}$$

$$y(n) = y(n-1) - \frac{1}{32}x(n) + x(n-16) - x(n-17) + \frac{1}{32}x(n-32) \tag{2}$$

The resulting band-pass filter removes noise due to power line interference, baseline wander, motion artefacts, muscle contraction and electrode contact noise. Then, the signal is differentiated as shown in Eq. 3 to find slope information.

$$y(n) = \frac{1}{8}(2x(n) + x(n-1) - x(n-3) - 2x(n-4)) \tag{3}$$

The differentiated output is then squared to maximize the amplitude difference of QRS complex with other peaks as shown in Eq. 4:

$$y(n) = [x(n)]^2 \tag{4}$$

The squared output signal passes through a moving windows integrator to smooth the signal by removing the fluctuations in signal peaks. For frequency sampling at 200 Hz the window width is typically chosen equal to 32 as shown in Eq. 5.

$$y(n) = \frac{1}{32}[y(n) + y(n-1) + \cdots + y(n-32)] \tag{5}$$

The resulting filtered ECG signal is shown in Fig. 2a. After the signal is filtered, QRS peaks are detected. The detection rules by which algorithm works, use peak height, peak location, and maximum derivative to classify peaks. When peak occurs, it is classified as either a QRS complex or noise. At each peak higher than detection threshold and classified as QRS complex, the algorithm associates a spike. It is shown in red in Fig. 2b. The detection threshold is automatically calculated using the mean estimate of the average QRS peak and the average noise peak. It is shown in green in Fig. 2b.

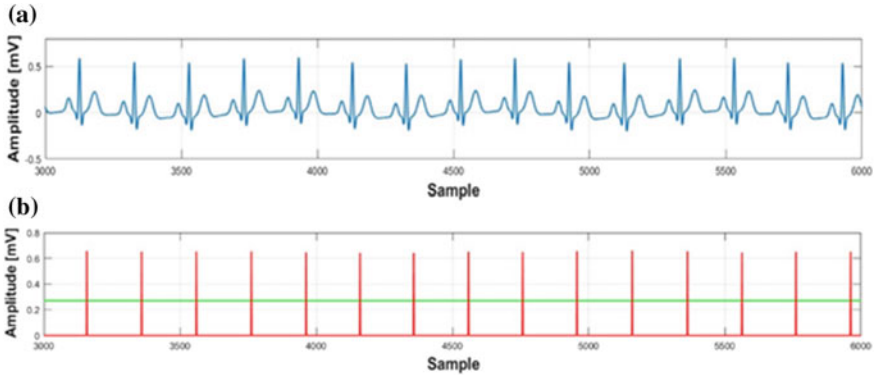

Fig. 2 In **a** is shown filtered ECG signal. In **b** are shown in red QRS detected, and in green the detection threshold

3 Fixed Point Analysis

The first step for the power consumption optimization consists in the fixed point analysis of the algorithm. All previous FPGA implementations presented in literature did not optimize bits number of the DSP circuits, and consequently area and power consumption [7–9].

Fixed point analysis is performed in MATLAB/Simulink (Fig. 3). The optimization is realized reducing as much as possible the bit number of input data, coefficients of the filters and the processing elements (adders and multipliers), without compromising the algorithm functionality. Experiments are performed providing as input of the model the data from the MIT-BIH ECG database. It contains 48 half-hours of ambulatory ECG recordings [11].

The fixed point analysis started considering 16 bits for the input data and for any coefficient of the IIR filters. This number is chosen considering previous FPGA implementation. The choice of size of multipliers is made taking into consideration

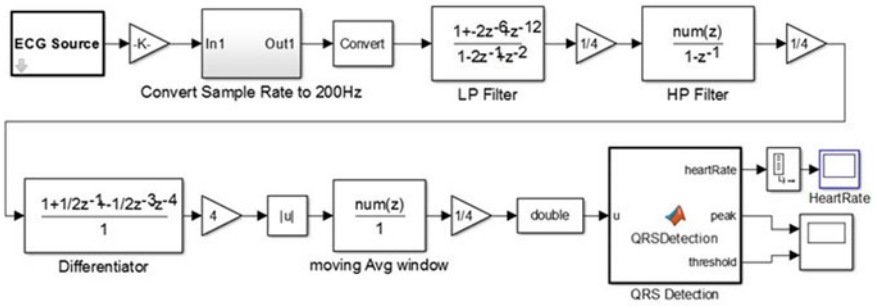

Fig. 3 Simulink fixed point model

Table 1 Coefficients bit number of filters

Filters	Num bit coeff	Den bit coeff
Low-pass	2	2
High-pass	7	2
Differentiator	3	–

bit number of coefficients and data. Previous FPGA implementation uses DSP blocks to realize multiplications [7–9]. However, if we consider that the filter coefficients are the power of two, it is possible to replace the DSP block with shifters, reducing hardware resources and power consumption. The least number of bits (relative to the filter coefficients) that can ensure the correct functioning of the algorithm is shown in Table 1. The simulation shows that the least bit number for the input is 4 bits.

4 Experimental Results

After the fixed point analysis, we described the system in VHDL and we implemented it on a XILINX artix FPGA. We performed the synthesis and the Place & Route using the VIVADO IDE. We estimated the power consumption during the post Place & Route simulation using as input the data coming from the MIT-BIH ECG database. In Table 2 hardware resources utilization is provided, whereas in Table 3 the power consumption is shown. Experiments are performed reducing the number of bits input (and consequently of all the processing elements involved in computation) from 16 bits to 4 bits that are the minimum number, as explained in the previous section. For the implementation of multi- plications, we performed measurements both using DSP blocks and shifters. The power consumption is reduced to about a factor 10 and area by a factor 2.

Table 2 Hardware resources

Bit input	Bit coeff	TYP	FF	IO	DSP	SliceL	SliceM
16	16	Mult	297	35	7	47	50
“	“	Shift	276	35	0	43	42
12	12	Mult	233	27	7	35	37
“	“	Shift	215	27	0	35	35
8	8	Mult	166	19	7	27	29
“	“	Shift	162	19	0	24	26
4	*Optimum case*	Shift	145	12	0	24	26

Table 3 Power consumption

Bit Input	Bit Coeff	DSP	Power (mW)
16	16	YES	39
"	"	NO	31
12	12	YES	28
"	"	NO	22
8	8	YES	17
"	"	NO	13
4	*Optimum case*	NO	4

5 Conclusion

In this paper, we proposed a low power hardware implementation of the Pan and Tompkins algorithm for the QRS extraction. Results show that hardware optimization significantly reduces power consumption. Reducing the number of bits at the input and replacing multipliers with shifters, we halved the occupied area avoiding the use of DSP blocks. The power consumption of the obtained system decreased of factor 10 with respect to the initial setup. The initial setup is based on other implementations proposed in the literature. In the future, it could be interesting to analyze power consumption by implementing the algorithm using a mixed approach based on SW and HW as show in [12–17].

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Digital Architecture of Next Generation Spacecraft Tracker Based on Wideband ΔDOR

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Abstract Tracking signals of an interplanetary spacecraft are distorted by various deep space noise sources and receiver imperfections. In recent years, a new technique called *Wideband Delta Direct One-Way Ranging*, based on broadband probe signals, was developed. This research work provides an architecture upgrade for the ESA X/Ka Deep Space Transponder, that supports the generation of Wideband DDOR signals. This implementation is envisaged to greatly improve the spacecraft tracking performance and unlock future missions requiring 1 nrad level of angular position accuracy.

Keywords WDDOR · Spacecraft tracking · On-board processing · FPGA

1 Introduction

Nowadays state-of-art spacecraft tracking techniques include Doppler, Ranging, and *Delta Direct One-Way Ranging* (*Δ*DOR) [1]. While the accuracy of the first two directly relies on the SC signal observation time, performance of a *Δ*DOR measurement depends, theoretically, only on the position of the SC and earth antennas [2]. The *Δ*DOR [3] tracking method is a type of Very Long Baseline Interferometry (*VLBI*) technique [4]. It calculates a SC angular position by differentiating (*Delta*) the Direct One-Way Range (*DOR*) measurements of the target probe and a reference quasar close in terms of angular range (<10°). This difference is a calibration by which several common mode errors are cancelled or heavily attenuated. A schematic representation is shown in Fig. 1. A single DOR measurement consists in assessing the time of arrival delay of a signal at two very distant earth antennas. In 2005 [2]

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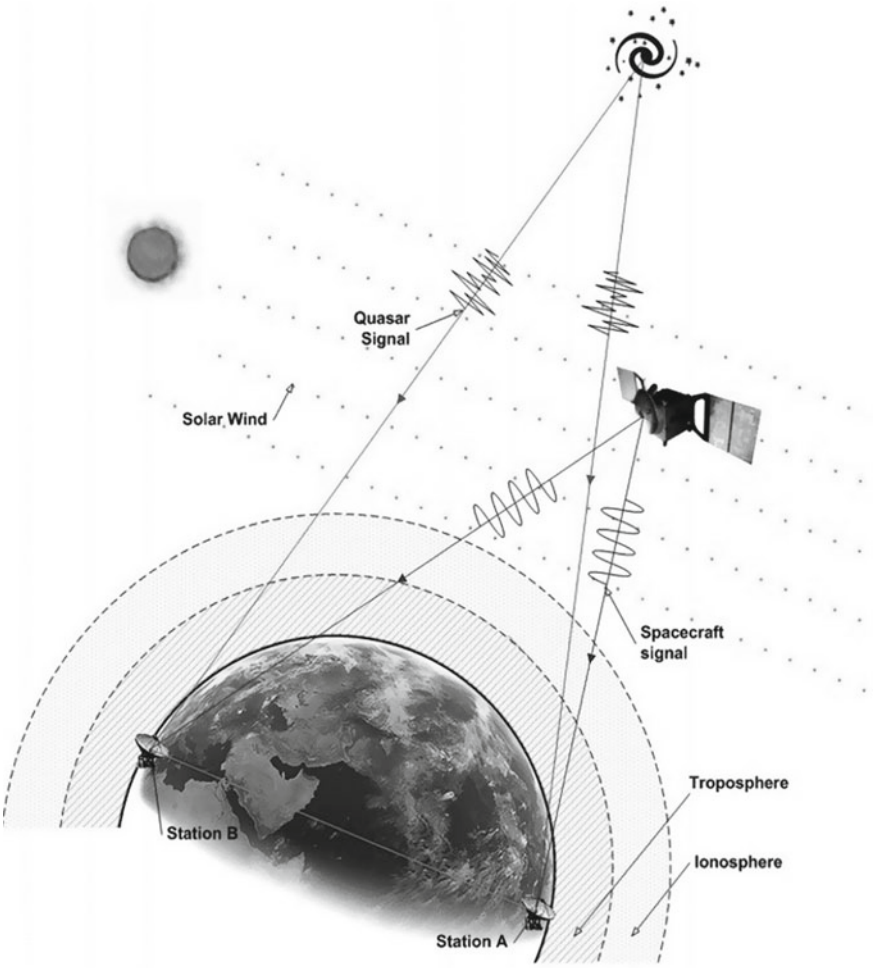

Fig. 1 ΔDOR geometry

the European Space Agency begun employ its own *Narrowband Δ*DOR system in the deep-space tracking network [5], making use of pure tones as spacecraft DOR observables. An evaluation of the *Δ*DOR error budget was undertaken in the frame of the ASTRA activity (*Interdisciplinary study on enhancement of end-to-end Accuracy for Spacecraft TRAcking techniques)* [6]. The main error sources are:

- Thermal noise in the received SC and quasar signal;
- Uncalibrated propagation media, introducing systematic and random errors;
- Phase non-linearities in the recording bandwidth.

Phase errors are caused by the receiver non-linearities, especially at the L-band downconverter RF section. Moreover, due to the different nature of the received sig-

nals (a broadband noise-like quasar signal and narrowband SC tones), *phase ripple* phenomena induce systematic phase errors [7]. Current and past ESA missions, such as *Mars Express*, *Venus Express* and *Rosetta*, do not have a dedicated DOR tone generator inside the Deep Space Transponder. Telemetry subcarrier harmonics (up to the 20th order) are employed and operate as DOR tones, although their amplitude is low and the total spanned bandwidth cannot be larger than 10 MHz [8]. The ESA Narrowband ΔDOR level of accuracy has been measured with spacecraft data collected during the Rosetta mission, and settles in the range of 10–15 nrad of uncertainty ellipse [9]. This accuracy will not be sufficient for future missions that will demand higher navigation requirements. For example, a direct planet landing or a narrow trajectory for an orbit insertion will require an estimated error below 1 nrad [10]. According to [11], *Wideband* DOR dedicated signals by means of pseudo-noise (PN) shall be used to decrease the probe and quasar phase dispersion differences in the downconverter section. This allows a *better phase ripple calibration* that makes the 1nrad level of accuracy possible. A previous research [10] presents a software testing environment that simulates the design of a *Wideband ΔDOR* communication link, showing that such accuracy can be achieved. The assessed phase ripple level of calibration depends on the SC channel bandwidth set by the PN *Chip Rate*, the portion of spanned recorded bandwidth, and signal roll-off thin the channels. In this research a system architecture for a future circuit implementation of a Wideband ΔDOR signal generator is presented.

2 Wideband ΔDOR Signal Generator Architecture

The consolidated modulation methods after BepiColombo X/Ka Deep Space Transponder [12], the upgrade from a Narrowband to a Wideband ΔDOR method will require a dedicated phase modulation scheme by means of pseudo-noise for the DOR subcarriers. The downlink signal model is presented in Eq. (1), where the summation terms within the downlink phase represent the spreading signals for the Wideband ΔDOR

$$s_{dl}(t) = A \sin\left[2\pi f_c t + TC(t) + \sum_{i=1}^{N} \phi_i PN_i \sin(2\pi f_i t)\right]. \quad (1)$$

A hardware upgrade to the ESA X/Ka-DST Digital Module is needed for the Wideband ΔDOR compatibility. The spreading signals are generated by a pseudo-noise modulator consisting of a multirate Digital Signal Processor. Mode switches for Narrowband ΔDOR compatibility are also present. A total of three PN codes are baseband modulated with a Non-Return-to-Zero (*NRZ*) decoder and two Root Raised Cosine (*RRC*) shaping FIR filters. Two NCOs generate two subcarriers. This multirate system requires an additional interpolation filter to adjust the sampling

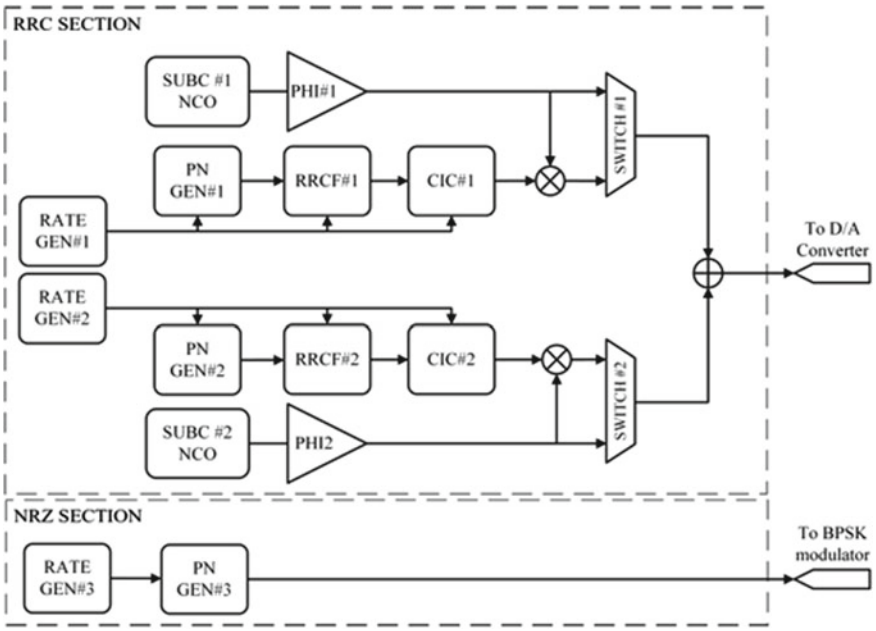

Fig. 2 Wideband ΔDOR architecture

rate at the sub- carrier section. CIC filters are suitable for this task because the only transfer function requirement is a linear phase.

Specifications: The X/Ka-DST hardware upgrade design specifications are given in [10], taking the TC subcarrier $F_1 = 9.6$ MHz as a reference frequency. The maximum sampling rate, i.e. the system clock frequency, is set at $8F_1$. The spreading signals are of two types: a baseband balanced Non-Return to Zero shaped signal, which is used for the 8F1 subcarrier BPSK modulation in the Ka-band transmitter analog section and a couple of baseband *Root Raised Cosine* shaped signals that modulate the $F_1/2$ and $2F_1$ numeric subcarriers in amplitude within the digital domain. These RRC signals modulate the relevant RF carriers in both X and Ka band transmitter modules of the transponder. The *RRC* spreading signals are converted by a 10-bit DAC and provided to the analog section. The PN Code are Gold sequences 2048 chips long. The possible Chip Rates (R_c) are: $F_1/2$, $F_1/3$, $F_1/4$ and $F_1/8$, and determine the channel width. Both NRZ and RRC signals are used as phase modulation components for the downlink signals. The whole set of system parameters must be reconfigurable and backwards compatible with systems relying on Narrowband Delta-DOR signals. A support circuit to control and reconfigure the Wideband ΔDOR Digital Signal Processor inside the Digital Module is envisaged for future FPGA implementation of the prototype.

Architecture: As shown in Fig. 2, the multirate digital signal processor requires the following building blocks:

NRZ and RRC channels

- Three independent *Sampling rate controllers, Rate Gen*;
- Three different *Pseudo Noise Generators*, in the form of Gold Code synthesizers, based on LFSRs;

RRC shaped channels only

- Two chip shaping *FIR filters, RRCF*, in a transposed serial polyphase structure;
- Two *CIC interpolation filters*, needed for the baseband signal to match the subcarrier sampling rate, made by 4 comb and integrator sections;
- Two distinct *Subcarrier NCOs;*
- Two *variable attenuators*, providing the needed modulation indexes;
- One *multi-channel modulator*, i.e. multipliers and an adder, to modulate the subcarriers and combine the broadband signals centered at $F_1/2$ and $2F_1$;
- Two *Channel Mode Switches*, that select the needed data path for the backwards compatibility with the currently existing Narrowband ΔDOR systems.

Current research [13] presents optimized fast memory-based numeric oscillators, but in the case of this research work a memoryless CORDIC structure is preferred as a future space compatible circuit implementation is envisaged.

3 Experimental Results

The system executes an algorithm that was simulated in the *MATLAB-Simulink* environment. Several tests have been run with different sets of parameters. In first place, Floating-Point arithmetic (FLP) was employed to consolidate and validate the Wideband ΔDOR signal generation algorithm. During a second phase, the algorithms were performed and analyzed in a Fixed-Point simulation environment (FXP). The NRZ and RRC power spectrum densities (PSD) are shown in Figs. 3 and 4, in the cases of $R_c = F_1/2$.

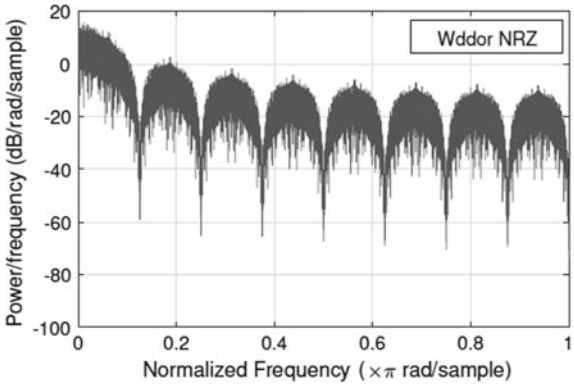

Fig. 3 NRZ channel FLP, $R_c = F_1/2$

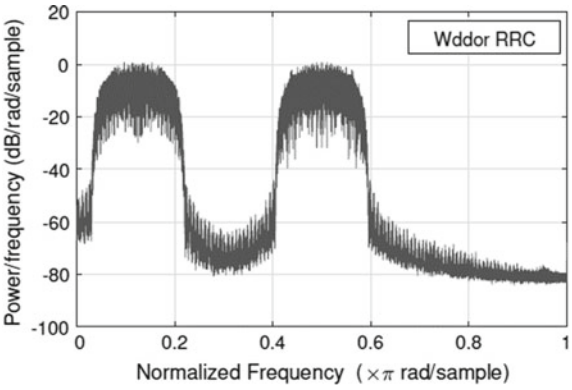

Fig. 4 RRC channels FLP, $R_c = F_1/2$

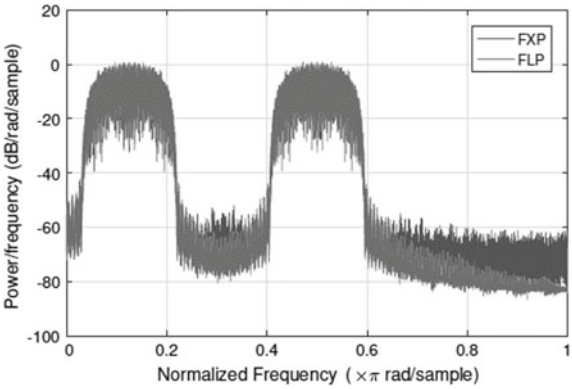

Fig. 5 FXP/FLP PSD comparison

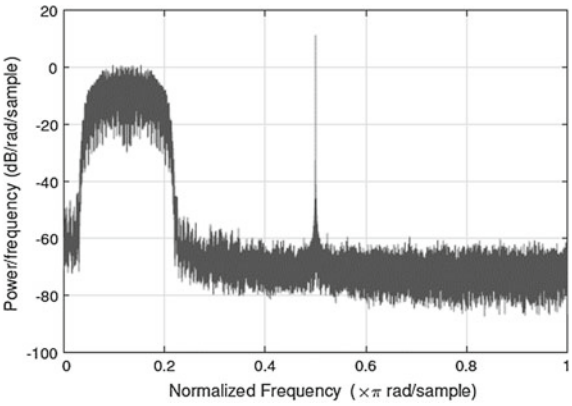

Fig. 6 Wideband and narrowband DOR signals

The Fixed-Point design required a 2-bit NRZ output register and a 10-bit for the RRC one. The expected Signal to Quantization Noise Ratio (SQNR) is approximately 60 dB for the 10-bit output. The CIC interpolation filter design is critical because the convergence of its algorithm depends on its register sizes. Since integrators are IIR filters, prone to overflow or saturation phenomena, they have been designed according to the mathematical criteria stated in [14] to obtain the safe register lengths. In the following Fig. 5, FLP and FXP relevant PSDs are superimposed to show the implementation loss. The FXP NRZ channel spectrum is the same as the FLP one. In Fig. 6 the narrowband ΔDOR signal generation capability is shown.

4 Conclusions

In this paper authors presented a system architectureof the Wideband ΔDOR The complete set of specifications prompted by cited researches has been met in a simulation environment, using Floating and Fixed-Point arithmetic. The generation of two types of phase modulating signals (NRZ and RRC) required the use of a tight set of different digital signal processing blocks, in the form of Rate Controllers, LSFRs, Root Raised Cosine FIR filters, CIC interpolation filters, Subcarrier CORDICs, adders and very few multipliers. The generated spectra, for RRC channels, provide the expected SQNR of 60 dB. A mixed Hardware Software implementation is actually under development. As shown in [15–18], mixed Hw/Sw approach can be useful to obtain high performance in terms of clock frequency and and maintain the ease of use typical of microprocessors. In order to mitigate the system respect to radiation, error detection techniques will be introduced [19]

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FPGA Implementation of a Channelizer with 2048 Channels Utilizing USRP-SDR Platform for Satellite Communications

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Abstract This paper presents an FPGA implementation of a channelizer based on digital filter bank with 2048 channels for satellite communications. The proposed architecture was simulated in Simulink and implemented on a Kintex-7 FPGA. The design was tested with a Universal Software Radio Peripheral (USRP).

Keywords Channelizer · Polyphase filter banks · Software Defined Radio

1 Introduction

Wireless communications are characterized by several standards and protocols constantly evolving. Typically, the common approach for processing this kind of data, is based on the use of a dedicated architectures developed for the application specific receiver. This approach leads to structures characterized by reduced flexibility and, in general, not compatible with the different standards. In the last decades, there is increasing interest to develop platforms that are able to work with different protocols. The most common example are the platforms based on Software Defined Radio (SDR) technology [1, 2]. A SDR-based system can be used to process at the same time different types of signals with different bands, rates, modulations, etc. One of the most important block that composes a SDR system is the receiver front-end since it must be able, for example, to extract smaller portions of band from a wideband signal. This operation is usually done using a channelizer [3, 4]. SDRs are usually implemented on Microprocessor, FPGAs or mixed architectures composed by a Microprocessor and an Hardware accelerator [5–11].

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This paper describes the implementation of a channelizer with a configurable number of channels for a SDR receiver, based on filter banks. The use of filter banks is a common approach for implementing systems able to manipulate wideband signals [12, 13]. The architecture was verified implementing a 2048 channel channelizer. It was mapped on a Xilinx Kintex-7 FGPA and finally validated with real satellite signals acquired with the Universal Software Radio Peripheral (USRP) [14, 15] by Ettus Research.

2 Channelizer Based on Filter Banks

The most common way to implement a channelizer is through the use of *analysis filter banks*. An analysis filter bank is a set of filters used for the decomposition of wideband signals. It allows the decomposition of the input signal into a set of M sub-bands, where each sub-band contains a portion of the original wideband spectrum. In the following sections, different channelizer architectures are discussed and analyzed in terms of hardware complexity and performances.

2.1 Parallel Implementation

The realization of a filter bank can be much expensive in terms of resources, since each filter should have the same order of the prototype filter $H_0(z)$ [16]. As an alternative to use a set of independent filters, the filter bank can be developed with a polyphase structure that optimizes the computation [17–19]. This new structure is composed by the prototype filter and a Parallel IDFT. Prototype filter must be a causal low-pass filter with a cut-off frequency smaller than π/M(where M is the number of sub-bands) and a real impulse response $h_0[n]$. The prototype filter is expanded in the polyphase form:

$$H_0(z) = \sum_{l=0}^{M-1} z^{-l} E_l\left(z^M\right)$$

where $E_l(z)$ is the polyphase component of $H_0(z)$:

$$E_l(z) = \sum_{n=0}^{\infty} h_0[l + nM]z^{-n}, \quad 0 \leq l \leq M-1$$

The multistage structure is shown in Fig. 1.
The passband filters can represented by the following matrix expression:

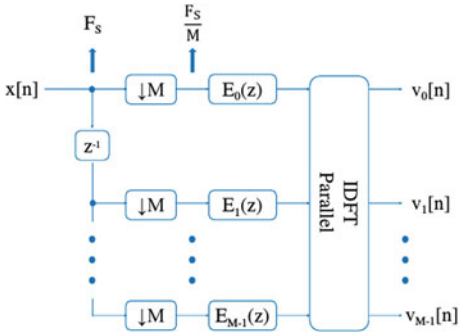

Fig. 1 Multistage implementation of digital filter bank

$$\begin{bmatrix} H_0(z) \\ H_1(z) \\ H_2(z) \\ \vdots \\ H_{M-1}(z) \end{bmatrix} = M\mathbf{D}^{-1} \begin{bmatrix} E_0(z^M) \\ z^{-1}E_1(z^M) \\ z^{-2}E_2(z^M) \\ \vdots \\ z^{-(M-1)}E_{M-1}(z^M) \end{bmatrix}$$

where **D** is the DFT matrix. The computational complexity of the multistage structure is much smaller of an independent filter implementation, because the filter bank based on a N-tap prototype filter and a M-point DFT (implemented using radix-2 FFT algorithm) requires $log_2(M + N)$ multipliers, whereas a direct implementation requires NM multiplications.

2.2 Serial Implementation

If data arrive serially to the filter bank the architecture shown in the previous section can be modified using a serial structure (obtaining some benefits in terms of area). This solution is shown in Fig. 2:

The input coefficients of the multipliers change at each cycle of clock and the output of filter, at each clock cycle, is equal to the polyphase component.

The output of the polyphase component is equal to $y_k[n] = x_k[n] \circledast h_k[n]$ where $x_k[n]$ and $h_k[n]$ are obtained from the polyphase decomposition:

$$x_{k[n]} = x[Mn + k],\ h_{k[n]} = h[Mn + k]$$

Let us assume $k = \langle n \rangle_M$ (where $\langle n \rangle_M$ represents the operation n modulo M) with $0 \leq k \leq M - 1$, the output of filter is given by:

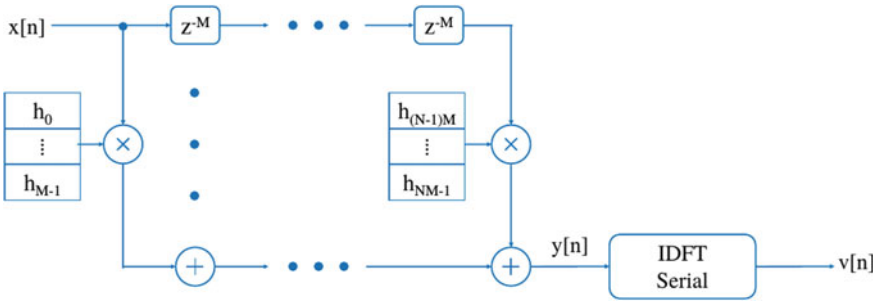

Fig. 2 Serial implementation of digital filter bank

$$y[n] = y_k[n] = y_{\langle n \rangle_M}[n]$$

Therefore, the output of system is:

$$\begin{bmatrix} v[0] \\ v[1] \\ \vdots \\ v[M-1] \end{bmatrix} = M\boldsymbol{D}^{-1} \begin{bmatrix} y[0] \\ y[1] \\ \vdots \\ y[M-1] \end{bmatrix}$$

The computational complexity of the filter is equal to N/M and the total computation complexity is $(M/2)\log_2 M + (N/M)$, using radix-2 FFT algorithm for the implementation of the M-point DFT.

3 Implementation, Test and Results

The channelizer functionality has been verified through fixed-point Simulink simulations. The Simulink model was simulated using real signals coming from a satellite for *Mobile Satellite Services*. For this purpose, we used the USRP X310 with *RF Network On Chip (RFNOC)* tool by Ettus Research [14, 15].

After this validation, a flexible VHDL core has been implemented. This core allows the generation of a customizable channelizer flexible in terms of number of channels and prototype filter. In this paper a 2048 channels channelizer has been implemented, the whole input spectrum was divided into 2048 sub-bands. Implementation has been performed on a USRP X310 equipped with a Xilinx Kintex 7 FPGA. The hardware resource utilization is shown in the Table 1.

In Fig. 3 are depicted the spectrograms of a portion of input signal (left side) and one of 2048 possible outputs of channelizer (right side), in this case the channel number 463.

Table 1 Resource utilization of the only channelizer

Site type	Used	Available	Util %
Slice LUTs	20459	254200	8.05
RAMB36E1	72	795	9.06
DSP48E1	79	15400	5.13

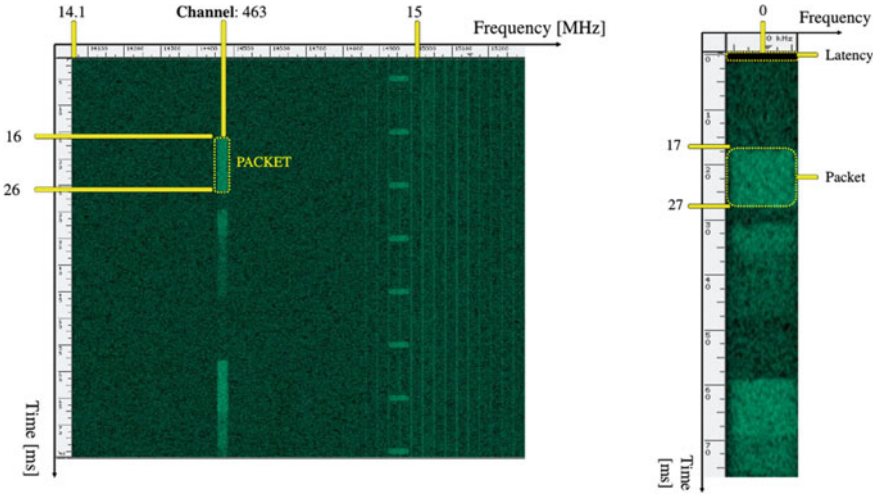

Fig. 3 The spectrogram of the input signal on the left and the spectrogram of an extract channel on the right

In the spectrogram of the input signal, the packet in the channel 463 has a duration of 10 ms (from instant 16 to 26 of the acquisition). The input signal is processed by channelizer and the packet is sent to the output about after 1 ms, this latency is dependent on the processing time (right side of Fig. 3). The input signal has a SNR value of about 25 dB and this value is unchanged also for the output signal. This means that the channelizer doesn't introduce noise.

4 Conclusions

In this paper the implementation of a 2048 channelizer for SDR applications was presented. The system was implemented on an Xilinx Kintex 7 FPGA and the tests have been carried out using real satellite signals acquired with USRP X310 device and RFNOC tool by Ettus Research. Despite the high number of channels, the implementation strategy allowed to use a very reduced number of resources. Furthermore, the VHDL structure allows to develop a channelizer with a different number of channels just changing few parameters. The tests, finally, allowed to verify that channelizer

doesn't introduce noise to the output. The future programs foresee to develop a system for aggregating any channel inside the transmitted band.

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FPGA Based Digital Lock-in Amplifier for fNIRS Systems

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Abstract Lock-In Amplifiers (LIA) represent a powerful technique helping to improve signals detectability when low signal to noise ratios are experienced. Continuous Wave functional Near Infrared Spectroscopy (CW-fNIRS) systems for e-health applications usually suffer of poor detection due to the presence of strong attenuations of the optical recovering path and therefore small signals are severely dipped in a high noise floor. In this work a digital LIA system, implemented on a Zynq® Field Programmable Gate Array (FPGA), has been designed and tested to verify the quality of the developed solution, when applied in fNIRS systems. Experimental results have shown the goodness of the proposed solutions.

Keywords Digital lock-in amplifier · FPGA · Functional near-infrared spectroscopy · Silicon Photomultiplier (SiPM)

1 Introduction

Lock-in techniques has been widely investigated and applied to many applications, spanning among very different fields, especially when there is the need to detect and measure very small signals, usually deeply immersed into high level noise.

Lock-in amplification is mainly a phase-sensitive detection technique capable to isolate a piece of the signal at a specific reference frequency and phase. Even if

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this signal is buried into noise sources many times larger, the system cuts down and strongly rejects noise signals, at frequencies other than a reference "locked-in" frequency, so they do not affect the signal measurement.

Within the e-health field, remarkable importance has been given to brain studies and recent investigations on neurology and Brain Computer Interface (BCI) have proved the benefits of functional Near-Infrared Spectroscopy (fNIRS) acquisition systems, especially when combined with simultaneous EEG traces, for better understanding the spectroscopy results [1, 2].

In [2] the system is based on double wavelength LEDs injecting infrared light into the scalp and recovering back the light, partially diffused and partially scattered, from the same surface but at a few centimeters away from the optical source, using a lock-in technique. At a proper source-detector distance, usually ranging between 2 and 3 cm, it is possible to detect optical variations of collected light and these are related, through a modified Beer-Lambert model [1], to brain activities in the form of oxygenation variations. Of course, higher numbers of sources-detectors couples (called fNIRS channels) lead to better volume resolution on the whole head, eventually ending up with a complete brain oxygenation mapping capability.

Since human scalp presents quite high attenuation values in the infrared region and it is not possible to increase the amount of impinging light for safety reasons, it is of great importance the choice of very sensitive detectors, capable to fully reach single photon counting performances. Silicon Photomultipliers (SiPM) have been then adopted since they fulfill these fierce requirements [3–5].

The main goal of this work is to design a tailored and digital version of LIA systems to be applied to a fNIRS system, in order to improve performances in signal detection and noise rejection capabilities.

2 System Architecture

As depicted in Fig. 1, it has been designed a system consisting of an fNIRS probe, a front-end board, an FPGA board (Avnet ZedBoard™ [6] in our case), and a PC for programming, data retrieving and tests. The fNIRS probe is composed by SiPM detectors (Silicon PhotoMultiplier) and dual-wavelength infrared LEDs as light sources. The front-end board is equipped with two TI ADS1298 ADC converters [7], capable to acquire signals from 16 SiPM, and a LED driver circuit that drives up to 4 LEDs. The signals coming from optical sensors are affected from flicker noise and interferences caused by ambient light and other light sources such as the neon lamps. To obtain a better SNR a digital lock-in technique has been implemented though proper LED light modulation and a signal processing chain.

The architecture of the used lock-in amplifier is the well-known dual-phase LIA [8]. It takes the input signal, modulated at a predefined and fixed frequency, and multiplies it by a generated sine and cosine reference signals, running at the same frequency of the modulated signal. The outputs are low-pass filtered with a properly designed digital filter in order to reject noise and unwanted frequency components.

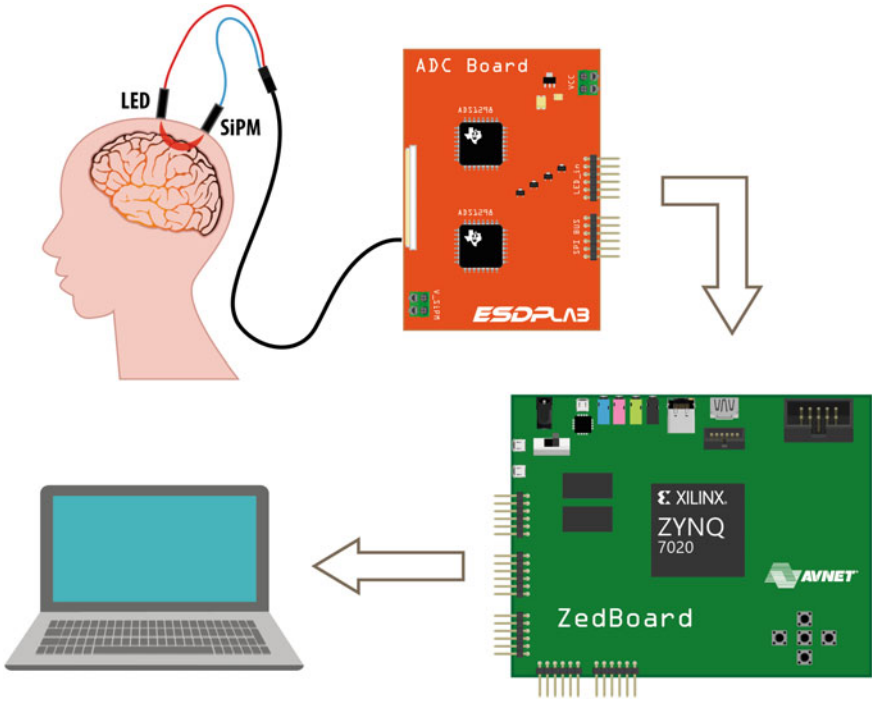

Fig. 1 Block diagram of the developed fNIRS acquisition system

The selected FPGA is the Xilinx Zynq 7020 that embeds a programmable logic section (PL) with a dual-core ARM. The processor is mainly used for data post processing and transferring to PC while in the PL hardware entities have been instantiated as shown in the block diagram (Fig. 2). This unit, named DigiLock, works as a lock-in amplifier by demodulating incoming signals and generating the reference lock-in frequency. The tasks of the fNIRS core are: collecting data from ADC converters through a dedicated ADC driver, managing time-sharing of optical channels and sending ADC samples to DigiLock. When DigiLock processes a new data set it will send it to the ARM processor via a hardware implemented Block RAM. More details regarding the DigiLock design process and architecture can be found in [9].

In fNIRS systems LED sources must not be simultaneously activated in order to avoid interference among different channels. So, it's very important to develop a time-sharing scheme that's properly manages the activation of light sources once at a time. The LED driver has been designed to implement a simple time sharing yet configurable scheme, depending on total number of sources and detectors. Figure 3 shows the implemented time sharing scheme limited to two LED sources. The switch between different sources is activated on the rising edge of a reference signal (REF), properly generated by DigiLock at lock-in frequency. SEL and BASE ADDRESS signals are used by DigiLock to select the set of registers and the internal memory

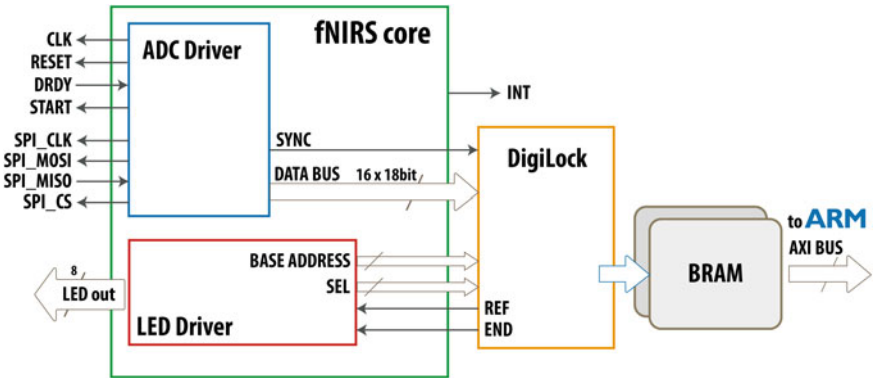

Fig. 2 Block diagram of the VHDL entities in the FPGA

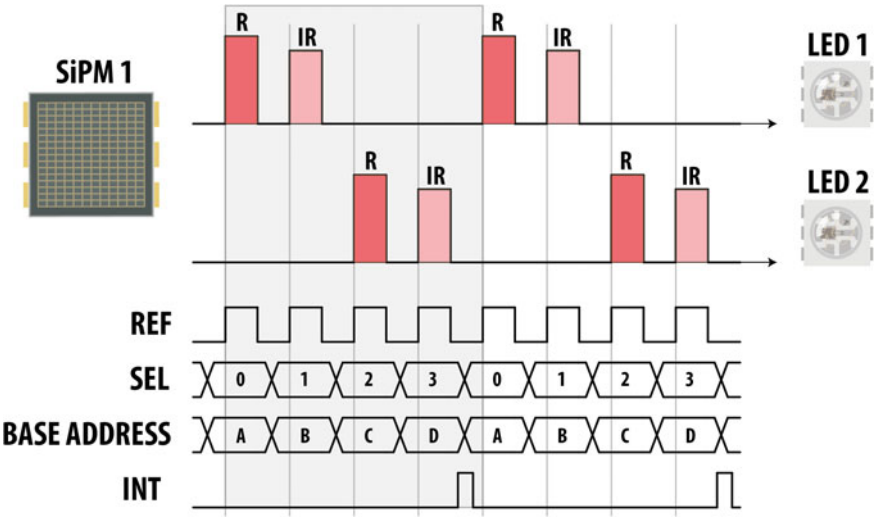

Fig. 3 Temporal diagram of the time-sharing scheme and an excerpt of related control signals

bank to be used. As it can be seen a single LED source, selected in this work, is capable to emit at two different wavelengths (735 nm, named R, and 850 nm, named IR); hence two cycles of the REF signal are required, each one for the R and IR wavelengths.

When a complete scan cycle of all sources is accomplished, the DigiLock carries out the raw amplitudes and raises the INT signal to interrupt ARM processor. This process is highlighted with a grey box in the Fig. 3. The new dataset is post-processed and sent to PC via a high speed TCP/IP Ethernet connection.

In the developed system, the SiPM output signals are simultaneously acquired by using the parallel sampling feature of the selected ADC converters. In this way, a

time-sharing of the detectors is not necessary and a higher scan frequency can be achieved.

3 Experimental Results

To test the functionality of the developed fNIRS system, an experimental probe with one SiPM and one LED has been arranged to measure hemodynamic bio-signals on the pre-frontal cortex. The detector and the source have been placed at 3 cm distance and kept tightly coupled with the skin using an elastic band. In the Fig. 4 the raw detected amplitudes at two wavelengths are shown. The signal is composed by an AC part summed with a slow varying DC component that represent the useful biological signal since it is related to changes in hemoglobin concentration into the tissue. The AC component is due to the heart beat and its frequency depends on the current heart rate [10].

The combined action of lock-in technique and good design of the front-end electronics leads to a very clean and almost noise-free waveform at system output (Fig. 4). The system gets rid of the interference due to ambient light variations and other interfering light sources (e.g. neon lamps).

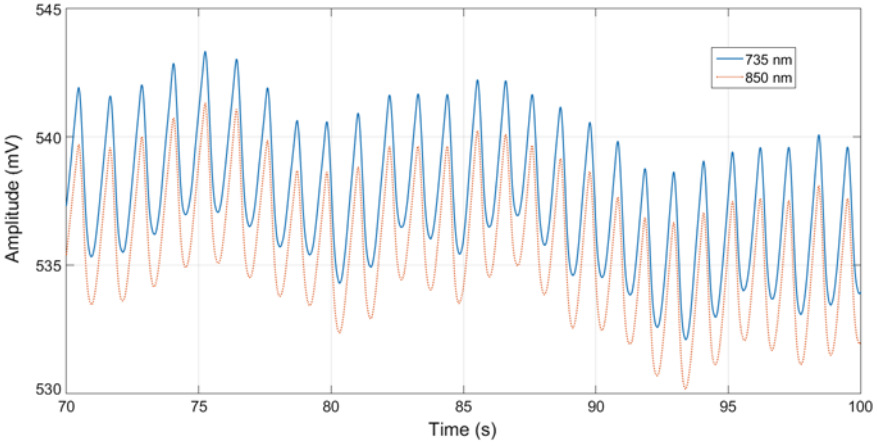

Fig. 4 Raw data waveform extracted from fNIRS system: solid line the measure at 735 nm, dotted line the measure at 850 nm. The AC component is due to heart beat while the DC offset represents the useful hemodynamic signal

4 Conclusion

In this work a CW-fNIRS system has been described and how the digital lock-in techniques, implemented within an FPGA, can be profitably applied to the fNIRS systems. The obtained signals are clean, free of ambient light and other light source interferences.

To validate the goodness of the system for hemodynamic monitoring, a deep measurement campaign is planned and an extended series of experimental tests such as: breath holding, finger tapping, visual and auditory stimulation are envisaged. These tests will led to a full medical validation in order to properly understand their physiological meaning. Up to date a few preliminary tests on breath holding have been carried out on some voluntaries, obtaining results comparable with the ones already seen in literature [2, 3]. Other investigations will be carried out in order to increase the number of implemented fNIRS channels, while leaving unchanged or furtherly improving its signal to noise ratio performances.

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A Low-Cost Smart Microwave Radar for Short Range Measurements

Alina Caddemi and Emanuele Cardillo

Abstract In this paper, the design and development of a smart microwave radar is described. The system has been designed with the aim of realizing a cost-effective flexible radar, capable of detecting short-range targets (within 5 m) and suitable for the integration in different scenarios. The miniaturization of the radar has been possible by working within the available ISM band extending from 24 to 25 GHz. A pulsed chirp has been used to achieve a high resolution (up to 15 cm with a 1 GHz chirp bandwidth). In addition, the transmitted signal has been pulsed thus achieving a lower power consumption. A system prototype has been realized and several tests have been carried out for confirming the expected performance.

Keywords Short-range radar · Microwaves · Frequency modulation · ISM band · Flexible smart solution

1 Introduction

Nowadays, the number of different radar applications is continuously growing. As an example, several short-range applications are appearing in the biological, biomedical, industrial or automotive fields [1–5]. This general trend fuels the importance that a feasible short-range radar system can have in various scenarios. In a short-range environment, one fundamental task is the capability to distinguish between two different targets. By using a pulsed waveform, it is known that the shorter the pulse duration τ the better the resolution ΔR, as shown in (1) [6].

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$$\Delta R = \frac{c_0 \tau}{2}. \tag{1}$$

where c_0 is the velocity of light.

As a matter of fact, for detecting targets within few meters, a pulse duration lasting nanoseconds is needed, which would require an expensive and complex pulse generator. In addition, a shorter pulse needs a higher peak power, which can involve electromagnetic compatibility (EMC) issues. On the other hand, the power consumption can be drastically reduced switching off the transmitter when it is not necessary.

For fulfilling all the requirements, a pulsed chirped signal has been adopted that allows for managing the range resolution in terms of the frequency modulation range. In the scientific literature it is possible to find other recent examples of compact modern radars [7–9]. The distinctive feature of the present work is certainly the feasibility of being adapted to several short-range applications. This task can be accomplished by taking into consideration its compactness and cost-effectiveness, without affecting its performance. As a final step, a single board will be realized, thus reducing of the overall dimensions. This paper has been organized as follows. The radar technology is presented in Sect. 2, the radar architecture is described in Sect. 2.1, the prototype measurement results are reported in Sect. 3. Finally, the conclusive remarks are drawn in Sect. 4.

2 Radar Technology

As stated before, the working frequency has been selected in the range from 24 to 25 GHz, which is typically used in the anti-collision automotive radars, because of two main reasons: firstly, the bandwidth is available for public use and it is possible to take advantage of existing technologies with a significant reduction of the final cost of the system. Secondly, the maximum resolution and range are suitable to be used in different scenarios. The aim of this system is to make the minimum detectable distance and the overall dimensions smallest possible, both within a few centimeters. In addition, the low energy consumption and the cost effectiveness are mandatory requirements. A pulsed chirp has been selected for the radar operation, thus benefiting from either energy saving and EMC immunity. In addition, by using a frequency-modulated signal, a very high resolution can be achieved if compared with such a short range. In this work, a linear frequency modulation (LFM) has been chosen for the transmitter signal modulation.

This modulation has some advantageous features and it is employed in many modern radar systems [10]. The waveform enables stretch processing which reduces the required bandwidth in high-resolution systems and it is considered to be Doppler tolerant [11, 12]. Indeed, the mainlobe and sidelobe structures are preserved also in

presence of large fractional Doppler shifts, given the ambiguity function of a pulsed LFM waveform, as reported in (2):

$$A(t, F_D) = \left| \frac{\sin(\pi (F_D + \Delta f t/\tau)(\tau - |t|))}{\tau \pi (F_D + \Delta f t/\tau)} \right| - \tau \leq t \geq \tau. \tag{2}$$

where F_D is the Doppler shift and Δf is the modulation range.

In addition, by considering that the peak of the function will occur when:

$$t = -\frac{\tau \boldsymbol{F_D}}{\Delta \boldsymbol{f}}. \tag{3}$$

The corresponding range error will be:

$$\delta R = -\frac{c\tau \boldsymbol{F_D}}{2\Delta \boldsymbol{f}}. \tag{4}$$

From Eq. (4), by taking into consideration the typical values of the Doppler shift, the pulse width and the modulation bandwidth of the proposed radar, the Doppler mismatch will induce very small errors in measuring the target range. As stated before, the target resolution can be expressed in terms of the linear frequency modulation range Δf:

$$R_t = \frac{c_0}{2\Delta f}. \tag{5}$$

From Eq. (5), a frequency modulation range of 1.0 GHz can be adopted thus obtaining a spatial resolution of 15 cm.

The Pulse Repetition Frequency (PRF) can be selected in order to obtain a sufficient feedback frequency for the user and can be tailored with respect to different applications.

2.1 Radar Architecture

The proposed radar architecture adopts the BGT24MTR11 integrated circuit as leading block, a SiGe MMIC Transceiver by Infineon Technologies AG [13]. By means of its 24.0 GHz fundamental voltage controlled oscillator (VCO), it can operate from 24.0 to 26.0 GHz by delivering a RF output power level of 11 dBm to comply with the required maximum range. It is equipped with a SPI interface, thus allowing to be controlled by a microcontroller unit. The adopted architecture schematic is shown in Fig. 1.

The realized radar employs commercial components for obtaining a cost-effective system and it is based on microstrip technology which allows an easy integration with the planar antennas as well as the prototype realization by using in-house facilities.

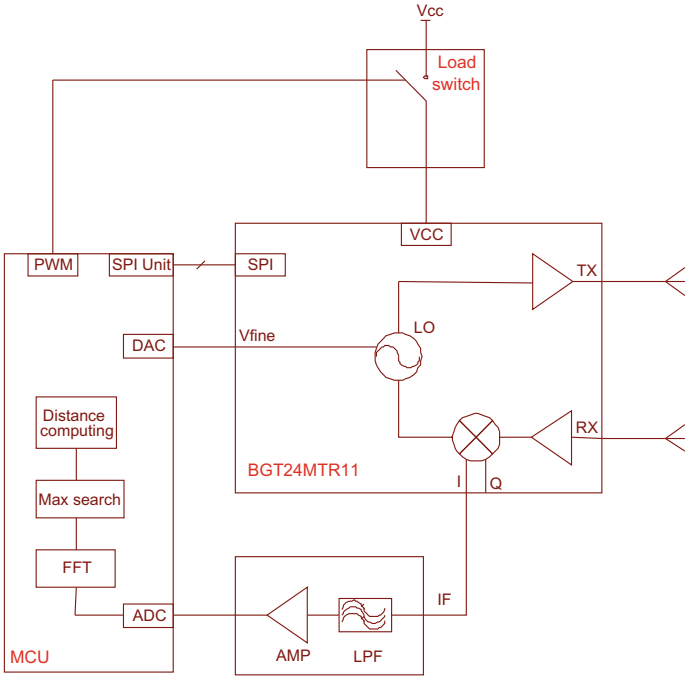

Fig. 1 Adopted radar architecture

The MCU's digital to analog converter generates a saw-tooth signal with a period of 2 ms to drive the VCO into the linear frequency sweep. The power amplifier switching time has been set for obtaining a pulse duration of 10 ms and a pulse repetition time (PRT) of 100 ms. These parameters have been chosen for achieving both a reasonable dwell time and a limited ON state period of the transmitter. The 10% duty-cycle can be considered a good compromise for either saving energy or guaranteeing a good data refresh time. It is important to underline that both the PRT and the duty-cycle can be tailored according to the application. A pulse-width modulation (PWM) unit manages the load switch operations by connecting and disconnecting the BGT24MTR11 from the supply voltage for saving power. This is necessary because disabling the transmitter outputs will not reduce the power consumption as all IC-internal blocks will still be running [14]. Finally, a fast-Fourier transform (FFT) is applied to the digitalized IF signal and maximum search algorithm is performed. To distinguish the signal from the noise, an adaptive threshold has been implemented, i.e. a crosstalk mapping is performed for calibrating the receiver without targets and finally the optimum threshold is computed [15, 16]. The frequency of the detected peak is strictly related with the delay of the signal, as reported in (6), whereas the target distance can be extracted using the well-known relationship showed in (7).

$$t_d = \frac{f_{peak} \cdot \tau}{\Delta f}. \tag{6}$$

$$D_t = \frac{c_0 t_d}{2}. \tag{7}$$

3 Experimental Results

With the aim to make the Infineon BGT24MTR11 pins accessible, a homemade board has been developed by means of a high precision mechanical plotter, on a Rogers Ro4350B substrate. The dimensions of the board are 3.4 cm × 5.2 cm. Afterwards, the Infineon XMC4500 development board has been used in order to drive the entire system and for processing the data. Two detailed pictures of the system are reported in Fig. 2.

To the aim of evaluating the accuracy of the system, different tests have been performed. A metallic cylinder-shaped target has been employed for performing two measurements at the distance of 1.5 and 2.5 m. The IF data extracted from the microcontroller and the threshold have been reported in Fig. 3 for confirming the expected performance.

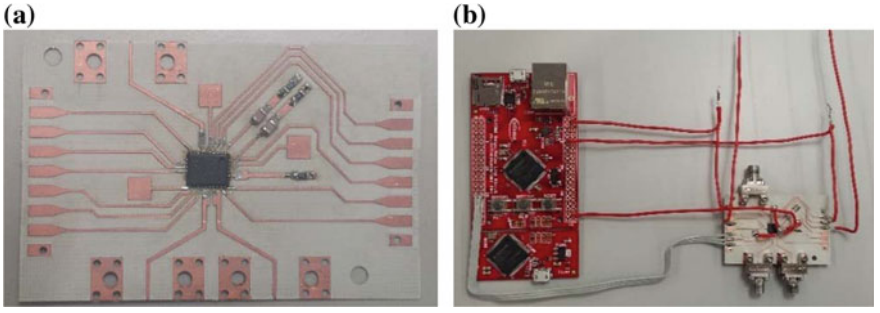

Fig. 2 Detailed pictures of the homemade board, alone (**a**) and with the XMC4500 development board (**b**)

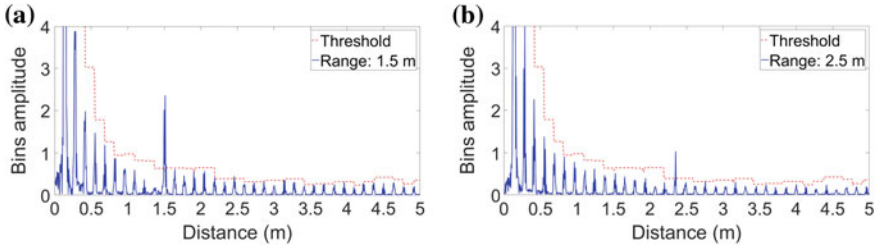

Fig. 3 IF signal (blue line) and threshold (red dashed line) for a target at 1.5 m (**a**) and 2.5 m (**b**) (Color figure online)

4 Conclusions and Future Works

In this paper, the design and development of a smart microwave radar is described. The aim of the work is the realization of cost-effective flexible radar for short-range applications and suitable for the integration in different scenarios.

The radar frequency bandwidth has been selected within the available ISM band, extending from 24 to 25 GHz. A pulsed chirp signal has been used for achieving a high resolution together with a low power consumption.

A system prototype has been realized with in-house facilities and several tests have been carried out, confirming the expected performance.

As a final step, a unique compact board will be designed for enhance the system miniaturization. Further developments are also foresight at 77 GHz.

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Multi-sensors Exhaust Gas Emission Monitoring System for Industrial Applications

Tommaso Addabbo, Francesco Bardi, Stefano Cioncolini, Ada Fort, Marco Mugnaini, Lorenzo Parri and Valerio Vignoli

Abstract The measurement systems commonly used for exhaust-gas composition analysis in industrial applications are usually expensive. Moreover, they need frequent calibration procedures to guarantee the measurement accuracy. The portable gas analyzer proposed in this paper takes into account a tradeoff between calibration time and device cost while maintaining an accuracy comparable with the standard instruments. The instrument is composed by a sensor array, based on both electrochemical and chemoresistive low-cost sensors, a measurement chamber, a custom front end electronics, and a PC-based acquisition and processing system. Specific processing algorithms have been designed to compensate problems such as sensor drift, sensor cross sensitivity to different gases, and dependence of the sensor response on temperature and humidity.

Keywords Electrochemical sensors · Chemoresistive sensors · Exhaust gas monitoring

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1 Introduction

Gas emission monitoring is becoming more and more important in the last years both in the industrial and the automotive field. The main reason is to satisfy the emission requirements, but the knowledge of the exhaust gas composition is also useful, for example, to control the combustion processes efficiency. The main problem in emission monitoring systems is not only to guarantee the required measurement accuracy but also to maintain it during time and in a large gas concentration ranges, which in general implies frequent calibration procedures and high costs. Taking into account these issues, in this work a measurement instrument based on an array of electrochemical and chemoresistive gas sensors is proposed for the accurate measure of carbon monoxide (CO), nitrogen oxides (NOx) and oxygen (O_2), which are the gases of greatest interest in emission monitoring. Moreover, processing algorithms designed ad hoc are used to compensate problems such as sensor drift, sensor cross sensitivity to different gases, and dependence of the sensor response on temperature and humidity. Different chemoresistive sensors are also used at the same time to increase the chemoresistive sensor selectivity and accuracy.

2 System Architecture

The proposed measurement system must be connected to a sampling and cooling apparatus (chiller), usually present in the industrial plants. It is composed by:

- An array of electrochemical and chemoresistive sensors hosted in two measurement chambers.
- A humidity and a temperature sensor.
- Dedicated front end electronics (one for each type of sensors).
- A data acquisition board (DAQ).
- A PC running the Labview-based control and data-processing program.

The sketch of the system is shown in Fig. 1.

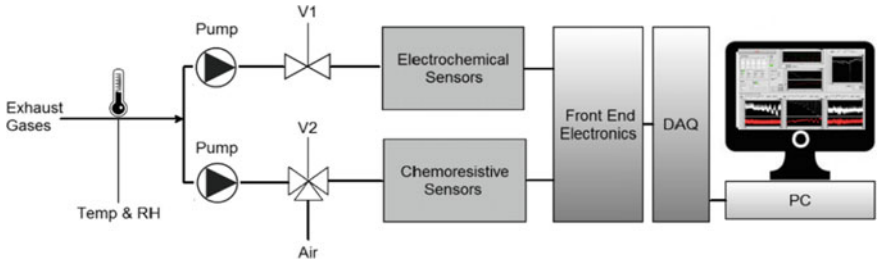

Fig. 1 System structure: the exhaust gases are pumped with a constant flow to sensors through two valves (V1 and V2); temperature and humidity are also measured

Table 1 Sensors used in the proposed system

Electrochemical sensors [1]	Chemoresistive sensors	Humidity sensor	Temperature sensor
Alphasense CO-A4	Alphasense CO-MMC [1]	Honeywell HIH4000 [4]	National Semicond. LM 32 [5]
Alphasense NO_2-A43F	Figaro TGS2620 [2]		
Alphasense NO-A4	$YCoO_3$ based prototype sensor [3]		
Alphasense O_2-A1			

The sensors used in the system are summarized in Table 1.

Electrochemical gas sensors are very accurate and selective, and can be used also at room temperature, but suffer from a relative short lifetime. In addition, these sensors can be damaged if exposed to very high target gas concentrations. On the other hand, chemoresistive sensors are usually less accurate, are characterized by a poor selectivity, and require to be heated to have a good sensitivity (the redox reaction at the sensor surface are promoted in the temperature range 150–350 °C), but they are more robust and durable in time. In the instrument described in this paper the chemoresistive sensors are used to detect high gas concentrations (accuracies of the order of tens of ppm are sufficient in this case), which could damage/poison the electrochemical sensors. In detail, with reference to Fig. 1, if CO concentrations > 100 ppm or NOx concentrations > 50 ppm are detected by the chemoresistive sensors, the valve V1 is closed avoiding the electrochemical sensors poisoning. On the other hand, in presence of CO and NOx concentrations within the electrochemical sensors' range, these latter are used to obtain high accuracy measurements (in the order of a few ppm).

2.1 Gas-Sensor Front End Electronics

For the proposed monitoring system three different front end boards (for the electrochemical sensors, the prototype chemoresistors, and for the commercial chemoresistors, respectively) were developed, which are connected to a data acquisition board (DAQ) with both analog inputs and analog output. The difference between the two front end boards for chemoresistors is due to the presence, in the prototype sensors, of a temperature sensor (PT100), not present in the commercial chemoresistors used, which requires a dedicated reading circuit. The temperature information, which is used to control the temperature in a feedback loop, is obtained in this case from the heater, which is used also as a temperature sensor after a characterization of its temperature coefficient.

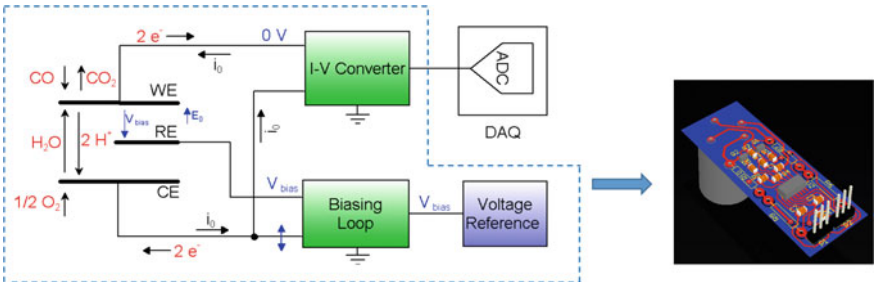

Fig. 2 Electrochemical front end block scheme

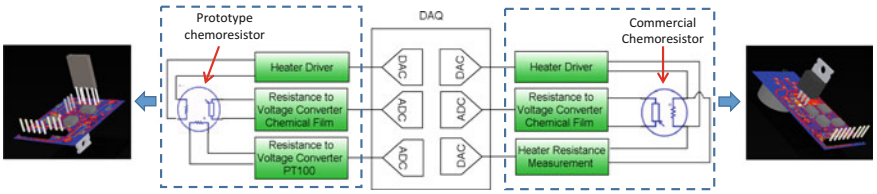

Fig. 3 Front end block diagrams for prototype (left) and commercial (right) chemoresistive sensors

The front end board block scheme for the electrochemical sensors is shown in Fig. 2. As an example the CO sensor is considered: the current flowing between Working Electrode (WE) and Counter Electrode (CE), which is proportional to the CO concentration, is converted to a voltage by an I-V converter. A biasing loop is used to maintain constant the potential at the WE interface by exploiting a third electrode (Reference Electrode—RE). The accuracy of the current measurements is ~1.5 μA, corresponding to an accuracy <3 ppm in terms of target gas concentration for all the adopted sensors.

The two front end circuit block schemes for the chemorestive sensors are shown in Fig. 3. In both cases the sensor resistance measurement is performed while maintaining constant the sensor temperature by a PI controller (~2 °C accuracy). This system allows for the measurement of the chemosensor resistance in the range 20 kΩ–50 MΩ with an accuracy up to 1%.

3 Measurement Post-processing

Electrochemical sensors exhibit in general a linear dependence of the output current with the gas concentration, with a low dependence on humidity and a well characterized dependence on temperature, which allows for an effective correction of the measured gas concentrations on the basis of the output of the LM 32 sensor (Fig. 1 and Table 1), as it will be shown in Sect. 4. For resistive sensors the problem is more complex: the sensor response is in general strongly dependent at a macroscopic level

on its working conditions, in terms of temperature, humidity, and presence of interfering gases. Hereafter a post-processing technique is introduced which allows to increase the sensor selectivity and accuracy [6], and which is based on the assumptions that the relationship between sensor resistance and gas concentration (CO and NO are considered in this case) can be written as:

$$R([CO],[NO]) = R_0\, e^{\frac{([CO^+]+[NO^+]+N_{si})^2}{T\alpha^2}}, \tag{1}$$

where N_{si} is the density of intrinsic surface states and $[CO^+]$ and $[NO^+]$ are the density of extrinsic donor surface states due to adsorbed CO and NO, respectively. Constant α includes Boltzmann constant k, dielectric constant ε, and electron charge q [3]. R_0 can be estimated by exploiting different responses of the sensor obtained at different working temperatures while maintaining constant the chemical environment, and by supposing that the quantity $\left[CO^+\right] + \left[NO^+\right] + N_{si}$ does not change.

3.1 Chemoresistive Sensor Data Processing Algorithm

The proposed processing algorithm is discussed with reference to an array of two chemoresistive sensors used in chemical environments in which both CO and NO are present. The approach is then generalized to the case of n sensors and k target gases, with n ≥ k.

For each one of the two sensors a set of preliminary resistance measurements is performed in reference conditions in terms of total gas flow, RH, room temperature, but changing the concentrations of CO and NO in a given range. In this way a surface *Rg*(CO, NO) can be defined in the [CO]-[NO] domain for each one of the sensors.

It is now possible to define the distance (*Dist*) between a measurement (*Rm*) and a point on the *Rg*(CO,NO) surface as:

$$Dist(CO, NO, Rm) = |Rg(CO, NO) - Rm| \tag{2}$$

Exploiting (2) it is possible, by combining the measurements of two different sensors, to find the most likely values of [CO] and [NO] by solving:

$$min_{CO,NO}(Dist(CO, NO, Rm_1, Rm_2)), \tag{3}$$

where:

$$Dist(CO, NO, Rm_1, Rm_2) = \sqrt{(Rg_1(CO, NO) - Rm_1)^2 + (Rg_2(CO, NO) - Rm_2)^2}, \tag{4}$$

and where subscripts 1 and 2 refers to sensor #1 and sensor #2.

This approach can be extended to *n* sensors and *k* gases S_i, i = 1:k, with $k > 2$, n ≥ k, included water vapor [7]. In this case Eqs. 3–4 become Eqs. 5–6, respectively:

$$min_{S_1,S_2,S_3,\ldots S_k}(Dist(S_1, S_2, \ldots S_k, Rm_1, Rm_2, \ldots Rm_n)), \tag{5}$$

$$Dist(S_1, S_2, \ldots S_k, Rm_1, Rm_2, \ldots Rm_n) = \sqrt{\sum_{i=1}^{n} (Rg_i(S_1, S_2, S_3, \ldots S_k) - Rm_i)^2}. \quad (6)$$

4 Experimental Results

Hereafter some examples of sensor-characterization results obtained in laboratory with the proposed system are presented. As anticipated, the electrochemical sensors exhibit in general a linear dependence of the output current with the gas concentration (Fig. 4), and the measurements can be effectively corrected for the effect of room temperature on the basis of the information reported in the data sheets.

The proposed post-processing technique for the chemoresistive sensors proved to be effective for mixtures of two gases (CO and NO). In Fig. 5, the surfaces Rg are normalized with respect to the sensor resistance R_{ref} measured in the same reference environmental conditions of Rg but without the target gases. An advantage of considering the normalized resistance is that, by periodically checking the R_{ref} value (in our system this is possible by acting on the valve V2 in Fig. 1) the sensor drift can be partially compensated.

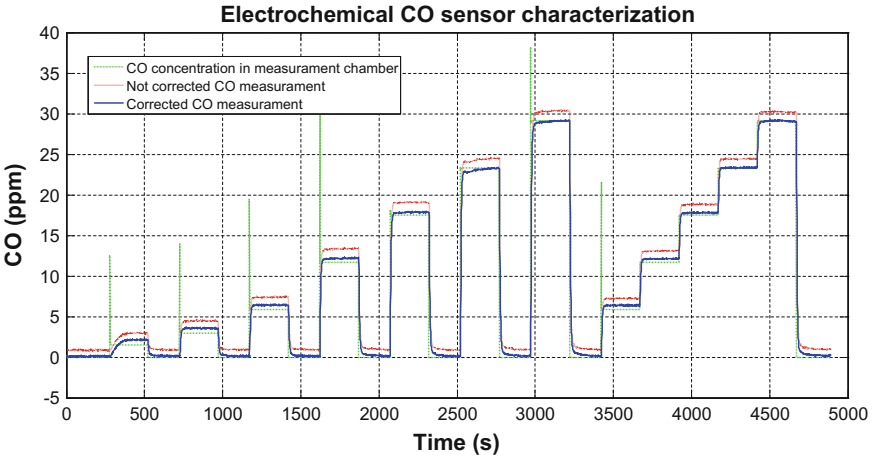

Fig. 4 CO-A4 sensor response to CO mixtures in air (RH = 50%, flow rate 200 mL/min). Green: real CO concentration, blue and red: measured CO concentration corrected and not corrected for temperature, respectively

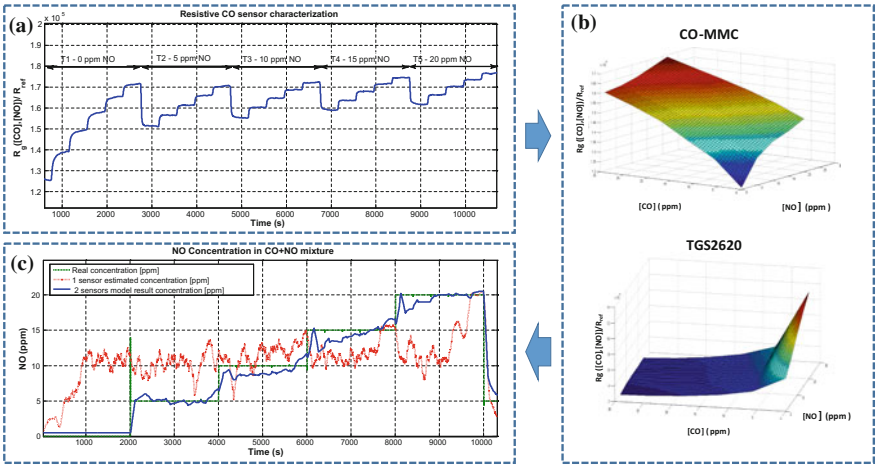

Fig. 5 A, B: Example of the processing technique described in Eqs. 2–4. In T1, T2, T3 and T4 are applied increasing concentrations of CO, from 5 to 20 ppm, while NO concentration is constant. C: NO concentration estimated with two sensors (continuous line), one sensor (dotted line). Dashed line: real NO concentration in the measurement chamber. During each stable phase of NO concentration the CO concentration varies as in T1 (plot A). For all the measurements, carrier gas is N_2 + 10% O_2, RH is 0%, flow rate is 200 mL/min, sensors' temperature is 400 °C

5 Conclusions

In this paper a measurement system for exhaust gas emission monitoring in industrial plants is presented. The system is based on an array of both electrochemical and chemoresistive sensors. During the laboratory tests the system proved to be able to guarantee measurement accuracies in terms of CO and NOx concentrations comparable with the ones required by the standard regulations (a few ppm).

The system, thanks to the chemoresistive sensors, can avoid to expose the electrochemical sensors to too high concentrations of target gases, which induce sensor poisoning and performace degradation. For this purpose, a post-processing technique for the measurement data of the chemoresistive sensors was proposed, in order to increase their accuracy and selectivity. After the laboratory tests, a prototype of the measurement system is continuously working in parallel with standard instruments at a test plant of BHGE in Florence.

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Challenging CPS Trade-off Adaptivity with Coarse-Grained Reconfiguration

Francesca Palumbo, Carlo Sau, Tiziana Fanni and Luigi Raffo

Abstract Cyber Physical Systems are highly adaptive systems, prone to change behaviour due to external/internal conditions. From the computation point of view, reconfigurable systems may address adaptation. In this paper, by a set of examples we show how coarse-grained reconfiguration may successfully allow achieving dynamic trade-off management, while considering different technology targets and different design flows.

Keywords Cyber · Physical systems · Hardware reconfiguration · Adaptive systems · Datapath merging

1 Introduction

In the era of Cyber-Physical Systems (CPS) designers need to cope with complex devices composed of different interacting components, with multiple and distinct behavioural modalities variable over time. CPS are characterized by three dominant layers: functional, physical and communication layers. These layers can be specified through different levels of abstraction and require deep inter/intra-communication. Computing devices, human users and physical environment are tightly bound, making CPS prone to changes. They no longer offer hard-wired performance with identical and predicable behaviour or execution profiles over time: CPS are highly evolvable

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systems where functional (F) and non-functional (NF) requirements are variable, and autonomous adaptation to environmental changes or unpredictable human requests should be supported. Varying workloads and performance objectives have to be guaranteed, while continuously optimizing performance goals, i.e. minimizing energy consumption, meeting the available power budget, and so on.

This paper demonstrates that, adopting a Coarse-Grained Reconfigurable (CGR) approach can suite the scope of providing flexibility and adaptation to changeable F/NF requirements to the computing layer. As an example you can consider an embedded video decoding system that lowers the quality of its output to augment battery life [1]. Embedded systems for acquisition, encoding and transmission of environmental images may benefit from variability. Continuously monitoring F (decoding quality) and NF (remnant battery) requirements, it would be possible to drive the CGR support to serve user requests or suggest a better device configuration.

This paper is organized as follow. Section 2 presents foundations and methodology to enable dynamic trade-off management. Section 3 provides, through different use-cases, a proof of concept of the feasibility of adopting a CGR approach to serve dynamic and variable environments. Section 4 concludes with final remarks.

2 Hardware Adaptivity Support in CPS Designs

CPS adaptivity implies system level flexibility. This latter typically collides with performance. Indeed, general purpose entities (i.e. CPUs, GPUs and DSPs) implement potentially any application described in the supported programming language, but their performance is quite limited due to their poor specialization. On the contrary, ASICs platforms boost performance, but execute only the application they have been designed for. In between, an appealing solution is provided by the adoption of reconfigurable platforms. Reconfigurable architectures are basically meshes of processing elements (PEs) whose functionality and connections can be configured at run-time. Depending on the granularity of the PEs, it is possible to have fine-grained or coarse-grained reconfigurability. The former, typical of FPGAs, involves bit-level PEs. It presents high flexibility though bit-level programmability, but implies some configuration time overhead. CGR systems deal with word-level PEs, guaranteeing less flexible, but faster, reconfiguration. Combinatorial switching logic allows single-cycle reconfiguration and, on top of that, a CGR approach can make ASIC designs flexible, allowing them to switch among a finite set of input functionalities. In the following we explain the contribution of this paper and the adopted methodology.

2.1 Contribution

CGR platforms are effective in flexible, but constrained, scenarios [2] and, in our opinion, they can tackle the adaptation needs of CPS designs. In this paper, we

show how CGR systems are naturally capable of guaranteeing dynamic trade-off management among relevant system metrics. Mapping CGR platform is not so straightforward, requiring a deep knowledge on the functionalities/kernels to be implemented. To mitigate this issue automated or semi-automated design environments have been proposed in literature [3, 4]. In our work we intend to prove that automated flows do not affect trade-off guarantees. On the contrary, in some cases, the features of those environments could possibly improve the trade-off itself.

2.2 Dynamic Trade-off Management

PEs used in CGR systems, can be homogeneous (identical computing blocks) or heterogeneous (not identical elements) and the computing fabric may not necessarily be composed of a regular, fully connected, infrastructure. PEs are normally not constrained in granularity, ranging from ALUs to a discrete cosine transform. The more a CGR system is customized to fit application needs, with application specific PEs and avoiding any redundancy or extra connection, the more its efficiency and performance are maximized. On the other hand, heterogeneous and irregular platforms are those that suffer the most mapping issues.

We have addressed the problems of dimensioning the hardware substrate and of mapping several kernels over it by combining dataflow models to the CGR approach. This combination allowed us facilitating and speeding-up system deployment, while being able to offer adaptivity support.

Design Time Support: Datapath merging techniques are used to minimize the number of PEs and communication links integrated into a CGR datapath. Our dataflow to hardware software infrastructure, named Multi-Dataflow Composer (MDC) tool, combines different input dataflow graphs, by merging the common PEs, into a unique dataflow specification. The resulting dataflow is then synthesized in hardware according to a one-to-one mapping strategy between graph nodes and PEs [6]. Different input graphs, sharing common PEs, access them by means of configurable switching elements, responsible of forking/joining the execution flow where needed. Some examples of the outcome of this process are shown in Fig. 1.

Run-Time Management: The CGR substrate executes all the input specifications one at a time. By switching from one configuration to another, varying the *execution profile*, you may change the system behaviour and performance. In CPS designs, the execution profile may vary due to user requests or internal system conditions. On the top of Fig. 1, an example of functional approximate computing is provided: the depth of the computation can be sized to serve different energy versus quality profiles. The more stage you use the more precise is your computation, but it is more energy hungry. At the bottom of Fig. 1, doubling the actor S2 you are able to execute faster, consuming more power. In both cases, different trade-offs between F/NF requirements are implemented over the same substrate and can be tuned according to the CPS needs at run-time.

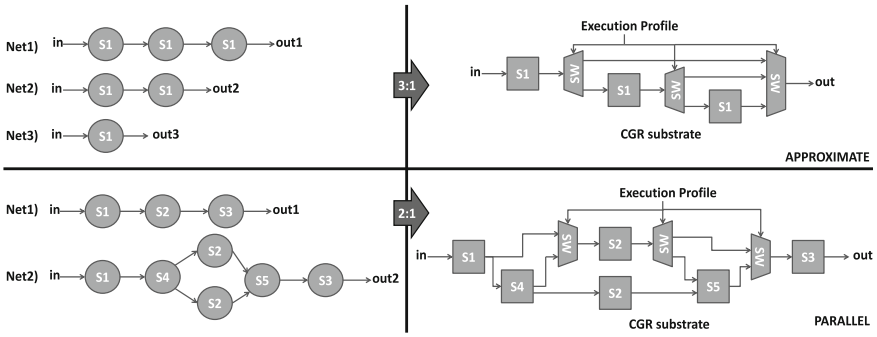


Fig. 1 Dataflow to hardware: Trade-off friendly CGR platforms

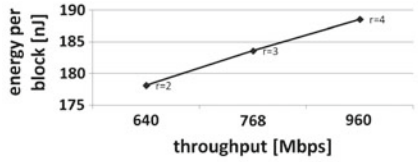
3 Experimental Results

We demonstrated the effectiveness of the CGR approach in dynamic trade-offs management on three scenarios. The first one is an AES blockcipher manually implemented on a Xilinx Artix-7 FPGA, while the others demonstrate that automatic deployment does not affect dynamic trade-off tuning neither adopting an FPGA technology (HEVC motion compensation interpolator) nor adopting an ASIC 90 nm CMOS one (FFT accelerator). Design automation follows the approach described in Sect. 2.2. All the reported power/energy numbers consider post-synthesis switching activity.

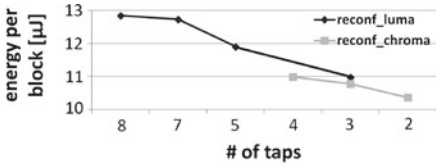
3.1 Manually Implemented CGR AES on FPGA

The 128 bits Advanced Encryption Standard (AES-128) blockcipher is the de facto encryption standard worldwide [5]. The cipher encrypts 128 bits of data in one pass of the algorithm and uses a secret key of length 128 bits. The ciphertext is achieved in 10 subsequent executions of a *Round Function* over the input plaintext. Lightweight AES designs adopt serialization, reducing the hardware footprint by reusing components over multiple clock cycles: latency increase allows energy saving [6]. In this scenario, Banik et al. demonstrated that energy consumption strictly increases with the number of *rolling rounds* (r) [7]. Therefore, a CGR platform combining designs with different number of r would offer different execution profiles.

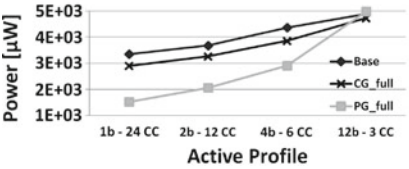
Our CGR infrastructure offers different working points: smaller r values give slower energy efficient ciphers, larger r quicker less energy efficient ciphers. Figure 2a depicts the trade-off curve achievable by a CGR AES-128 design, where different profiles with 2, 3 and 4r are implemented. Energy consumption is proportional to r: to reach 25% additional throughput, going from $2r$ to $4r$, you need to pay an extra 6% of energy consumption. Smaller r profiles suite less computa-



(a) AES: energy vs. throughput



(b) HEVC: energy vs. quality



(c) FFT: power vs. throughput

	Area [GE]	Vs Base %
Base	885,575	---
CG_full	885,871	0.03
PG_full	926,835	4.66

(d) FFT: Area. GE = Gate Equivalent

Fig. 2 Results analysis

tional demanding tasks, e.g. communicating with a RFID. Larger *r* profiles, enabling the maximum throughput, can be used to serve high performance applications, e.g. video stream encryption. In terms of resources, a CGR system typically implies an overhead. Here we have no FF penalty, but +16% LUTs are required wrt a *4r* AES stand-alone design (on the XC7A35tlCPG236 FPGA).

3.2 Automatically Derived HEVC Interpolator on FPGA

The High Efficiency Video Coding (HEVC) standard provides 50% more subjective video quality with no penalty on the bit rate, at the price of an increased complexity and system consumption [8]. Within HEVC decoding, motion compensation is one of the most computationally intensive portions of the algorithm. When fractional pixel motions have to be compensated, the block prediction is performed through an interpolation (two cascaded N taps FIR filters, one for horizontal and one for vertical motion) of its reference block. To reduce and dynamically tune the energy consumption of the interpolator, Nogues et al. [9] exploited functional approximate computing. They demonstrated in software that it is possible to waive some image quality (# of taps reduction) to save energy. In hardware, an analogue behaviour can be obtained leveraging on CGR architectures, as presented in [10]: starting from a legacy implementation of the interpolation filters, run-time adaptive solutions can be derived by dynamically excluding some taps from the computation (as presented on top of Fig. 1).

In this paper, we present the results achieved by feeding different dataflow specifications, representing variable interpolation filter sizes, to the MDC tool to automat-

ically produce a CGR luma interpolator (*reconf_luma*), performing 8, 7, 5 and 3 taps filtering, and a CGR chroma one (*reconf_chroma*), performing 4, 3 and 2 taps filtering. Reconfiguration has a negligible impact on FFs (legacy luma +1.6%, legacy chroma +5%), but largely impact on LUTs (legacy luma +186%, legacy chroma +63%) on the considered FPGA target (XC7A100TCSG324). The trade-off curves for both the color space components are shown in Fig. 2b. The 3-taps CGR luma profile saves 15% of energy per block wrt the 8-tap legacy configuration, while CGR chroma saves up to 5%. This variability can be exploited on a smart device equipped with a proximity sensor: when the user is close to the device, quality should be high, but when he/she is far, and cannot distinguish details, the quality can be lowered to save energy. This demonstration testifies that, even adopting a completely automated flow (which was not the case in [10]), dynamic trade-off management can be still offered.

3.3 Automatically Derived and Optimized FFT on ASIC

Fast Fourier Transform (FFT) is an optimized algorithm for the Discrete Fourier Transform calculation, widely adopted in several applications (from differential equations to digital signal processing). This use case involves a radix-2 FFT of size 8, obtained by means of three pipelined stages of four butterflies each (12 butterflies overall). From the 12 butterflies dataflow design, three variants have been derived decreasing the butterflies number: resources are multiplexed in time and reused, latency increases and throughput becomes lower. The CGR infrastructure, automatically derived with the MDC tool, includes the following profiles: (1) *12b* is the baseline 12 butterflies FFT design, taking 3 clock cycles to execute; (2) *4b* involves 4 butterflies and computes in 6 cycles; (3) *2b,* 2 butterflies and 12 cycles; (4) *1b,* 1 single butterfly and 24 cycles. The trade-off analysis is presented in Fig. 2c as the *Base* curve. Power versus throughput instead of energy results is shown: in some cases the rate of producing/consuming energy has to be considered, e.g. to ensure battery would be able to power up the other logic. This graph confirms that dynamic trade-off management is achievable, on ASIC too, using an automated design flow.

On ASIC more efficient power reduction methodologies can be implemented to save the power due to the portion of the system in idle while one of the profiles (input dataflows) is running. MDC offers the possibility of automatically implementing power-gated and clock-gated designs [11]. The results of such implementations are shown in Fig. 2c respectively as *PG_full* and *CG_full* curves. The *PG_full* case is capable of achieving the largest power saving going from the *1b* to the *12b* FFT implementation. Figure 2d depicts the area overheads, in gate equivalent, of these more advanced implementations: it is clearly negligible, being always below 5%.

4 Conclusions

In this paper we analysed the possibility of providing adaptivity support to different execution profiles by leveraging on the coarse-grained reconfigurable paradigm. Considering different application scenarios, we proved that a CGR approach can suite the F/NF requirements run-time adjustment with different technologies and when automated design strategies are adopted without any particular need of manual fine tuning. The results of this paper will be used as a starting point for the EU Project CERBERO (http://www.cerbero-h2020.eu/). In particular we intend to enable embedding runtime models in the CPS systems to address changeable requirements variations.

Acknowledgements This work has received funding from the EU Commission's H2020 Programme under grant agreement No 732105.

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A Novel Wearable Sensor System for Multi-lead ECG Measurement

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Abstract This work is concerned with the development of a wireless low-power wearable system to be used for multi-lead ECG monitoring. Potential applications can range from sport and fitness to healthcare.Query The paper aims to present the architecture of the system and its performance, along with in vivo results achieved with carbon based smart textiles.

Keywords Wearable sensor system · ECG · Smart textiles

1 Introduction

According to the World Health Organization (WHO), ischemic heart disease is the world's biggest killer in the last 15 years [1]. This kind of heart diseases represents a concern not only for high-income and middle-income economies, but also for low-income and lower-middle-income countries. Heart diseases arise not only as consequences of wrong lifestyles and food habits, but also for the lack of prevention behaviors. In this framework, the early diagnosis plays a key role and may be possible by means of targeted screenings on high-risk patients, yet they have to cope with budget reduction in healthcare. Electrocardiogram (ECG) is one of the most common and reliable diagnostic exam for detecting cardiovascular and other related diseases. It is based on a representation of the electrical activity of the heart recorded through electrodes placed on the patient's body and showing the heart activity from different angles (leads) of the electrical potential. Up to 12 leads can be recorded by means of 10 electrodes placed in specific positions. The right leg electrode can be actively driven with a specific circuitry (Right Leg Driver or RLD) in order to reduce the

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Common Mode Voltage [2]. Thanks to advances in semiconductor and microelectronic technologies, we are beholding the increasing diffusion of wearable devices able to detect physiological signals. This kind of systems can be used not only as consumer devices for sport and fitness applications [3], but also as diagnostic means for healthcare and biomedical purposes [4, 5]. This work describes the development of a wireless platform to be used for multi-lead ECG monitoring applications within a wearable system. Moreover, it can measure the bioimpedance, thus providing an estimation of the respiration frequency, and integrates additional sensing features for the measurement of other physiological parameters, such as body skin temperature, ambient temperature, and the 3D body acceleration. All these requirements have been achieved in a small form factor and in such a way that integration with garments can be easily done. The paper aims to describe the architecture of the system and summarizes the preliminary results. In particular, Sect. 2 describes the architecture of the system, the embedded firmware and the power consumption in different modes of operation. Section 3 reports the noise performances and the results of the measurements carried out in vivo by means of disposable gel electrodes and a carbon-based smart textile. Section 4 provides a comparison between the system proposed in this work and several state-of-the-art solutions. Finally, the conclusions are drawn.

2 System Architecture

The electronic system presented in this work is the result of a design aiming to provide as many desirable features as possible in a small form factor. A picture and the block diagram of the system are depicted in Fig. 1. In the following sections, an overview about the main building blocks and features of the system is given.

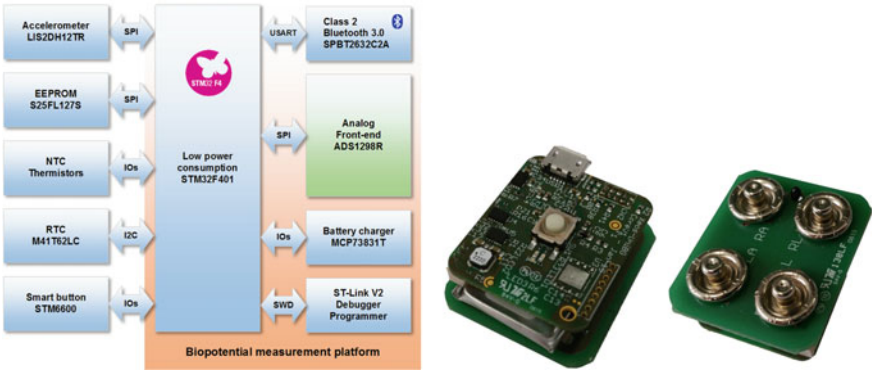

Fig. 1 Block diagram and picture of the proposed wearable system. The electronic system is based on two PCBs, one hosting the main electronics (left) and one exposing the 4 ECG electrodes and the thermistor (right). The battery is located in between the two PCBs

System architecture: As shown in Fig. 1, the electronic system is based on two Printed Circuit Boards (PCBs), stacked and connected one on top of the other with a board-to-board connector carrying bio-signals and the ground reference. The higher board integrates the main electronics, whereas the lower PCB provides a mean for interconnection with garments by means of snap-buttons as ECG electrodes. In such a configuration, the form factor of the system is $30 \times 25 \times 10$ mm^3.

CPU: The processing core of the system is the STM32F411 microcontroller, which combines a wide range of peripherals and interfaces, the fairly high processing power of an ARM Cortex™ M4 32-bit architecture and low-power performance in a 7×7 mm^2 package.

Power supply: The system is powered by a 3.7 V, 155 mAh lithium polymer battery and is scaled down to the 3 V operating voltage with a high efficiency step-down power management circuit. The battery can be recharged through the dedicated micro USB connector and is placed in-between the two PCBs building up the electronic system. In this configuration, the system can operate for up to 5 h of continuous 3 leads ECG measurement with streaming via Bluetooth.

Analog Front End (AFE): The ECG measurement is carried out by the ADS1298R integrated circuit [6], featuring 8 low-power and low-noise differential amplifiers with adjustable gain.

The analog signals are internally digitized with 8 24 bits delta-sigma ADCs running at programmable frequencies between 250 sps and 32 ksps. The digital traces can be read out with an SPI bus. The system integrates modulation-demodulation circuitry for the respiration impedance measurement. The AFE provides flexible configuration of input multiplexers and includes the circuitry required for lead-off detection, RLD and other ECG-specific features. Even though up to 8 channels can be measured with the ADS1298R integrated circuit, in the proposed system only 4 electrodes for the 3 limb leads measurement and the RLD have been foreseen. However, the number of measured channels can be scaled up to 8 with a lower PCB properly designed, yielding to a 11 leads ECG detection.

Connectivity: The system integrates the SPBT2632C2A Bluetooth V3 Class 2 module with antenna enabling a high data rate wireless communication capable of streaming up to 4 traces at 500 Hz through the Serial Port Profile (SPP).

For a lower power consuming solution and lower throughputs, the footprint of the module has been designed to be pin-to-pin compatible with the one of the Bluetooth Low Energy (BLE) SPBTLE-RF module.

Inertial and temperature sensors: The system integrates the LIS2DH12 3D accelerometer for activity detection and recognition. Moreover, a thermistor for ambient temperature measurement is located on the higher PCB whereas body skin temperature can be measured with a dedicated thermistor mounted on the lower PCB.

Storage: The system features a 128 Mb flash memory for data storage enabling a low-power mode of operation during which data are logged on-board and downloaded afterwards. The memory can retain up to 2 h of single ECG trace recorded at 100 Hz.

Firmware: The system can be awakened from the low-power stop mode either with the push-button or with an acceleration exceeding a determined threshold. Here-

Table 1 Power consumption for different modes of operation

Mode	Current drawn [mA]	Power cons. @ 3.8 V [mW]
Stop	0.2	0.76
Idle	6	22.8
Log	9	34.2
Stream	30	114

after, the operation is controlled by means of a set of commands transmitted via Bluetooth:

- In streaming mode, the system transmits periodically the selected ECG and bioimpedance signals, along with the acceleration data, at a desired frequency.
- In log mode, the Bluetooth module goes in deep sleep and the storage of the selected traces at the desired frequency is enabled. Logged data can be downloaded afterwards by means of a specific command.
- In single shot mode, body skin temperature and ambient temperature can be retrieved once.

Power consumption: Table 1 summarizes the power consumption of the proposed system in the different modes of operation. It has to be noted that the results reported refer to preliminary measurements and power consumption has not yet been optimized.

3 Performance

3.1 Noise Measurements

A characterization of the system's input referred noise has been done using two different methods:

- Inputs internally shorted by means of the specific registers of the AFE
- Inputs externally shorted in order to consider also the noise contribution of the cables

Each reading has been done using a different gain of the differential amplifiers. A minimum of 55 s of readings at 500 Hz was used to calculate the RMS (Root Mean Square) and peak-to-peak noise. Figure 2 depicts the measured input referred noise; at the maximum gain and with the inputs externally shorted, the RMS value is 0.8 μV whereas the peak-to-peak value is 6.1 μV.

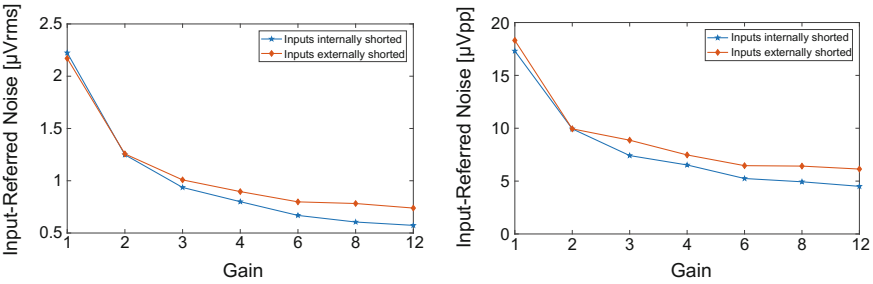

Fig. 2 Input-referred noise

3.2 Results with Disposable Gel Electrodes and Carbon-Based Smart Textiles

After a first characterization of the system achieved by means of a patient simulator [7], measurements have been carried out using disposable ECG electrodes connected to the platform in order to assess the performance of the system with medical grade electrodes. Figure 3 depicts a raw measurement of the three limb leads with the Right Led Drive buffer disabled and with the RLD enabled. In both cases the ECG signal is clearly represented, but it is possible to observe that the noise contribution is lower when the RLD buffer is enabled. To demonstrate the feasibility of a fully wearable system based on the proposed hardware, carbon based membranes have been used as electrodes to carry the ECG signals from the body. Almost any kind of substrate can be treated by applying a thin layer of these materials, making them suitable for wearable applications. Several kinds of carbon-based textiles have been characterized by evaluating the surface resistance and among these the one featuring the lowest surface resistance has been used for the development of ECG electrodes. Each strip is 31 cm long, 4 cm wide and 35 µm thick. A 10 pins connector has been crimped at one end of the strip, whereas a wider area has been tailored at the other end of the strip to improve the electrical contact with the body skin. In a final envisioned application, the membranes are applied to a garment in such a way that all the 3 leads can be measured and the right leg can be driven. During these preliminary tests, only lead I has been measured with a pair of strips firmly connected to the left and right wrists by means of elastic wrist-bands. Even though the noise contribution in the acquired ECG is not negligible, the results are promising and demonstrate that the proposed system can be used for the measurement of the ECG in wearable applications.

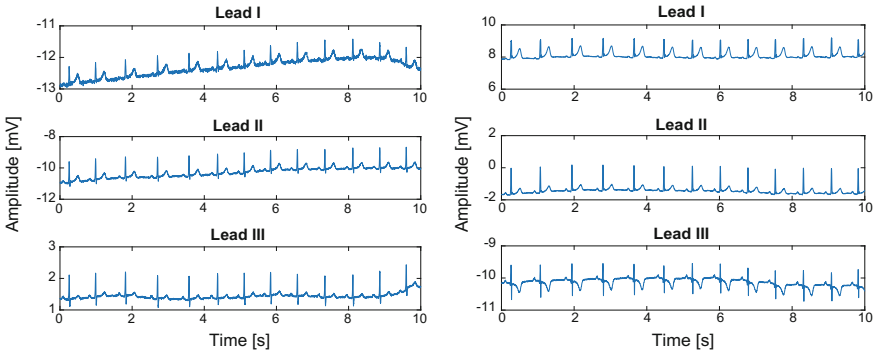

Fig. 3 ECG signal with gel electrodes. Left side: RLD not active. Right side: RLD active

4 Comparison with State-of-the-Art Systems

The system proposed in this work has been compared to wearable state-of-the-art solutions presented in literature [8–14] and commercially available [15, 16] in terms of number of leads, additional sensing capabilities, RLD circuit, dimensions, wireless capabilities and power consumption.

Results are summarized in Table 2. As it can be noticed, the proposed system is among the few featuring more than 1 lead ECG and respiration detection, as well as body skin temperature measurement and the RLD capability. In streaming mode at the maximum frequency (500 Hz), the current drawn is about 30 mA, setting the battery life to about 5 h of continuous operation. However, the power consumption can be lowered significantly by transmitting only some key parameters and a higher capacity battery can be used in order to increase time between charges. All these features have been achieved in a form factor which is comparable to or lower than state-of-the-art solutions, making the proposed system an attractive solution for wearable multi-lead ECG applications.

5 Conclusion

In this work, a wearable sensor system for multi-lead ECG measurement has been presented. The system is capable of measuring up to 3 ECG leads, the bioimpedance, the 3D acceleration, the body skin temperature and the ambient temperature. The architecture can be easily modified in order to increase the number of detectable ECG leads up to 11. A first set of measurements have shown promising results proving that the proposed solution can be integrated in garments for a non-invasive and easy to use wearable system. Ongoing activities are focused on the optimization of the power consumption through the implementation of a wireless communication based

Table 2 Characteristics comparison between wearable ECG devices

	# leads	Resp.	Body temp.	RLD	Area W x L [mm^2]	H [mm]	ADC res. [bits]	Spl rate [SPS]	Radio	Current drawn [mA]	Battery life [h]
[8]	1	N	N	Y	55×42	6.9	12	250	No	2.72	220
[9]	1	N	N	Y	40×25	0.6	12	512	BT	31	33
[10]	1	N	N	N	58×22	n/a	14	100	Zigbee	41.8	10
[11]	3	Y	N	No	n/a	n/a	10	125	BT	n/a	n/a
[12]	1	N	N	Y	n/a	n/a	10	500	BLE	11	24
[13]	1	N	N	N	65×34	17	24	320	Zigbee	4.07	160
[14]	1	Y	N	Y	130×50	11	12	750	BLE	9	96
[15]	3	Y	Y	N	28 (diam)	7	12	250	BT	n/a	18
[16]	1	N	N	N	90×40	16	8	300	BT	n/a	48
This work	3 (11)	Y	Y	Y	30×25	10	24	500	BT	30	5

on the Bluetooth Low Energy technology and embedded low-power algorithms able to extract key parameters of the ECG trace.

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Real-Time in-Line Industrial Fluids Characterization Using Multiple Pulse Repetition Frequency

Valentino Meacci, Riccardo Matera, Johan Wiklund and Stefano Ricci

Abstract The characterization of fluids flowing in industrial pipes is of paramount importance to optimize the production process and guarantee the final product quality in most industries. Rheological parameters of the fluid can be efficiently calculated starting from the Pressure Drop (PD) along a tract of the pipe, and the velocity profile that the flow develops along the pipe diameter, which can be assessed through Ultrasounds Pulsed Wave Doppler (PWD). Unfortunately, in PWD the maximum detectable velocity is restricted by the aliasing limit related to the Pulse Repetition Frequency (PRF). The use of PRF sequences at different rate can recover de-aliased velocities by combining the aliased data. In this work, we extend the capabilities of an embedded PWD ultrasound system used to characterize industrial fluids by implementing, in real-time, the multi-PRF method.

Keywords Doppler measurement · Fluid characterization · Nyquist velocity extension · Staggered double-PRE

1 Introduction

The assessment of the fluids properties in chemical, cosmetic, pharmaceutical, and food industries is fundamental for optimizing the production process. Moreover, their careful monitoring during the production steps guarantees the final product quality. Classical methods for fluid characterization consist in off-line analysis of specimens collected at different levels of the production chain. An efficient method for in-line fluids characterization uses ultrasounds to detect the velocity profile of the fluid moving in the pipe. The profile data, combined with pressure measurements, allows an accurate characterization according to the Pulsed Wave Doppler (PWD) + Pressure

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Drop (PD) method [1–3]. Unfortunately, in PWD, the maximum detectable velocity is related to the Pulse Repetition Frequency (PRF), which, in turn, is limited by the maximum investigation depth. High flow-rates flowing in large industrial pipes produce Doppler frequencies that easily exceed the Nyquist limit, thus resulting in aliased, corrupted measurements. Multi-PRF (MPRF) is a known technique that allows an extension of the Nyquist limit [4, 5]. MPRF is based on the transmission of successive burst sequences, where the period between pulses changes according to specific PRFs ratios. Each aliased spectrum achieved at different PRFs is recombined to reconstruct de-aliased spectra needed to calculate the velocity profile of the fluid in the pipe. In this work, we present a PWD system that implements MPRF in real-time to characterize industrial fluids. Experimental de-aliased velocity profiles measured by this system are reported.

2 Multi-PRF Method

According to the Nyquist-Shannon theorem the maximum velocity v_N of the fluid that can be investigated without ambiguity is:

$$v_N = \frac{PRF}{4}\lambda \tag{1}$$

where Pulse Repetition Frequency (PRF) is the number of the transmitted signal per second and λ is the wave length of the transmitted ultrasound signal. The maximum investigation depth D_m is directly related to the PRF and v_N by:

$$D_m = \frac{c}{4PRF} = \frac{c}{8v_N}\lambda \tag{2}$$

where c is the sound speed in the medium.

To measure the velocity of the fluid beyond the Nyquist limit, Multi-PRF (MPRF) generates sequences of two or more PRFs to measure Doppler velocities v_D that alias differently. Unambiguous Doppler velocity v_D^u is related to velocities v_D through a Nyquist number $n_N \in \mathbb{Z}$:

$$v_D = v_D^u - 2n_N v_N \tag{3}$$

The Nyquist number is obtained from the difference between Doppler velocities affected by aliasing as follow:

$$Np = nint\left(q_i \frac{v_{Di} - v_{D1}}{2v_{N1}}\right) = nN_1 q_i - nN_i p_i \tag{4}$$

Table 1 Nyquist numbers with $\boldsymbol{PRF}_2 = \frac{3}{4}\boldsymbol{PRF}_1$

$Np = nint\left(q_i \frac{v_{D2}-v_{D1}}{2v_{N1}}\right)$	nN_1	nN_2
−3	0	1
−2	1	2
−1	−1	−1
0	0	0
1	1	1
2	−1	−2
3	0	−1

v_{Di} and nN_i are the corresponding Nyquist velocity and Nyquist number at the $PRF_i = \frac{p_i}{q_i} PRF_1$, where p_i and q_i are positive integer ($p_i < q_i$) which defines supplementary smaller PRF_i; *nint(x)* is the integer nearest to x.

In this application, a multi-PRF with $PRF_2 = \frac{3}{4} PRF_1$ and $p_2 = 3$, $q_2 = 4$ are used to extend Nyquist velocity v_{Ne} by a factor k = 3 achieved by:

$$v_{Ne} = LCM(p_2, ..p_i, ..)v_{N1} = kv_{N1} \tag{5}$$

where LCM is the least common multiple.

As detailed in [4, 5], to ensure the reconstruction of the unambiguous Doppler velocity the Nyquist numbers must respect the following relations:

$$|nN_i| \leq ceiling\left(\frac{kq_i}{2p_i} - \frac{1}{2}\right) \quad \text{and} \quad |nN_1 q_i - nN_i p_i| = \frac{1}{2}(p_i + q_i) \tag{6}$$

where *ceiling(x)* gives a smallest integer equal to or greater than x.

In the multi-PRF scheme with $i = 2$, $|nN_1| \leq 1$ and $|nN_2| \leq 2$ are achieved from the (6) which combined with the (4) produces the Nyquist numbers reported on the Table 1.

Finally, to obtain the unambiguous Doppler velocity v_D^u the first term of (4) must be calculated, then by a Table 1 the corresponding Nyquist numbers (nN_i) are achieved, and v_D^u is reconstructed through the follow equation:

$$V_D^u = \frac{\sum_i \frac{q_i}{p_i}}{\sum_i \frac{q_i}{p_i}} v_D^u = \frac{\sum_i \frac{q_i}{p_i}}{\sum_i \frac{q_i}{p_i}} (v_{Di} + 2n_{Ni} v_{Ni}) \tag{7}$$

3 The System

The system depicted in Fig. 1 is made up of two boards: The Analog Front-End and the Digital Board needed to process and condition the ultrasound signal [6–9]. A

Table 2 System features

Features	Value
TX/RX channels	2, multiplexed
Dimension	10×12 cm
Power consumption	5 W max
Analog Gain	7–55 dB
Tx voltage	10–80 Vpp
TX/RX frequency range	1–7 MHz
TX burst	Arbitrary waveform
Internal buffer	64 MB
Sampling Freq.	100 MHz
Processing time	42 μs/depth
Input noise on 50 O	1.5 nV$\sqrt{}$Hz
On board Proc.	RF and IQ data, Spectral Matrix, Freq. Profile, Multi-PRF

sbRIO family board (National Instruments, Austin, TX), connected to the system manages an Ethernet network connection to an industrial PC where a software sets the working parameters and downloads raw and processed data. The main features of the system are reported in Table 2.

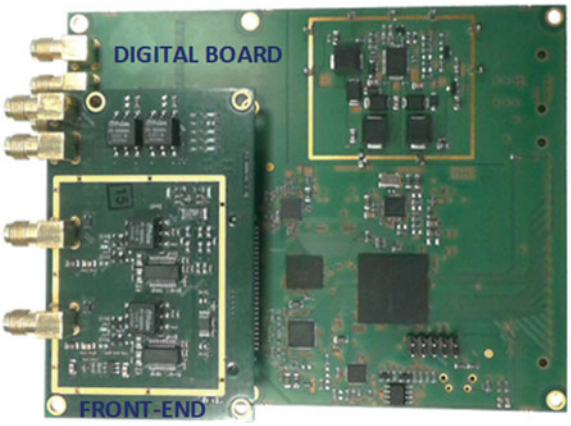

Fig. 1 System electronic boards: analog front end and digital board

3.1 Hardware Architecture

The analog front-end (Fig. 1) is subdivided in two equivalent channels, each one embeds a Transmission (Tx) and Reception (Rx) section. During the transmission, a current feedback linear amplifier is turned on to amplify ultrasound bursts up to 80 Vpp needed to excite the ultrasound transducers. In reception, the Tx amplifier is turned off to reduce noise. Low Noise Amplifier and a Programmable Gain Amplifier amplify the backscattered echoes in a range of 7 to 55 dB with bandwidth between 0.8 and 7 MHz. The selection of the Rx and Tx channels is managed by switches, controlled through the Field Programmable Gate Array (FPGA), located on the Digital board.

The Digital Board (Fig. 1), is based on the EP3C25F256 FPGA from the Cyclone family of Altera (San Jose, CA), which manages all the digital devices present on the board. A Digital Direct Synthesizer (DDS) implemented on the FPGA produced a transmission burst with programmable amplitude, frequency, number of cycles and tapering. A 14-bit resolution, 100 MSPS Digital to Analog Converter (DAC) converts and sends the burst to the analog front end. In reception, an analog to digital converter AD9265 (Analog Devices, Norwood, MA) converts at 100 MSPS with 16-bit resolution the echoes and finally the data are processed in the FPGA.

3.2 FPGA Firmware

The FPGA is programmed to produce an excitation sequence composed by 2 groups of 128 pulses at PRF1 and PRF2 = ¾ PRF1 rate according to multi-PRF method. The Nyquist limit is extended 3-fold. The FPGA processing chain coherently demodulates the samples [10] by a multiplication to two quadrature-phase sinusoidal signals, which have the same frequency as the transmission burst and it filters the in-phase and quadrature components by a Cascaded Integrator Comb filter (CIC) [11] with a programmable cut off frequency and down-sampling factor. Finally, the filtered samples are stored in the 64 MB SDRAM buffer. When enough data are stored, the multi-gate spectral analysis starts, moving from the SDRAM to the FPGA blocks of 128 complex samples acquired from the same depth. The Hanning window is applied to each block and a block-floating point complex FFT processes the results. The sums of the square of the FFT output, allow the system to obtain the power spectrum. All the available depths are processed and the results are stored in the rows of a Doppler spectral matrix. Then, at each depth, the (possibly aliased) Doppler velocities $\boldsymbol{v}_{D1}$ and $\boldsymbol{v}_{D2}$ are calculated according to the Doppler equation, Np is obtained by (4), $\boldsymbol{nN}_1$ and $\boldsymbol{nN}_2$ are read in the look-up of Table 1 (integrated in the firmware), and (7) is applied for obtaining the final de-aliased velocity. The process is repeated for the next 128 + 128 pulses.

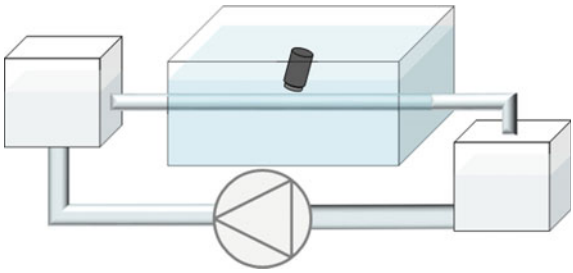

Fig. 2 Flow-rig where a peristaltic pump recirculates a fluid in an 8 mm pipe

4 Experiments and Results

The system with real-time MPRF was tested in the flow-rig depicted in Fig. 2. A peristaltic pump was used to recirculate a fluid at 60 cm/s inside an 8 mm pipe. The fluid was constituted by degassed water with dissolved 10 μm diameter plastic particles capable of generating a suitable echo to the ultrasound burst transmitted by the system. 5 MHz ultrasound bursts were transmitted with PRF1 and PRF2 set at 4 kHz and 3 kHz, respectively. A transducer was positioned at 60° with respect to the axis of the pipe. The echo signal was processed in the system by calculating an FFT every 40 us, and thus a 512-depth frame was produced in about 20 ms. A de-aliased velocity profile was calculated for every frame-pair acquired with different PRFs. The picture below (Fig. 3) shows an example of FFT frames, coded in grey levels, obtained at PRF1 (left) and PRF2 (center). The reconstructed velocity profile, which exceeds the Nyquist velocity limit (red vertical dashed line), is reported on the right.

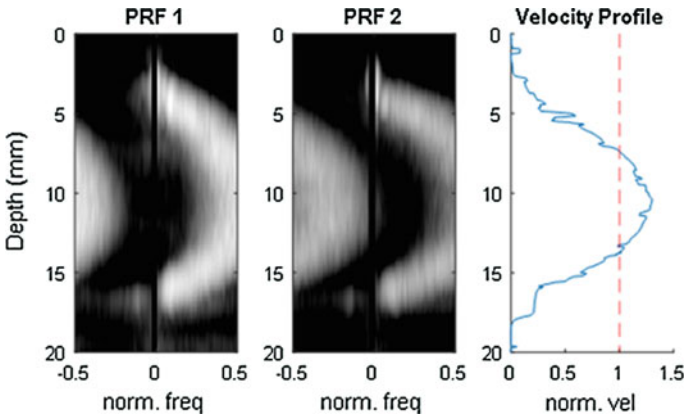

Fig. 3 Left: Aliased profile obtained at PRF1. Center: Aliased profile obtained at PRF2. Right: Reconstructed velocity profile

5 Conclusion

A system capable to evaluate in real-time velocity profiles of industrial fluids that flow in a pipe with velocity exceeding the Nyquist limit, was presented. The reconstruction of the de-aliased velocity profiles was tested with multi-PRF method on a flow-rig by investigating a fluid flowing at 60 cm/s. The extended capability of the MPRF real-time implementation, and the FPGA programmable architecture make the system is ideal for a wide range of on-site industrial applications. Indeed, it is an essential part of the Flow-Viz^{TM} [12] system, designed to characterize opaque, non-Newtonian industrial fluids, currently under test in several production plants.

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Model-Order Reduction Procedure for Fast Dynamic Electrothermal Simulation of Power Converters

A. P. Catalano, M. Riccio, L. Codecasa, A. Magnani, G. Romano, V. d'Alessandro, L. Maresca, N. Rinaldi, G. Breglio and A. Irace

Abstract Thermal Feedback Blocks represent an efficient means to perform thermal and electrothermal analyses of power converters, for which the adoption of strategies relying on 3-D numerical tools is too onerous or even impossible. In this work, we describe a RC-based thermal network extracted with a model-order reduction procedure improving the conventional Foster and Cauer solutions, which is used for the study of a DC/DC boost converter. The accuracy of the proposed approach is verified by comparing: (i) the output of purely-thermal simulations with those obtained through a commercial software based on the finite-element method, and (ii) electrothermal simulation results with measurements.

Keyword Model-Order Reduction (MOR) · Thermal Feedback Blocks (TFBs) · Electrothermal simulations · IGBT power module · Boost converter · Thermal modeling

1 Introduction

Devices, circuit and systems for power applications are characterized by high operating temperature due to the large dissipated power. The temperature increase entails electrothermal (ET) effects that reduce the performance, reliability, and lifetime [1, 2]. From a thorough industry survey, it was found that active devices are the most fragile components in most applications [3]. As a consequence, ET simulations

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coupling the thermal and electrical problems are needed to perform a thermal-aware design, especially for power module analyses [4].

Thermal Feedback Blocks (TFBs) are a good solution to perform thermal and ET simulations of electronic systems with very fast-switching inputs, for which combining a finite-element method (FEM) thermal solver with a physics-based or a circuit simulator can be computationally onerous or even unviable [5]. TFBs describe the thermal problem through an electrical equivalent (based on the thermal version of the Ohm's law), thus enabling a dynamic link between the dissipated power of devices with their temperature. ET simulations can then be performed by connecting TFBs with temperature-enabled SPICE models of the active devices [6].

TFBs are made of controlled sources, resistors and capacitors, usually in the form of Foster and Cauer networks that allow compactly modeling the system thermal step response, i.e., the thermal impedance matrix $\mathbf{Z}_{\mathrm{TH}}$. In the two aforementioned cases, (i) $\mathbf{Z}_{\mathrm{TH}}$ has to be preliminarily evaluated by long thermal-only analyses using FEM simulators, and (ii) only a few average temperatures (at chosen system points) can be obtained as output [6].

An improved approach resorting to detailed model-order reduction (MOR) techniques is here proposed, which allows obtaining TFBs that can be used in lieu of Foster and Cauer ones, with a comparable number of components, while providing a host of advantages in terms of speed and accuracy.

The paper is structured as follow: in Sect. 2, the MOR technique with the output TFB is described. A DC/DC boost converter using an IGBT power module is showed in Sect. 3 as a case study in order to verify the accuracy of SPICE-like ET analyses using the MOR approach by comparing simulations with experimental results. Finally, conclusions are given in Sect. 4.

2 TFB Extraction with MOR Technique

The proposed TFB can be extracted through a MOR process with the work-flow reported in Fig. 1.

The mesh obtained from commercial (e.g., COMSOL [7]) or open-source tools (e.g., SALOME SMESH), as well as material properties and boundary conditions are to be provided as input. The fully automatic MOR relies on Multi-Point Moment Matching (MPMM) [8, 9] and its subsequent improvements [10–12], in which the model precision is user-defined by specifying a single error parameter. The TFB topology for n heat sources (HSs) requires a small number $\hat{n}$ of RC pairs, and is given as output in the form of SPICE netlist.

The MPMM algorithm involves the solution of a limited number of thermal problems in the frequency domain (denoted as *moments*), at automatically evaluated frequencies σ_j. The TFB is equipped with the following terminals: P_1, … P_n are the power inputs for the HSs, the average temperature rises of which are given by ΔT_1, … ΔT_n; $\hat{\xi}_1,\ldots,\hat{\xi}_{\hat{n}}$ are additional variables that allow reconstructing the temperature field over all the points of mesh, and at any time instant, in a *post-processing* step.

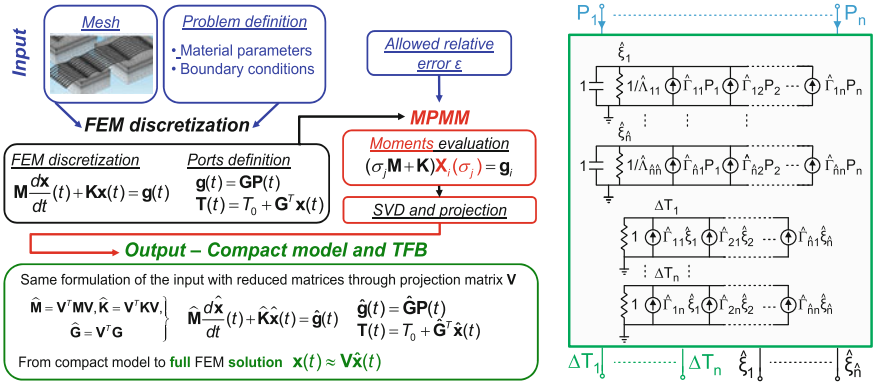

Fig. 1 Proposed TFB extraction procedure (left) and topology (right)

This approach benefits from the following advantages: (i) it is extremely fast since it does not require costly transient thermal simulations in pre-processing, while preserving all the information of the detailed FEM model; (ii) it can be used for power devices and circuits, including modules and packages, with arbitrary geometries.

3 Case Study—eT Analysis of a DC/DC Boost Converter

As a case study, a simple DC/DC boost converter, assembled from a commercial IGBT power module with devices rated at 600 V and 30 A, operating at 1 kW was considered in order to validate the proposed approach. The aforementioned topology is commonly adopted in automotive applications, battery systems, and consumer electronics [13]. As far as the passive components are concerned, the inductor and the capacitor were chosen equal to 1.17 mH and 1 mF, respectively; these values allow the converter to operate in Continuous Current Mode (CCM) with a switching frequency of 5 kHz and duty cycle 50% with small output voltage oscillations for a resistive load of 94 Ω.

3.1 Thermal Model

The IGBT power module comprising 2 IGBTs and 2 diodes (thus including 4 HSs) depicted in Fig. 2 was built in COMSOL [7] and meshed with 300 k tetrahedra.

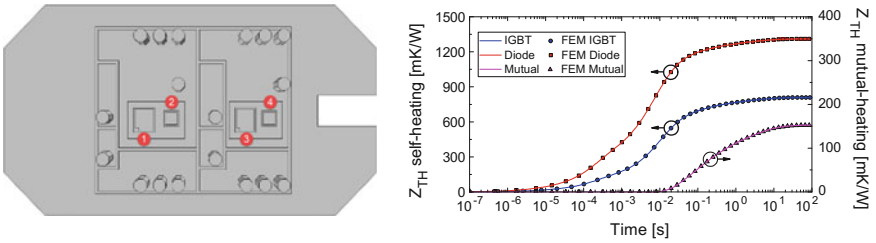

Fig. 2 (Left) Top-view of the FEM model of the commercial power module under test. IGBTs are denoted with #1 and #3, while their respective antiparalleled diodes as #2 and #4. (Right) Self-heating and mutual thermal impedances of an IGBT-diode pair: comparison between COMSOL (symbols) and TFB (solid lines) results

The module is placed on top of a heatsink, which is assumed to be at room temperature T_0 = 27°C. The thermal impedance matrix $\mathbf{Z}_{\mathrm{TH}}$ can be computed in COMSOL by invoking a conventional approach [6], i.e., by activating one HS at a time and averaging the temperature rise over all the HSs: for the case study, one $\mathbf{Z}_{\mathrm{TH}}$ row is computed in 1.5 h on a desktop PC equipped with an octa-core Intel i7-5960X, i.e., a total of $4 \times 1.5 = 6$ h is needed for the whole matrix. The TFB extraction involving 56 RC pairs for all the 4 HSs, conversely, required only 4 min with the previously-described MOR technique, while the subsequent $\mathbf{Z}_{\mathrm{TH}}$ simulations are almost instantaneous. As a result, the adoption of the proposed MOR technique allows a relevant time saving of more than one order of magnitude. Self and mutual heating thermal impedances of an IGBT-diode pair are reported in Fig. 2, which witnesses that very good agreement between TFB and COMSOL results is reached, in spite of the very short extraction time.

3.2 *Active Devices Electrical Model Calibration*

As a preliminary step toward the ET simulation of the converter, temperature-dependent models of the active devices have to be developed. The diodes are described according to [14, 15], while the IGBT model to be calibrated is an extension of the Kraus model [16–20], for which 43 parameters are needed. The IGBT temperature-dependent electrical model extraction procedure is fully-automatic: the flow-chart, as well as the model results, are depicted in Fig. 3.

3.3 *Boost Converter eT Analysis*

The ET analysis of the boost converter was performed in SIMETRIX: the simulation of 1.5 s of normal operation lasts about 2 h, in spite of the short <1 μs time step, while

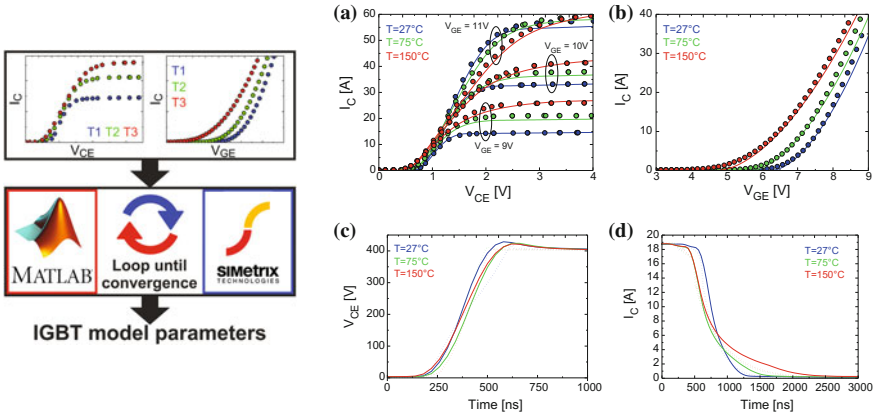

Fig. 3 (Left) Flow chart of the calibration procedure. The input is given by the measured isothermal (pulsed) static (e.g., I_C-V_{CE}, I_C-V_{GE}) as well as dynamic (e.g., turn-off) characteristics measured at different temperatures. Optimization is performed by grouping parameters in small subsets depending on their impact on the IGBT behavior, and minimizing the error between measurement input and IGBT model output with a MATLAB-SIMETRIX coupling. (Right) **a** Static output I_C-V_{CE}, **b** transfer I_C-V_{GE} characteristics, as well as **c** and **d** turn-off of the IGBTs at T = 27°C (blue), 75°C (green) and 150°C (red): excellent agreement is obtained between measurements (dots) and calibrated SPICE model (solid lines)

it would have been unviable by resorting to a relaxation process until convergence between a FEM thermal simulator and a SPICE-like tool. Figure 4 depicts the steady-state output voltage (288.1 V with input 150 V), the collector to emitter voltage and collector current for IGBT1: a good match can be seen between computed and measurement data. In addition, the simulated steady-state temperatures match the ones obtained from the ET simulation, as shown in Fig. 5. Figure 5 also depicts the temperature maps over the active devices computed in a *post-processing* stage at three different time instants: $t_1 = 8$ ms, $t_2 = 60$ ms, and $t_3 = 1.5$ s.

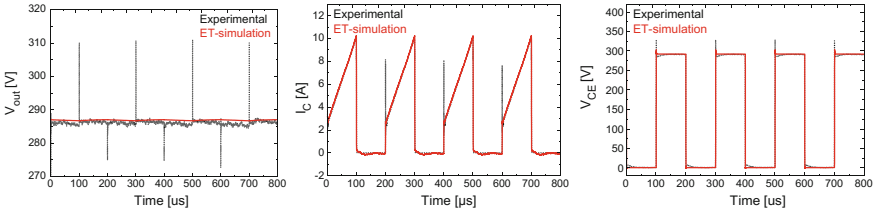

Fig. 4 ET (solid) versus measurement data (dots) for the boost steady-state behavior

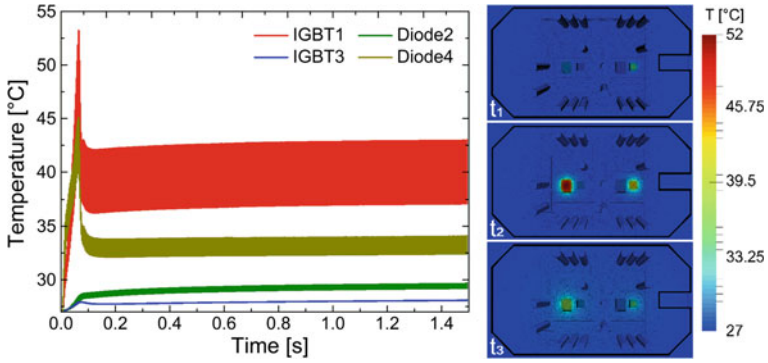

Fig. 5 Temperature as obtained from the ET simulations: waveforms (left), and maps (right)

4 Conclusions

A MOR procedure has been presented to extract optimized TFBs that enable the circuit designer to perform accurate, yet fast, dynamic ET analyses of power circuits at module and system levels. Purely-thermal simulations benefit from a speedup of more than one order of magnitude in CPU time with respect to a FEM tool with negligible error. ET simulations of a boost converter have been performed by: (i) extracting the TFB of a commercial module; (ii) calibrating temperature-dependent IGBT and diode electrical models with measurement data; (iii) building and simulating the whole circuit in SIMETRIX. Despite the time step shorter than 1 μs, only 2 h were needed for the full ET simulation, which has been found to describe measurements with good accuracy. The proposed simulation strategy can be also suggested to describe the behavior of power devices and circuits operated under harsh conditions, like in e.g., short-circuit and unclamped inductive switching tests.

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The Microarchitecture of a Multi-threaded RISC-V Compliant Processing Core Family for IoT End-Nodes

Abdallah Cheikh, Gianmarco Cerutti, Antonio Mastrandrea, Francesco Menichelli and Mauro Olivieri

Abstract Internet-of-Things end-nodes demand low power processing platforms characterized by heterogeneous dedicated units, controlled by a processor core running multiple control threads. Such architecture scheme fits one of the main target application domain of the RISC-V instruction set. We present an open-source processing core compliant with RISC-V on the software side and with the popular Pulpino processor platform on the hardware side, while supporting interleaved multi-threading for IoT applications. The latter feature is a novel contribution in this application domain. We report details about the microarchitecture design along with performance data.

Keywords Microprocessors · RISC-V · FPGA · IoT · Multi-threading

1 Introduction

Internet-Of-Things (IoT) end-node design demands low-power low-cost specialized processors [1–3]. Typical IoT end-node software runs on platforms integrating specialized units, scratchpad memories [4] and I/O units, controlled by a processing core executing multiple control threads in parallel [5], resembling the architecture depicted in Fig. 1. In such perspective, the growing interest for an extendable microprocessor instruction set has led many IoT companies to support the RISC-V open standard [6].

In this work, we present the microarchitecture solutions adopted in an open-access RISC-V compatible processor family supporting multi-threaded execution in a single core, targeting the implementation of IoT end-nodes running a limited number of concurrent control loops.

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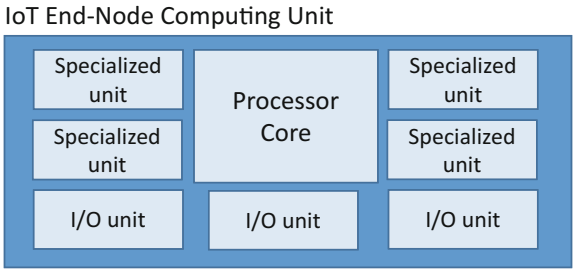

Fig. 1 Concept of specialized digital platform for local processing in IoT applications

2 Architecture Design Specification

2.1 Overview

The Klessydra processing core family features full compliance with the RISC-V instruction set on the software side, and with the existing Pulpino System-on-Chip [7] on the hardware side. To date, the Klessydra family includes a single-thread core, Klessydra-S0, and a set of multi-threaded cores, Klessydra-T0, available in different implementations. All the cores of the family have been synthesized and tested on Xilinx Series 7 FPGA devices; an IC prototype design is in progress.

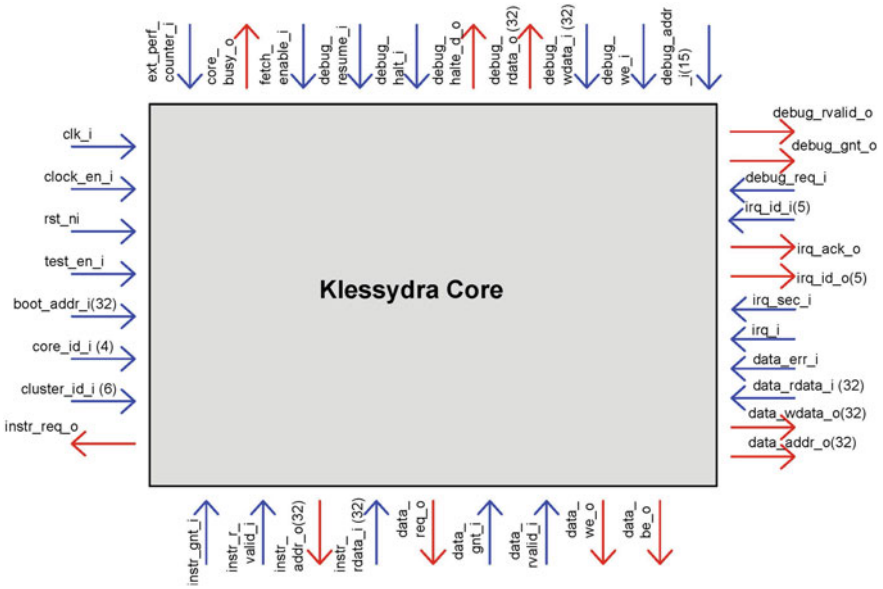

Fig. 2 Klessydra processing core pinout

Table 1 Summary of RISC-V instructions supported by Klessydra cores

Opcode	Funct 3/7/12 instruction operation field	Format type
OP_IMM	ADDI/SLTI[U]/ANDI/ORI/XORI/SLLI/SRLI/SRAI	I
OP	ADD/SLTI[U]/AND/OR/XOR/SLL/SRL/SRA/SUB	R
LUI	–	I
AUIPC	–	I
JAL	–	UJ
JALR	–	I
BRANCH	BEQ/BNE/BLT[U]/BGE[U]	SB
LOAD	LW/LH[U]/LB[U]	I
STORE	SW/SH/SB	S
MISC_MEM	FENCE/FENCE_I	I
SYSTEM	*PRIV*: "ECALL/EBREAK/MRET/WFI"/CSRRW/CSRRS/CSRRC/CSRRWI/CSRRSI/CSRRCI	I
AMO	AMOSWAP.W	R

Klessydra cores implement the 32-bit integer RISC-V M-mode instruction set. The core interface is signal-to-signal compatible with the Pulpino microprocessor platform, and as such it is the same as RI5CY core's. The pinout of the of a typical Klessydra core contains 321 I/O signals (Fig. 2).

Klessydra T0 cores implement interleaved multi-threading, i.e. at each clock cycle a new instruction is fetched from a different hardware thread. The T0 core synthesizable code is parameterized in order to have different implementations available, labelled as Klessydra-T0*BS* where *B* is the value of the Thread Pool Baseline (minimum number of active threads for stall-free pipeline operation) and *S* is the value of the Thread Pool Size (maximum number of active threads). Presently, the publicly available implementations are T022, T023, T024, T033, T034, while T012, T013, T014 are internal designs used for evaluation purposes.

2.2 Supported Instruction Set

Klessydra cores fully support the RV32I Base Integer Instruction Set V2.2, the M-mode privileged instruction set V1.10, and one operation of the Optional Atomic Instruction Extension RVA for thread synchronization (absent in S0 core). Table 1 reports the list of instructions implemented. Details on the operations of each instruction can be found in the RISC-V specification documents [8, 9].

3 Microarchitecture Building Blocks

Without loss of generality, the following description refers to the Klessydra-T023 implementation, according to Fig. 3.

3.1 FSM_IF

The FSM_IF state machine manages instruction fetch and is able to supply one instruction per cycle when coupled with a program memory capable of one access per cycle. Instruction are 32-bit word aligned. Compressed instruction format is not supported and no prefetch logic is present. The FSM_IF unit may stall the subsequent pipeline stages if the program memory access takes longer than one cycle.

The FSM_IF unit is not aware of multiple program counters corresponding to the different hardware threads, but simply performs the memory access with the instruction address provided by the program counter update units. The hardware thread id value (*harc*) is passed "as is" to the subsequent pipeline stages.

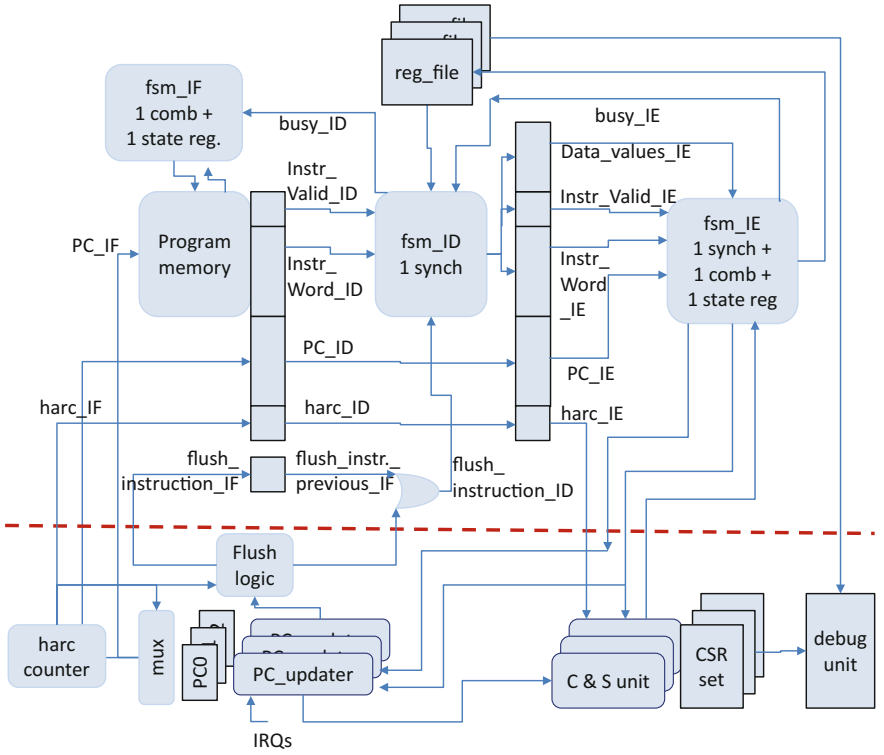

Fig. 3 Microarchitecture scheme (Klessydra-T023)

3.2 *FSM_ID*

The FSM_ID is a single-state synchronous unit that concurrently performs operand data fetch from the register file along with instruction operation decoding.

The decoded operation is passed to the subsequent pipeline stage in a one-hot coding format, thus generating considerable flip-flop count amplification at the advantage of largely optimizing the critical path in the architecture.

3.3 *FSM_IE*

The FSM_IE state machine handles execution/writeback of instructions. The unit can be in one of the following states:

Sleep state: core idle, waiting for the *fetch_enable_i* signal or an interrupt request;
Reset State: initial state of the core before it fetches the first instruction;
Debug State: core now is in debug mode, controlled by the debug inerface;

Normal State: The state where the processor is decoding/executing instructions;
Data Grant: core waiting for a grant signal to initiates new memory access;
Data Valid Waiting State: core waiting for data from the memory;
CSR Instruction Wait State: core handling CSR instruction;
WFI Wait State: core waiting for an interrupt to arrive (S0 core only).

The branch delay slot is managed by automatically flushing the fetched instructions *belonging to the branching thread*, when the Thread Pool Size is insufficient to avoid branching hazards. The microarchitecture does not implement hardware interlocks for managing data dependencies. When the active threads are less than the Thread Pool Baseline value, void threads (i.e. performing null operations) are inserted in the instruction pipeline to avoid data hazards and guarantee correct operation. Alternatively, thread data consistency may rely on classic RISC instruction scheduling to avoid hazards, as was done in [10].

3.4 Data Register File

Klessydra cores have 32×32-bit wide registers ranging from registers $\times 0$ to $\times 31$. Register $\times 0$ is statically bound to 0 and can only be read. Notably, the data register file is necessarily replicated on a per-thread basis.

3.5 Program Counter Management Units

In Klessydra cores the next program counter for each hardware thread is set by the *pc_updater* units. This synchronous single-state unit updates the program counter value according to the events raised by the following signals coming from other units:

- Branch Signals: *set_branch_condition, branch_condition_pending*.
- Exception Signals: *set_except_condition, set_mret_condition*.
- WFI Signals: *set_wfi_condition, wfi_condition_pending*
- Interrupt Signals: *irq_pending, served_irq*.
- Boot Signal: *rst_ni*

If none of the above are active, the unit simply increments the program counter of 4 units.

A dedicated hardware thread counter (*harc*) governs the interleaving of threads in the instruction fetch. Inactive threads (i.e. waiting for interrupt) are skipped; however when active threads are too few to guarantee data-hazard avoidance, then NOPs are automatically interleaved in the pipeline to avoid the hazards.

Table 2 Control and status registers supported by Klessydra cores

Name	R/W	Description
MSTATUS	R/W	Status register
MEPC	R/W	Exception program counter
MCAUSE	R/W	Trap cause
PCER	R/W	Performance counter enable
MESTATUS	R/W	Exception status register backup
MHPMCOUNTER	R/W	Performance-monitoring counter
MHPMEVENT	R/W	Performance-event selector
MCPUID	R	Cpu description
MIMPID	R	Implementation description
MHARTID	R	Hardware thread integer id
MIP	R/W	Interrupt pending type
MTVEC	R/W	Trap-handler base address
MIRQ	R	Ext. interrupt request number
MBADADDR	R/W	Misaligned address value

3.6 Control and Status Registers Units

Each CSR unit is a state machine handling three kinds of operations on the control/status registers: CSR instruction, exception/interrupt events, and MRET instructions. Klessydra cores implement a subset of the control and status registers specified in the RISC-V privileged specification, along with some additional CSRs specifically needed for the core operations and/or for compliance with the Pulpino microprocessor platform. Such extension is composed of the MIRQ and PCER registers. The whole set of CSRs implemented in the Klessydra cores is reported in Table 2.

3.7 Debug Unit

The cores feature a debug unit capable of taking control of the instruction execution after an external debug request or the execution of an EBREAK instruction. The unit can operate in two modes, namely *halt mode* in which the core stops after the execution of the last fetched instruction, and *single step mode* in which the core executes one instruction at each command of the debug unit. When the debug unit is active (and the Fsm_IE is in the debug state), the data register file is accessible by the debug unit. The debug unit is compliant with the Pulpino debug interface.

Table 3 Performance results. ("–" = not applicable)

Core module	Pipeline stages	Cycle time [ns]	Average throughput (MIPS)			
			1 thread	2 threads	3 threads	4 threads
S0	2	12.0	71.84	–	–	–
T012	2	12.7	67.88	78.74	–	–
T022	3	8.9	48.43	96.86	–	–
T013	2	13.9	62.02	71.94	71.94	–
T023	3	9.7	44.44	88.87	103.09	–
T033	4	7.3	30.58	59.05	118.09	–
T014	2	15.9	54.22	62.89	62.89	62.89
T024	3	9.4	45.85	91.71	106.38	106.38
T034	4	7.4	30.16	58.25	116.50	135.14

4 Performance

Table 3 reports the throughput obtained by different implementations of the core microarchitecture. The clock cycle time refers to the present FPGA implementations on a Xilinx Series 7 device. Throughput results refer to the execution of multiple threads constituted by basic integer computational kernels. When running at baseline thread count (i.e. with active threads = Thread Pool Baseline), the four-stage-pipeline cores exhibit no pipeline stalls, while the other cores exhibit just one stall cycle per executed branch. Furthermore, according to the design expectations, the microarchitectures with higher thread pool baseline exhibit a shorter clock cycle time, as a consequence of shorter pipeline stage critical path.

5 Conclusions

We showed the microarchitecture solutions adopted in implementing a family of processing cores compliant with RISC-V integer 32-bit instruction set and with the popular Pulpino System-on-Chip platform. Performance analysis was also reported, showing the trade-offs between different micro-architecture organizations and minimum/maximum number of threads in the target application software. Future work will be in the power efficiency analysis and in the IC implementation of the best performing micro-architecture modules. The presented work is a step towards the realization of fully open design solution database for IoT system design, from microprocessor cores to printed circuit boards and software layers.

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Analysis and Simulations of mmW Transceiver for System-in-Package Communications

Sergio Saponara, Gabriele Ciarpi and Filippo Giannetti

Abstract This paper uses an analytical approach to provide a performance analysis of a millimeter-wave short-range link for System in Package (SiP) applications. Thanks to an analytical modeling of the real Si-integrated antenna, an easy-to-use expression of the Intersymbol Interference (ISI) is derived and used to estimate the performance of the communication system. The performance of two different low-complexity binary constellations (bipolar and unipolar symbols) and four different pulse shapes, i.e., No-Return-to-Zero (NRZ), Return-to-Zero (RZ), Manchester (MAN) and Root-Raised-Cosine (RRC) are compared to highlight the different performance in relation to the tight area and power constraints.

Keywords System in package · mmWave · Wireless links

1 Introduction

System in Package (SiP) is a flexible technology that allows integrating, into a single package, systems fabricated with different technology and passives. This allows to decrease the used area while keeping high performance and low cost. For the past 40 years the cost per transistor has declined by 25–30% every year thanks to scaling and material innovation. However, the most advantage technologies below 28 nm require also structural innovations (as FDSOI and FinFET), which reduce and cancel this trend [1]. The SiP is the key to improve the electronic performance keeping a low cost. The market of the packaging is increased from 2010 to 2017 of 18.9 B$ and an increase of 13.6 B$ is forecasted for the next three years [1]. The growing computation demands of scientific and commercial workloads in both speed and volume requires the integration of more processor cores and very large capability memories. The required off-chip I/O bandwidth doubles about every two years, significantly

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exceeding the growth rate of the number of pins due to packaging limitations [2]. The integration of these systems in a SiP reduces the number of off-chip I/O pins shifting the signal-integrity issue inside the package. This trend implies a growth in the inter-/intra-chip communication bandwidth, which has been a major challenge in recent decades. The major limitation of electrical interconnection is the low bandwidth-distance product of the metallic medium. Therefore, its energy efficiency drops down significantly when transmitting large throughput over 1 mm distance due to the high channel losses. In addition, the micro-balls to interconnect stacked chips and the bonding wires to interconnect side-by-side chips have hardly controllable electrical parameters. This due to larger tolerance of mechanical process than electrical ones, which reduces the reliability of high-speed communication networks. The optical fiber has very wide bandwidth-distance product, which makes it usable for long distance communications. However, the issues of system integration and overhead, such as electronic-to-optical and optical-to-electronic conversion, environment sensitivity, and high cost of short-distance communications make this technology not recommended for many applications [3]. In this paper, a feasibility study of millimeter-Wave Network in Package (mWNiP) is presented. Section 2 presents the model and the analytical analysis of the communication system. In Sect. 3 the performance of the different configuration is evaluated and the conclusions are drawn in Sect. 4.

2 Model of the Communication System

The proposed wireless communication system operates in the unlicensed band around 57.5 GHz, i.e., in the vicinity of a peak of oxygen absorption that introduces an attenuation of about 15 dB/km. Therefore, this band can be effectively used only for short-range communications [4–7], enabling the spatial-separation multiplexing. The block diagram of the communication system, shown in Fig. 1, is made of a transmitter, an integrated antenna for the transmitter, the propagation channel model, the channel's additive white Gaussian noise (AWGN), the receiver antenna and the receiver featuring the pulse matched filter. The subsequent signal sampler and data detection blocks are not shown in the diagram.

Due to the low-area and low-power constraints, two low-complexity binary constellations are implemented in the system, one with unipolar symbols and one with bipolar symbols. A comparison between four different pulse shaping filters, i.e., non-return-to-zero (NRZ), return-to-zero (RZ), Manchester (MAN) and root-raised

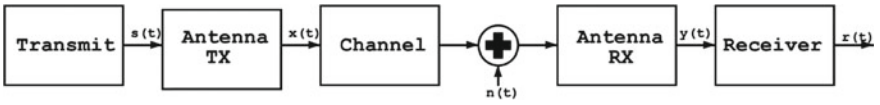

Fig. 1 Communication system

cosine (RRC), is also carried out to highlight the best solution. The complex-valued baseband representation of the information-bearing transmitted signal is in Eq. (1).

$$\tilde{s}(t) = A \sum_{k=-\infty}^{+\infty} \tilde{D}_k * p(t - kT_s) \tag{1}$$

where A is an amplitude coefficient to set the average energy-per-symbol, $\tilde{D}_k = D_k^{(I)} + jD_k^{(Q)}$ is the kth information-bearing transmitted symbol (represented as a complex-valued random variable), $p(t)$ is the impulse response of the transmitter's symbol shaping filter and T_s is the symbol interval. The I/Q modulated signal at the output of the transmit antenna is shown in Eq. (2).

$$x(t) = s(t) \otimes h(t) = \left[s^{(I)}(t) \otimes \hat{h}(t)\right] \cos(2\pi f_0 t) - \left[s^{(Q)}(t) \otimes \hat{h}(t)\right] \sin(2\pi f_0 t) \tag{2}$$

where $h(t)$ is the impulse response of the transmit antenna and $\hat{h}(t)$ is the real-valued impulse response of a low-pass (LP) filter, $s^{(I)}$ and $s^{(Q)}$ are the I and Q components of $\tilde{s}(t)$. The signal at the output of the receive antenna (which is assumed identical to the transmit one) is also affected from AWGN, see Eq. (3).

$$y(t) = \left[\frac{x(t)}{PL} + n(t)\right] \otimes h(t) = y^{(I)}(t) * \cos(2\pi f_0 t) - y^{(Q)}(t) * \sin(2\pi f_0 t) \tag{3}$$

where PL is the propagation path loss and $n(t)$ is the band-pass complex-valued random process representing the AWGN with two-sided power spectral density $N_0/2$. The I/Q signal components are then passed through a filter matched to the symbol pulse shape obtaining the result in Eq. (4).

$$\begin{aligned} \tilde{r}(t) &= \tilde{y}(t) \otimes p(t) \\ &= \frac{A}{PL} \sum_{k=-\infty}^{+\infty} D_k^{(I)} * \boldsymbol{g}(t - kT_s) + w^{(I)}(t) + \mathrm{j} \frac{A}{PL} \sum_{k=-\infty}^{+\infty} D_k^{(Q)} * \boldsymbol{g}(t - kT_s) + \mathrm{j} w^{(Q)}(t) \end{aligned} \tag{4}$$

where $\boldsymbol{g}(t) = p(t) \otimes \hat{h}(t) \otimes \hat{h}(t) \otimes p(t)$ is the overall shape of the received pulse, $w^{(I)}(t)$ and $w^{(Q)}(t)$ are the I/Q components of the band-pass filtered noise process $\tilde{w}(t) = \tilde{n}(t) \otimes \hat{h}(t) \otimes p(t)$. The signal is then sampled at instants $t_i = iT_s$, yielding the following sequence of samples (Eq. 5).

$$\tilde{r}_i = \frac{A}{PL} \tilde{D}_i \boldsymbol{g}(i) + \frac{A}{PL} \sum_{\substack{k=-\infty \\ k \neq 0}}^{+\infty} \tilde{D}_k * \boldsymbol{g}(i - kT_s) + \tilde{w}_i \tag{5}$$

where the first term at the right-hand side is the useful data sample, the second is the intersymbol interference (ISI) and the third is due to AWGN noise $\tilde{w}_i = w^{(I)}(t_i) + \mathrm{j} w^{(Q)}(t_i)$. The $\boldsymbol{g}(t)$ function plays a very important role in the communication system

as it determines the amount of the ISI, which instead is typically neglected in a lot of system models.

2.1 Antenna Modelling

One of the strong constraints of this application is the very small size of the system and this collides with the integrated antenna size and its performance. The two antennas used in the system are on-chip zig-zag antennas [8], whose area is about 400 μm × 80 μm. For the purpose of analytical performance evaluation, the antenna gain (Fig. 2) is well approximated by the Gaussian shape shows in Eq. (6).

$$|H(f)|^2 = \begin{cases} G_0 * \mathrm{e}^{-\ln 2\left(\frac{f-f_0}{B}\right)} & f>0 \\ G_0 * \mathrm{e}^{-\ln 2\left(\frac{f+f_0}{B}\right)} & f<0 \end{cases} \tag{6}$$

where $G_0 = -26.56\text{dB}$, $f_0 = 57.5\text{GHz}$ and the RF half-band is $B = 8\text{GHz}$.

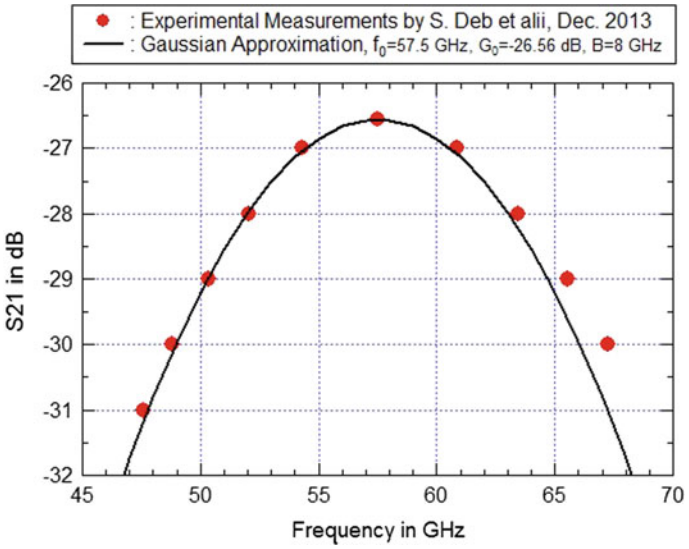

Fig. 2 Approximation of the antenna gain with a Gaussian gain shape

2.2 Intersymbol Interference

The ISI arises from the bandlimited feature of the whole transmission channel, including the antenna. Actually, passing a signal through such a bandlimited channel results in the removal (or attenuation) of frequency components outside the RF bandpass. This filtering of the transmitted signal affects the shape of the time-domain information-bearing pulses that arrive at the receiver. For instance, filtering a time-limited rectangular pulse changes the shape of the pulse within the first symbol period, and it is also spreads it out over the subsequent symbol periods. When a message is transmitted through such a channel, the spread pulse of each individual symbol will thus interfere with subsequent symbols. The $g(t)$ pulse shape in Eq. (4) takes into account this phenomenon, so comparing the $g(t)$ functions of the different pulse shapes we can evaluate the ISI level. The Eqs. (7, 8 and 9) display the analytical functions $g(t)$ obtained thanks to the Gaussian antenna approximation. For the RRC pulse only, a numerical approximation of the $g(t)$ function is derived. Figure 3 presents the function $g(t)$ for the four pulse shapes taken into account in the paper, and the relevant samples taken at symbol rate $g(k) = g(kT_s)$.

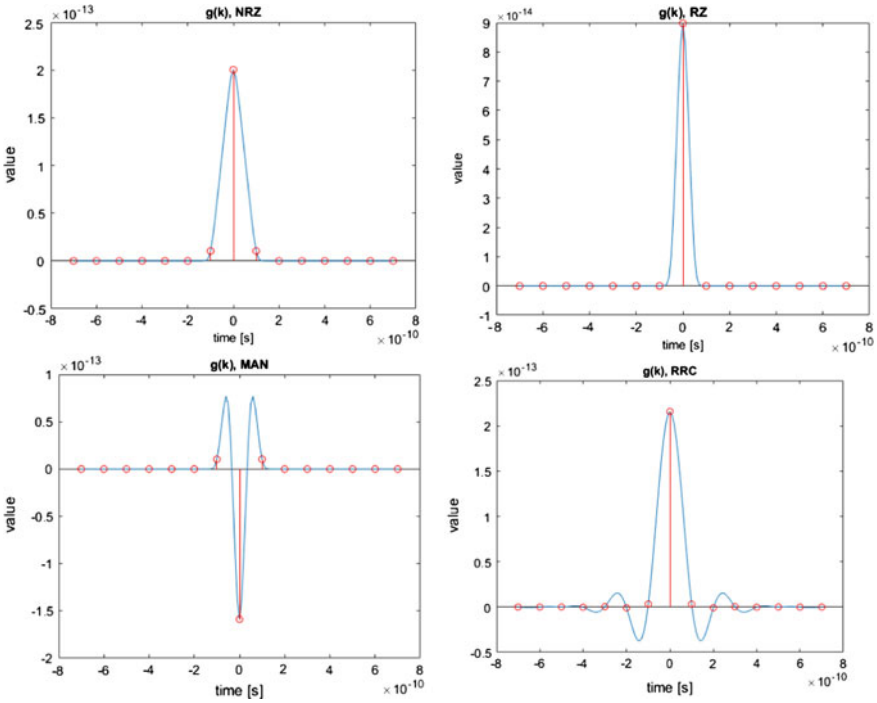

Fig. 3 Plots of $g(t)$ and $g(k)$ for the four pulse shapes taken into account in the paper

$$\text{NRZ} \quad g(t) = G_0[\Psi\left(\frac{t+T_s}{\sigma'}\right) + \Psi\left(\frac{t-T_s}{\sigma'}\right) - 2\Psi\left(\frac{t}{\sigma'}\right)]\sigma' \tag{7}$$

$$\text{RZ} \quad g(t) = G_0[\Psi\left(\frac{t+T_s/2}{\sigma'}\right) + \Psi\left(\frac{t-T_s/2}{\sigma'}\right) - 2\Psi\left(\frac{t}{\sigma'}\right)] \tag{8}$$

$$\text{MAN} \quad g(t) = G_0 6[\Psi\left(\frac{t}{\sigma'}\right) - 4\Psi\left(\frac{t+\frac{T_s}{2}}{\sigma'}\right) - 4\Psi\left(\frac{t-\frac{T_s}{2}}{\sigma'}\right) + \Psi\left(\frac{t+T_s}{\sigma'}\right) + \Psi\left(\frac{t-T_s}{\sigma'}\right)]\sigma' \tag{9}$$

where all the pulse expressions are function only of $\Psi(t) = \int_y^\infty Q(z)dz$ and $\sigma' = \frac{\sqrt{2*\ln(2)}}{2\pi*B}$.

The RRC pulse has lower ISI than the other pulses (i.e., $g(kT_s) << g(0)$) if the pulse is sampled with ideal symbol-timing synchronization, otherwise the ISI increases. The NRZ impulse has higher ISI, but lower sensitivity to synchronization errors.

3 Communication Link Performance

Some tests are done to highlight the performance of the communication system under different configurations. Figure 4 shows the Symbol Error Ratio (SER) at 10 Gbps, with transmitter-receiver separation of 1 cm, and 2 dB noise figure of the receiver. The bipolar constellations (−1, 1) have lower SER than the unipolar (0, 1) ones because the symbols gap is higher. However, they require more complex electronic system, so more area. Thanks to its limited power spectral density, the ISI of the RRC pulse is lower than that of the others and so it is preferable. However, the implementation of the RRC filter requires more area and this goes against the system constraints. The NRZ pulse has a SER close to that of the RRC pulse without using shaping filters and this increases its usefulness, reducing the area overhead. Considering an acceptable SER of 10^{-6}, Table 1 shows the transmitted power required for different configurations of the system using a bipolar NRZ pulse.

4 Conclusions and Future Works

The mWNiP are very interesting communication systems to connect more dies inside the package, reducing the effects of the mechanical issues (tolerances, stress, material compatibility) on the reliability of the electronics devices. This work, based upon an analytical solution, gives some formulas to estimate the ISI of the system. In addition, a comparison of the communication performance of the different system configurations is done to highlight the best configuration in relations with the strong system constraint. The compromise between area and performance highlights that the bipolar NRZ is the best solution for this application. However, Table 1 shows that the transmitted power to achieve a SER = 10^{-6} could be too high for the application, but

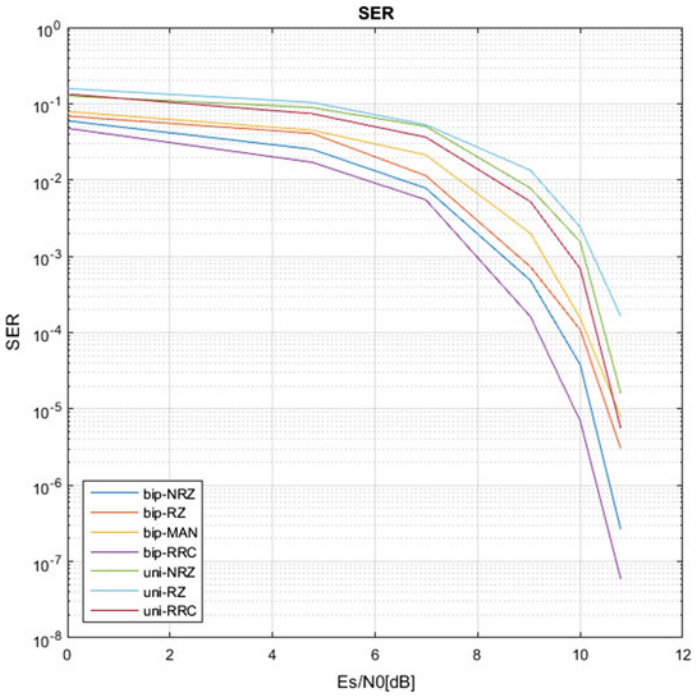

Fig. 4 Symbol error ratio of the system configurations at 10 Gbps, 1 cm distance and 2 dB receiver's noise figure. As expected the best performance are achieved with bipolar symbols. The RRC and NRZ pulses have the lowest SER as expected from the $g(t)$ pulse

using an antenna with higher gain (from −26.56 to −16.56 dB) the required power decreases down to 0.15 dBm for 10 Gbps and to −3.51 dBm for 5 Gbps, which are more manageable values for this application. The critical element for the mWNiP is the antenna design. It must be small to be easy integrated in a chip and should have a gain higher than −15 dB. In side-by-side dies configuration (as show in Fig. 5) the wireless transmission is based only on Non-Line-Of-Sight (NLOS) propagation. This can lower the effective received power. A better study of the channel inside

Table 1 Transmitted power required for SER = 10^{-6}

Set up	Transmitted power (dBm)
10 Gbps	19.75
8 Gbps	18.75
5 Gbps	16.35
10 Gbps, antenna gain −16.56 dB	0.15
5 Gbps, antenna gain −16.56 dB	−3.51

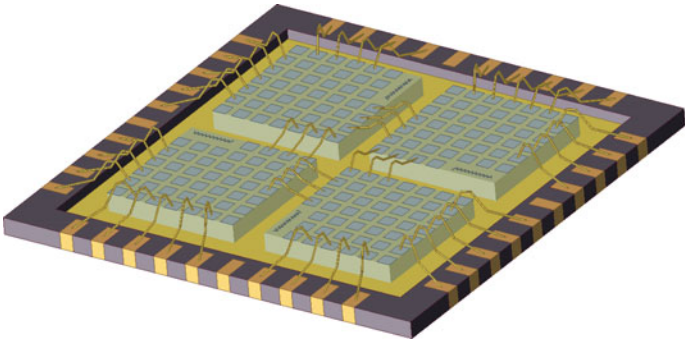

Fig. 5 System in package with four side-by-side dies and the zig-zag antennas

the package will be done, considering the high number of multipath due to package, dies, bonding wires and other surfaces. Considering an extreme number of paths, the channel response is close to Gaussian shape (Central Limit theorem) and this should be inserted in the transmission model. The increase of the communication frequency will reduce the antenna size and the use of new technology will increase the integrated antenna gain.

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Integrated Microwave Photonics: Overview and Promising Space Applications

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Abstract Photonic integrated circuits technology now enables the integration of several hundreds of optoelectronic and photonic active and passive devices on a single chip. This technology is having a disruptive impact on the field of microwave photonics with the demonstration of chip-scale complex sub-systems for generating and processing RF signals. Such integrated microwave photonic circuits exhibit features very attractive in the field of space engineering such as small size, weight, and power consumption. In this paper, the space applications of integrated microwave photonics are discussed with a special emphasis on RF pass-band filters for reconfigurable telecom payloads and delay lines for wideband beamforming.

Keywords Microphotonics · Microwave photonics · Photonic filters · Delay lines · Spacecraft engineering

1 Introduction

Since several decades, the key enabling role of photonics is well recognized in several scientific/technological areas such as telecommunications, life science, healthcare, lighting and so on. In the last years, photonics is becoming one of the most important enabling technologies also in space engineering [1].

In the satellites currently in orbit, photonic components are included in at least two sub-systems, i.e. the attitude control and the power supply sub-systems. In fact, photonic gyros based on the Sagnac effect, star trackers, sun sensors, and multi-junction high-efficiency solar cells are routinely used in Space [1]. In addition, optical payloads are widely used especially for Earth observation [2].

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We expect that in the near future, photonic devices and circuits will be included in other sub-systems forming the satellite platform such as the data processing/handling and the communications ones, and in other classes of payloads, e.g. telecom ones.

Several integrated microphotonic devices and integrated circuits for space applications are currently under investigation [3, 4], while the interest towards photonic payloads with advanced functionalities, such as entanglement-based quantum key distribution, is quickly growing [5].

In this context, integrated microwave photonics (MWP) is becoming more and more attractive because chip-scale integrated photonic circuits carrying out very complex functionalities with a very good performance can be implemented by this technological approach.

In this paper, after an overview of integrated MWP, two of its promising space applications are discussed.

2 Overview of Integrated Microwave Photonics

Integrated MWP brings together radio-frequency (RF) engineering and optoelectronics and photonics aiming at developing high-performance chip-scale photonic integrated circuit for generation, processing, control, and distribution of microwave signals [6]. By integrated MWP, complex functionalities that may not be realizable in the electrical domain can be implemented by exploiting wide bandwidth and low loss characteristics offered by the microphotonic technologies.

The application domain of integrated MWP is currently very wide including telecommunications, defense, sensing, and medicine, in addition to the most well-established application field of aerospace and defense.

The most interesting recent advances of integrated MWP are in the fields of RF waveform generation, analog-to-digital conversion, RF filtering, and wideband beamforming. Some selected recent achievements in this field are briefly discussed in the Sect. 2.1.

2.1 Selected Recent Advances

A spectral shaper in silicon technology based on chirped waveguide Bragg gratings for continuously tunable linearly chirped microwave waveform generation has been recently designed [7]. The chip-scale integrated circuit is a key building block for RF arbitrary waveform generation.

A miniaturized optoelectronic oscillator based on a photonic resonator with a Q-factor $> 10^8$ generating a sine-wave signal at a fixed frequency in the range 34–36 GHz, with a phase noise equal to −108 dBc/Hz at 10 kHz offset from the carrier, has been reported in [8]. This component has a performance that is not achievable by the standard RF technology.

Two photonic sampled analog-to-digital converters operating at approximately 40 GHz with a very low jitter (of the order of 10 fs) and an effective number of bits of 7 have been recently experimentally demonstrated [9, 10]. The best electronic analog-to-digital converters have a jitter of the order of 100 fs. Thus, the photonic components exhibit an improvement of the state-of-the-art of one order of magnitude.

In the field of RF filtering, a valuable recent result is the experimental demonstration of a coherent tuneable low-pass MWP filter monolithically integrated into an InP chip [11]. This is the first fully-integrated MWP component.

A new fast (response time < 1 ns) approach for optically tuning the integrated photonic delay lines based on ring resonators has been investigated in [12]. This tuning approach is very promising in the context of ultra-fast photonic beamforming.

3 Promising Applications in Space

RF signals are widely used on board of satellites to observe the Earth by radar systems and to receive/transmit data (telecom satellites). Therefore, MWP has many space applications.

Current trends in spacecraft engineering are towards the miniaturization of sub-systems forming payloads and spacecraft buses. This is the reason why MWP components (e.g. oscillators, filters, mixers, beamformers) can be attractive for space applications only if they are manufactured by integrated microphotonic technologies and thus are chip-scale, low-power, and light.

In this section, we report on two classes of integrated MWP sub-systems for Space: Ka-band pass-band filters for flexible telecom payloads and graphene-based delay lines for RF beamforming.

3.1 Ka-Band Pass-Band Filter for Flexible Telecom Payloads

Complex payloads, which can be reconfigured after the launch according to the varying user demands in terms of bandwidth, coverage, and frequency allocation, are strongly required for future satellite communications missions [13]. In this context, the development of flexible telecom payloads is a hot R&D topic. One of the key building block of a flexible telecom payload is the reconfigurable RF front-end, including a band-pass filter (BPF) with tunable central frequency and bandwidth.

The typical requirements for the BPF to be included in such reconfigurable RF front-end, e.g. widely tunable central frequency (4–40 GHz), tunable bandwidth (from 30 to 300 MHz), and flat-top shape of the spectral response close to the central frequency [14], are very challenging for RF standard technologies. This is the reason why integrated microwave photonics is the most promising approach for implementing the BPF with the above-mentioned features.

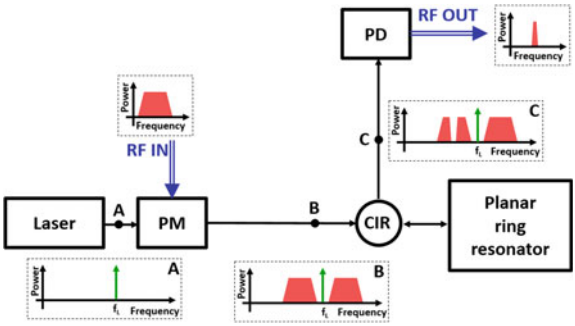

Fig. 1 Block diagram of the coherent microwave photonic band-pass filter. CIR: optical circulator. f_L is the laser frequency

We are currently developing a coherent microwave photonic BPF having the configuration shown in Fig. 1 [15]. The narrow-linewidth light wave (spectrum A), generated by the laser, is sent to a phase modulator (PM). Two sidebands are generated by the PM (spectrum B). One of the sidebands is partially filtered by a photonic notch filter implemented through a planar ring resonator. At the output of the planar ring resonator, the phase modulated signal is O/E converted by the photodiode (PD). The detection at the PD generates the filtered RF signal (spectrum C).

The hearth of the BPF is the planar ring resonator serving as photonic notch filter that should have a flat spectral response close to the resonance wavelength. Such flat spectral response is obtained by including a one-dimensional photonic crystal (1D PhC) section within the resonant path of the ring resonator. This section is placed in a symmetric position with respect to the coupling region. The presence of one or more defects within the 1D PhC generates a narrow reflection dip at the resonance wavelength inside photonic bandgap. In particular, we can obtain a flat reflection spectrum close to the resonance wavelength by engineering the defects according to Newton binomial rule [16].

The selected waveguide for the ring resonator is a silicon wire having a width of 500 nm, a height of 220 nm, and a propagation loss = 0.4 dB/cm [17]. The PhC is implemented through the square-wave modulation of the waveguide width (max width = 520 nm, min width = 480 nm). A period equal to 311 nm has been chosen to obtain the resonance wavelength λ_0 at about 1550 nm. Engineering the 1D PhC defects leads to a flat and narrow reflection spectrum. Seven defects have been introduced in the PhC according to Newton binomial rule, with a defect length of 49.4 μm.

The PhC section consists of 1024 periods and the defects have been placed at the 8th, 64th, 232th, 512th, 792th, 960th, 1016th period. The reflection spectrum of the resonant device, calculated by our model based on the transfer matrix method, exhibits a full-width-at-half-maximum (FWHM) of 10 pm, a Q-factor equal to 1.5 $\times$ 10^5, an extinction ratio equal to 15.2 dB, and a maximum ripple less than 0.5 dB within the frequency range $\lambda_0 \pm$ FWHM/4.

3.2 Graphene-Based Delay Lines for RF Beamforming

Phased-array antennas consist of arrays of stationary radiating elements that are closely spaced. By controlling the phase of RF signals feeding each antenna element, the direction of the transmitted beam can be electrically tuned [18]. Phased-array antennas are extremely attractive for several space systems, such as telecom or radar payloads. Consequently, they are widely used in space engineering.

The critical sub-system in a phased-array antenna is the network of true-time-delay phase shifters imposing tunable delays to the RF signals feeding the antenna elements. This beamforming network can be implemented in the photonic domain to avoid the beam squinting effect occurring when large-bandwidth RF signals are transmitted or received [19].

Recently, we have designed a fast tunable delay line for beamforming based on a resonant structure formed by two vertically stacked ring resonators [20]. The bottom ring is evanescently coupled to a straight bus waveguide. The delay tuning is achieved by a graphene-based capacitor placed between the rings. The resonant device is able to impose a delay up to 360 ps with a footprint of only 1.6×10^3 μm^2. The same building block has been used to design a tunable delay line, with a more complex configuration, able to impose a delay up to 920 ps [21]. The device includes a first section that is able to generate only four discrete values of delay and a second section, based on the above-mentioned resonator formed by two vertically stacked rings, able to impose a fine-tunable delay. The first section is formed by two cascaded spiral waveguides and two graphene-based Mach-Zehnder interferometer switches. The maximum delay generated by this delay line could be used to develop a Ka-band synthetic aperture radar (SAR) with a resolution of a few tens of centimeters, significantly better than the SAR systems currently in orbit.

4 Conclusions

The fundamentals and some application domains of integrated MWP have been briefly reviewed, with a special emphasis on the space application domain. Some selected recent advances on a Ka-band pass-band-filter and graphene-based fast tunable delay lines for beamforming have been presented. The encouraging results on the integrated MWP filter suggest to engineer the filter tuning and to develop the first prototype of the component aiming at experimentally demonstrate its interesting features.

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A New Recognition Procedure for Palmprint Features Extraction from Ultrasound Images

Donatella Nardiello and Antonio Iula

Abstract In this work, an improved palmprint recognition system based on 3D ultrasound images is proposed and experimentally validated. The system exploits an ultrasound gel pad as coupling medium, which results much more practical and non-invasive in real applications than water. An ad hoc recognition procedure has been derived; it uses as input a 2D image of the palmprint at a fixed under skin depth and extracts main features exploing the Frost filter and a series of morphological operations. The recognition system has been preliminarily evaluated through verification experiments carried out on an ad hoc established database composed of 75 samples from 17 different volunteers.

Keywords Biometrics · Ultrasound imaging · Image processing

1 Introduction

In the last years, the demand of automated systems based on person identification is dramatically increasing and the development of new biometric systems is growing as well [1].

Ultrasound has shown several advantages over the other technologies, including the intrinsic capability of proving a 3D representation of the biometric characteristics and of detecting life (Doppler mode). Also, ultrasound is not sensitive to surface contaminations like ink stain, dirt or oil.

In recent times, the authors have widely experimented with the possibility to acquire a volume of the human hand or finger through an ultrasound linear probe. The technique has been exploited for extracting and evaluating different biometric characteristics based on ultrasound by exploiting both piezoelectric and cMUT linear

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arrays: internal hand geometry [2], hand vein pattern [3], fingerprint [4, 5], and palmprint [5, 6].

More recently, they proposed a new system for the acquisition of ultrasound images [7] based on the open ultrasound platform ULA-OP [8], which allows nonstandard and dedicated transmit/receive strategies and is able of providing a very quick acquisition. An improved automated system, which exploit a numeric controlled pantograph, was employed to guarantee stable and repeatable measurements. That system used water as coupling medium between human hand and probe. Acquired 3D images were successively elaborated and several kinds of features that contain different 3D information of the palmprint were extracted [9, 10].

The proposed wet systems however resulted not very practical and acceptable by the user. To overcome this problem, an alternative approach for achieving volumetric images of the hand, which exploits as coupling medium an ultrasound gel pad placed between the palm of hand and the probe, has been recently proposed [11].

In the present work, a dedicated and optimized procedure for features extraction as principal lines from ultrasound images acquired with the gel based system is established and experimentally evaluated.

2 Experimental Setup

Figure 1 shows a photo of the experimental setup used for acquiring 3D ultrasound palmprint images [11].

The user's hand is leaning against an in-house developed hand-holder, where there is a window filled with a layer 20 mm thick of commercial ultrasound gel pad (Parker Aquaflex—USA). The gel pad is placed between the palm of hand and the probe and works as coupling medium. The proposed system results much more practical, comfortable and non-invasive for the user than the previous wet systems [3–7] and, consequently, the number of invalid acquisitions (mainly caused by hand motion or misplacing) was dramatically reduced.

ULA-OP (ULtrasound Advanced Platform) research scanner [8] was exploited to drive the probe LA435 (Esaote S.p.A., Genova, Italy). In order to acquire 3D ultrasound imaging data of a volume of the palm, the probe is mechanically shifted along the elevation direction while 250 B-mode images are one by one acquired and stored in an asynchronous way with respect to the continuous motion of the pantograph arm. The system is able to scan and acquire a 3D ultrasound image of $38 \times 25 \times 7$ mm^3 in about five seconds. The volumetric image is then reconstructed in post process by simply grouping the acquired B-mode images in a 3D matrix.

Figure 2a shows a 3D rendering of an acquired example where the curvatures, the ridges, the valley, the principal and secondary lines can be clearly appreciated.

2D renderings, i.e., projections of the palmprint on a plane (2D palmprints), can be also achieved. Figure 2b shows such an image extracted from the same sample.

Fig. 1 A photo of the experimental set-up

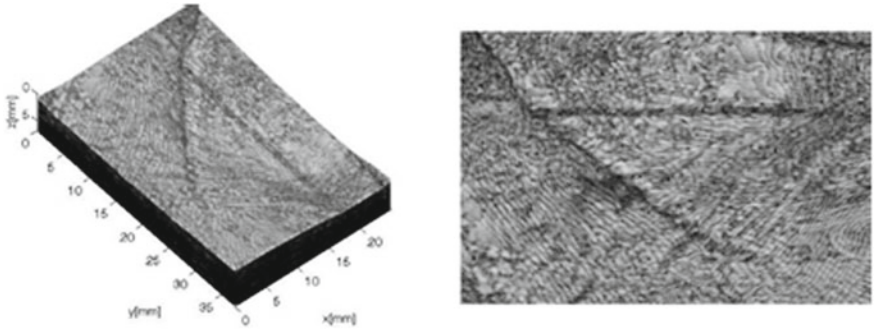

Fig. 2 Renderings from an acquired sample: **a** 3D rendering and **b** 2D rendering

3 Recognition Procedure

The input for the proposed procedure is an 8 bits gray scale image of a 2D ultrasound palmprint (542 × 814 pixels) like the one shown in Fig. 2b. The effects of main steps of the features extraction procedure on the test image are illustrated in Fig. 3. As is known, the speckle noise is a main problem in ultrasound images. In order to reduce it and to preserve the most important features as the principal lines, we proposed a procedure that is based on the Frost filter, which strikes a balance between averaging and the all-pass filter. Main successive operations were normalization of gray levels, in order to minimize differences between max and min values of the input image,

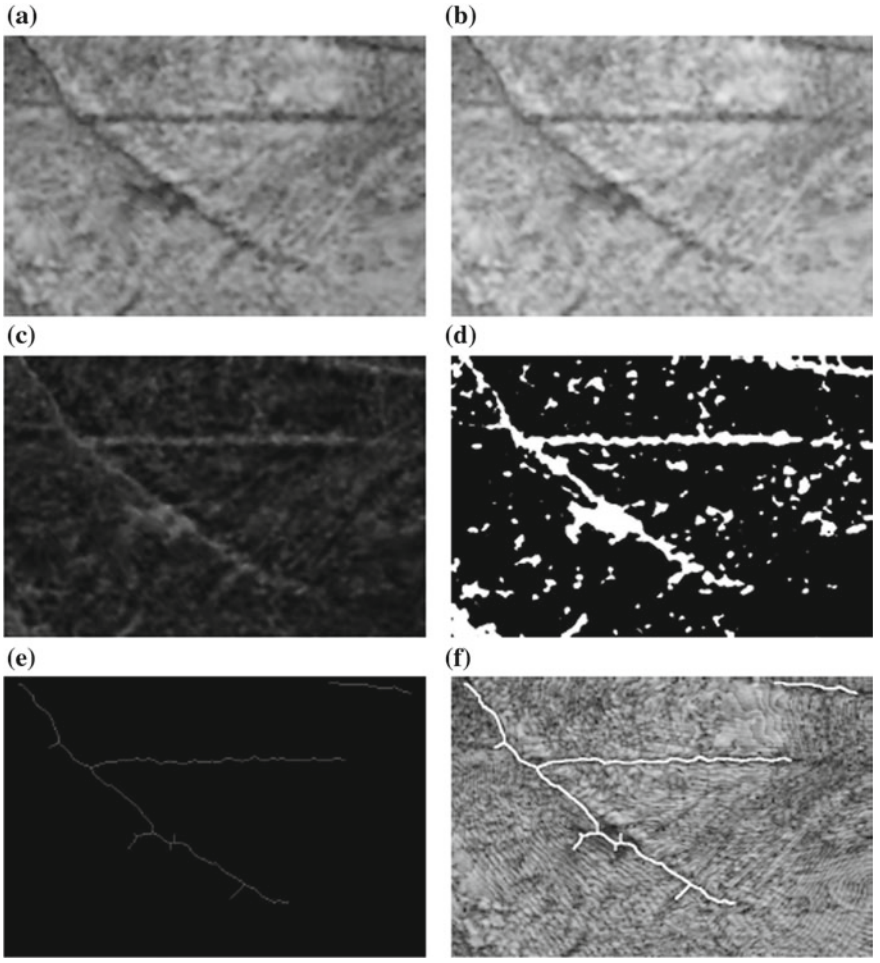

Fig. 3 Results of the main processing steps: **a** after Frost filtering; **b** after normalization; **c** after bottom hat; **d** after binarization; **e** after morphological operations; **f** template superimposed to the source palm image

and bottom-hat operation to highlight the palmprint lines that have to be detected. Finally, the image is binarized by choosing a suitable threshold and some classical morphological operations (closing, thinning and pruning) are performed. Figure 3f shows the resulting template superimposed to the source palm image. As can be seen the extracted template accurately reproduces the principal lines of the palm.

4 Recognition Results

In order to provide a first evaluation of the proposed palmprint recognition system through verification experiments, a preliminary small database, composed of 75 samples acquired from 17 different volunteers, was established.

The method used to implement the matching is the so called pixel-to-area matching [9, 10], that provides scores with values in the range [0,1]. As is known, genuine scores represent comparisons from different images that belong to the same person. Instead, impostor scores represent comparisons from different images that belong to different persons. Figure 4a shows the normalized genuine and impostor distributions and Fig. 4b False Acceptance Rates (FAR) and False Rejection Rates (FRR) versus threshold. For comparison, the same plots obtained by applying the recognition procedure derived for wet acquisitions [10, 11] on the samples are shown in Fig. 4c and d, respectively.

An important merit of the proposed procedure is the lower main value of the impostor distribution than the other one. A parameter often used to compare different

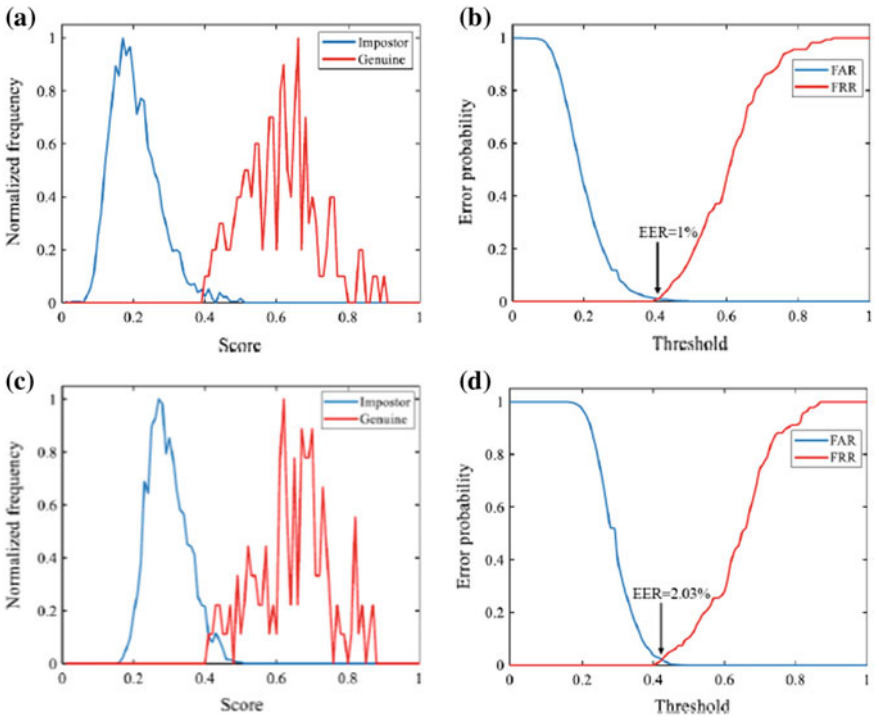

Fig. 4 Experimental impostor and genuine distributions (**a**) and FAR and FRR versus threshold (**b**) obtained with proposed procedure. Experimental impostor and genuine distributions (**c**) and FAR and FRR versus threshold (**d**) obtained with the procedure derived for wet acquisitions

algorithms is the Equal Error Rate (EER), i.e., the error obtained if the threshold is chosen in such a way that FAR = FRR. As can be seen, the proposed procedure exhibits a lower EER value. Also, it allows to obtain a smaller template, which results in a matching time 35% faster.

5 Conclusions

In this work, a new palmprint recognition procedure for ultrasound images acquired through a system that exploits gel as coupling medium is proposed and experimentally evaluated. The feature extraction method is based on the use of the Frost filter and various morphological operations. Preliminary verification results obtained exploiting a small ad hoc established database have shown improved recognition performances with respect to a previous procedure developed for wet acquisition. Next work will be devoted to increase the size of the database and to upgrade the procedure in order to extract a 3D template by exploiting several 2D images acquired at different under skin depths.

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Real-Time DNN-Based Face Identification for the Blind

Jhilik Bhattacharya, Francesco Guzzi, Stefano Marsi, Sergio Carrato and Giovanni Ramponi

Abstract We present some results from an ongoing project about face detection and recognition in an apparatus wearable by a visually impaired person. Specifically, we explore the usable equipment and we experiment on the realization of three prototypes that give the opportunity of dealing with different topics, ranging from the architecture of the network to database creation, from the reliability of the identification results to real-time operation issues.

Keywords Face identification · Convolutional neural networks · Visual impairments · Persons with disabilities

1 Introduction

We present in this paper some results from an ongoing project that studies face detection/recognition methods to build an apparatus usable by a visually impaired person.

Notwithstanding the huge progress of computer vision tools, especially since the advent of Deep Neural Networks (DNNs), techniques for face recognition that may help blind users in their relational life have not yet found practical usage. The layman perceives that this problem has been already solved, since many tools have been recently made available in the consumer world (especially in social networks) to determine the identity of people. However, the reliability that is required for an apparatus to be used by persons with disabilities (PwD) is the same as the one required by a professional user (say, a bank), while its cost must be much lower: the reliability/cost ratio is presently far from satisfactory.

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A peculiarity of the system we are realizing, which must be usable by a blind person, is the availability of a limited number of faces for the training of the network [1]. For this reason, we decided to fine-tune an existing DNN rather than train one from scratch. The same acquisition hardware will be used in the two different operating phases: during the implementation of the user's friends database (recording a video of the friend) and during the so called inference (i.e. the operative) phase of the device.

Section 2 describes different approaches that can be followed for fine-tuning; we provide detailed information about the involved procedures and the possibility of using single or multiple networks. Section 3 discusses three different realizations of the system, aiming at achieving real-time operation. Some quantitative data about the effectiveness and reliability of the identification is provided in Sect. 4.

2 Face Verification Approaches

The scenario we consider in this phase of the project is the one of a blind person who has planned to meet a friend at a predefined spot and wishes to be able to recognize him as early as possible during the approach. It can be cast as a 1-to-1 face verification task: the equipment has to acquire the scene, detect faces, compare each detected face to the faces representing the class of the specific friend the user has to meet, and inform the user if a positive answer results. Information about the reliability of the verification may be provided too, e.g. as a percent number. Before the meeting the user must activate a classifier dedicated to that specific friend. However, the scenario can also be cast in a different way, as a 1-to-N open recognition task: each detected face is compared to N classes representing N possible friends of the user's, and a single (but more complex) classifier is adopted; the recognition is deemed open because the system must be able to also label the face as not belonging at all to the set of friends [2]. In this 1-to-N context, too, some information may be provided to the user about the reliability of the identification; moreover, a suitable threshold will be needed to label out-of-the-set faces. We will show in the following some preliminary results for both the 1-to-1 and the 1-to-N approaches.

We take three different approaches towards handling the identification scenario, utilizing a feature extractor and distance classifier, a single-class verification network, and a multi-class verification network with class criteria threshold. In all the cases we start from a basic deep convolutional network, a variation of FaceNet [3], henceforth referred in this paper as the basenet. The face detection results are hence directly fed to the various finetuned version of the basenet developed for this work. For each of the cases further elaborated, the same ground truth was used.

The basenet is a feature extraction network with a 128 feature vector output. The duty of the network is to embed in the feature space faces that belong to the same individual. Thus, using the basenet as a pure feature extractor and adopting a distance classifier with a suitable threshold approach, the test feature vector x is matched with the ground truth data to verify the face. The number of classes activated for the ground truth comparison depends on how many faces the user wants to identify.

In order to get the minimal false positives we select an optimal threshold (on the network classifier output) determined using an ROC curve. We compare the result with the mean vector μ of each class and we define the acceptance ratio of the result thresholding the absolute distance above the standard deviation σ. Indeed, it has been proved that μ and σ are capable of tackling the pose and the lighting variations.

For the single-class approach, we finetune the basenet to build a 1-to-1 face verification system. In this case five separate networks for the five subjects are created by adding a single classifier to the basenet. The user in this case will be required to load the network corresponding to the person he or she wants to meet. The network will return a verification confidence of each face it sees. It is left to the user to accept a low confidence verification or to wait for a high confidence one, and in general to control the flow of information the equipment provides. Finally, in the multi class verification, we finetune the basenet to build a 1-to-5 face verification system. In this case a five-class classifier is added to the basenet. The network will return the confidence value of each of the five subjects, for each face it sees.

3 System Details

The system we developed is at its early stage but is already capable to fulfill all of the basic requirements needed:

- acquisition of a video stream from a webcam with HD resolution;
- detection of multiple faces from the scene, even if people are not perfectly in front of the camera and the faces have some yaw, pitch and roll;
- verification of one or more candidates in the scene;
- generation of a vocal output as a synthesized voice saying the name of the recognized faces and a confidence value.

Different implementations of the system have been realized, each having their own peculiarities and drawbacks: a Linux x86 64 program for a PC, a Linux (Arm-based) program for a single board computer (SBC) and an Android software for smartphone. The first two implementations are tightly coupled, since they basically run the same software.

The system was first programmed and tested on an Intel i7-6700, 3.4 GHz, quad-core CPU with 16 GB RAM, Linux OS. The fine-tuning of the basenet is carried out on this machine, within a Torch environment; the overall learning time is, on the average, around 0.33 s per sample (on the CPU). The basic system (Fig. 1a) for the inference phase is composed of three modules: a face detection tool, written in C, that utilizes the PICO [4] tool modified in order to exploit temporal information for the reduction of the false faces; a face verification tool, written in Lua; and an audio message synthesizer, which uses a Linux ESPEAK module.

Adopting a single-board PC is a convenient way to port the previously described solution on a wearable lightweight platform without having to perform substantial

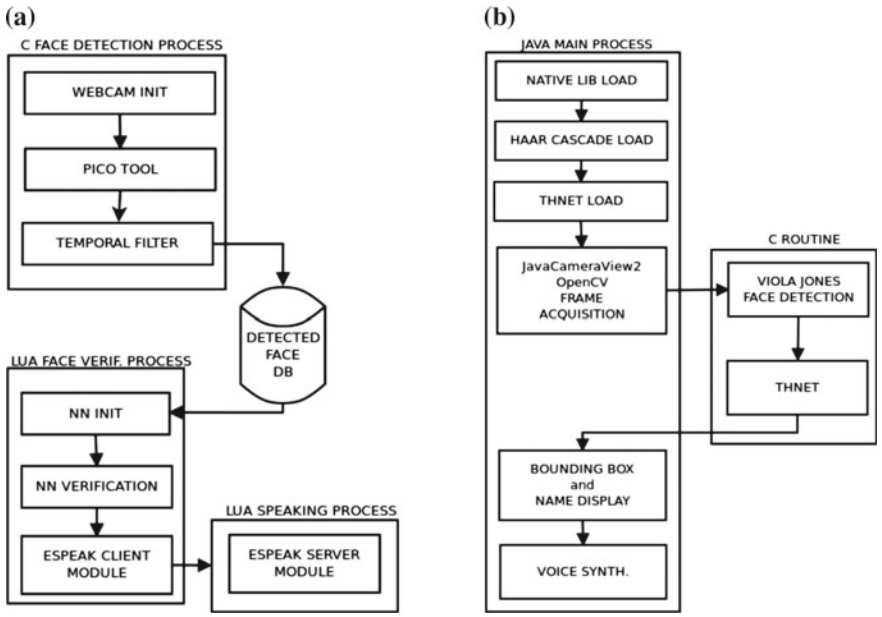

Fig. 1 Processing scheme for the tree prototypes: (**a**, left) Multiple process face verification system, PC/Odroid prototype; (**b**, right) Android prototype

changes. Of course, the typical drawback of these platforms is their lower performances. However, analyzing the vast panorama of such systems very interesting solutions can be discovered. Indeed, several SBCs have recently appeared on the market, the most renowned being Raspberry, Udoo, Odroid, Lattepanda, BeegleBone; they are released at an impressive cadence in progressively more powerful versions. We decided to adopt an Odroid XU4 board to develop our prototype. It can be noted that even if most developers seem to consider Raspberry Pi 3 the best platform [5], while the Odroid XU4 currently is just ranked 5th, this ranking is related not only to system performance, but also to other aspects that we did not consider mandatory for the present project, such as the platform cost, the availability of software in the Web or the presence of communities that support software updates and forums. The most attractive feature of the Odroid XU4 platform is its processor: the Odroid XU4 adopts a Samsung Exynos5422 octa-core working at 2 GHz and presents performances highly superior to those of all other competitors. High performances in our case are fundamental in order to process the data through the DNN in real time, since this architecture is computationally very demanding. Additionally, the presence of an ARM Mali—T628 GPU may be very useful to further improve in the future the processing throughput by exploiting parallel computation, thanks to the OpenCL support. Another important aspect is the large amount of available memory, 2 GB of embedded DDR3 RAM, which allows easy storage of both the image data and the DNNs configuration parameters. Moreover, the memory can be increased up

to 64 GB in eMMC format, allowing much faster access with respect to a common SD memory. Finally, two USB 3.0 ports allow us to easily capture high-resolution video streams from two cameras, while only slower USB 2.0 ports are available for example on the Raspberry. The system currently runs at about 1 fps. We decided to use Android as the software platform for our first smartphone implementation, using the rear camera of the device. Some testing has been performed on an external USB camera too, but the smartphone solution becomes very interesting specially if used as is, without external hardware. The main advantage of smartphone-based implementations is of course their ubiquitous presence. This gives us the opportunity to exploit a very powerful and sophisticated platform, without the need of designing any hardware or any low-level software. In the preliminary implementation we are developing (Fig. 1b), for the face detection part we use the Viola-Jones (VJ) algorithm [6] already provided in OpenCV; in particular, in order to improve the speed of detection we use C code instead of Java, implemented using the Native Development Kit (NDK) provided by Google. The porting of the face recognition algorithm, in turn, has been possible thanks to the *thnets* library [7] freely available on the *github* repository; it is a stand-alone library for Torch neural networks, and relies on openBLAS and OpenMP. In order to fulfill these dependencies, and since part of the code is written in assembly language for performance reasons (and is thus strictly hardware dependent), presently we limit ourselves to Arm devices only, that anyway represent the largest portion of the smartphone market; further work will be necessary for the x86 Android version. Finally, for what concerns the voice synthesis, we use the Java interface for the embedded talk system provided by Android. The mobile phone used for testing uses an octa-core Huawei HiSilicon Kirin 655 SoC (Arm-v8a architecture): four cores run at 2.1 GHz and the remaining four at 1.7 GHz. The SoC embeds even an OpenCL-ready Arm Mali-T830 MP2 GPU, that is presently not used. In order to improve compatibility with many devices, all the native codes are compiled for a 32 bit Arm-v7 architecture.

4 Results

The accuracy of the three different verification systems discussed in Sect. 2 was tested using the same set of 1500 images, with 250 positive samples for each subject and 250 negative samples, while the fine tuning was done using roughly 2500 images both for positives and negatives. In particular, the negative sample test set is composed by 25 images each of 10 different individuals. There is no intersection between the training set and the test set negative images for a single class verification not only in terms of the samples (which is obvious) but also in terms of the individuals.

For the distance classifier and the multi-class verification, all 1500 images were tested, whereas for single-class verification 250 positive and 250 negative faces were tested. The true positive and false positive rates in each case are shown in Table 1.

It may be seen that the true positive and false alarm rates of the distance classifier and of the single-class verifier are good on this test set, while the false alarm rate of

Table 1 The left part of the table shows the percent accuracy of the distance classifier (DC) and of the multi-class verifier (MV). TA is the rate of ground-truth positive samples correctly classified as positive, FA is the rate of negative samples incorrectly classified as positive ones. The right part of the table shows the percent accuracy of the single-class verifier for classes 1…5 (the threshold of the network's output is 0.9)

	DC	MV	C1	C2	C3	C4	C5
TA(%)	93	97	94.2	92.0	89.3	89.8	94.7
FA(%)	3	30	0	0	0	0	1.6

Table 2 Processing time per frame

	Face detection	Face verification	Total
x86	0.2	0.02	0.22
Odroid	0.08	0.8	0.9
Android	0.07	0.3	0.5

the multi-class verifier is by far too large. A basic reason may be that the fine tuning of the classification layer for the latter, made with 10,000 images, is not sufficient for the detection of outliers. Another reason could be that the number of classification layer is too low. In such a case it is advisable to use the other two approaches. However, it is also noted that the distance classifier works better with the fine-tuned network as compared to the base feature extractor network.

It is left to the user to select the reliability threshold for the verification. Table 1 shows results at 0.9 threshold in a scale of 0–1. If the user receives no verification output from the system, he/she may lower the threshold for a weak match; for example, (TA, FA) for C4 in Table 1 becomes (93, 0.8) at 0.85 threshold. It may be noted that the user can set separate thresholds for the different single-class verifiers at the same time, or a single threshold for all classes in case of the distance classifier.

Some real-time experiments of the entire system were run on the different hardware versions and their average performance in terms of speed is reported in Table 2. The actual frame rates depend on the scene content. For example, the detection time for the VJ algorithm used for Android varies according to the number of faces found in a frame. This is because it uses a cascade of classifiers: if a classifier in the first layer finds something, information is passed to the other classifiers, searching for Haar features. For the Android system used in this work, face detection runs at about 25 fps with no face detected, while it drops to 6 fps with 6 faces in the scene. Similarly, the time for verification per frame increases with the number of faces to be verified.

5 Conclusions

The main indication that our results provide is that, thanks to the effectiveness of novel DNN techniques and to the ever-increasing computational power of the available hardware, we are getting closer to the realization of effective and usable devices. We have realized several different preliminary versions of our system: a Linux x86 64 program for a PC, mostly used for software development and debugging, a Linux (Arm-based) program for a single-board computer and an Android software for smartphones. The two latter solutions are real mobile implementation which will be given to the members of our Users Group in order to collect information on their actual advantages and drawbacks.

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Exploring Particle Swarm Optimization to Build a Dynamic Charging Electric Vehicle Routing Algorithm

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Abstract Electric vehicle (EV) limited range is a serious concern for its wide scale commercialization. Dynamic battery charging is being developed as a promising technology for increasing the range, vehicles are charged through inductive points placed in the net. The choice of a proper navigation route becomes essential, and algorithms must be identified for a run time identification of the better path. In this paper, we propose and explore the application of the particle swarm optimization (PSO) algorithm to solve the problem of energy efficient routing problem for inductive dynamic charging EVs. The paper presents the results obtained in a simple simulation of a road network with 11 dynamic charging inductive lanes.

Keywords Fully electrical vehicles · Dynamic wireless charging · Routing · Navigation · Particle swarm optimization

1 Introduction

Electrical vehicles exhibit a number of design challenges related to power consumption, ranging from battery technology to energy-optimized digital control [1, 2, 3]. An electric vehicle (EV) consumes a relatively small amount of power while being idle in the roads intersections, charges its battery while driving downhill and recuperates energy with regenerative braking in high traffic. These advantages from an

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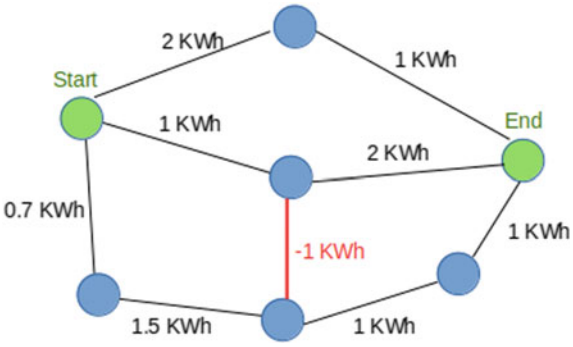

Fig. 1 Road graph for dynamic charging electric vehicle

energy efficiency point of view, however, have not been sufficient to boost the sales of EV compared to the sales of fossil fuel cars. The main reasons are the limited battery capacity, which reduces the EV driving range, the high battery costs, the scarcity of charging stations and the long recharging time. There are some solutions to reduce the recharging time like battery swapping [4], fast charging [4] and dynamic inductive charging. Dynamic inductive charging is a different, emerging technology, which consists in charging a moving EV wirelessly from a charging device buried under the road. FABRIC is an FP7 research project [5], which aims to assess the feasibility of large scale integration of dynamic charging EV. ICT will play a major role to support dynamic charging [6, 7]. Dynamic charging is powerful, as it able to extend the battery range dynamically. However, as not all the roads are expected to be equipped with coils for charging, the navigation routing algorithms have to be adapted in order to allow a vehicle to reach its destination with a sufficient battery range level. We have then to implement a shortest path algorithm with negative weight (representing the dynamic charging road Fig. 1).

The particle swarm optimization (PSO) algorithm seems suitable to be used in this case. PSO proved itself to be useful in several optimization applications (e.g., [8, 9]), and many enhancements were added to this algorithm in the last years. Efficiency of execution, also on embedded systems [8], and computational efficiency are the most important advantages of PSO. Also, just simple mathematical operators and minimal customizable parameters are needed to develop a PSO algorithm. In the end, only few lines of codes are required to write a PSO program.Given these features, this paper proposes and starts investigating the idea of applying PSO to tackle the emerging problem of EV dynamic charging.

The rest of the paper is described as follows. Section 2 presents the state of the art of EV routing. Section 3 describes the application of PSO to solve the dynamic EV routing problem. Section 4 presents the results for simulating dynamic charging EVs and dynamic charging lanes using PSO to find the energy efficient path in a

road network. We simulated the problem with the MATSIM simulator (reference). The paper then ends with a conclusion and a future work section with suggestions to enhance further the routing algorithm.

2 EV Routing State of the Art

Many works in literature. addressed the static charging EV routing problem. A routing algorithm based on the EV range, the location of charging station and origin-destination (OD) location was developed by Kobayashi et al. [10]. A recharging model to find the minimum cost path for EVs was proposed by Sweda and Klabjan [11]. Abousleiman and Rawashdeh used PSO [12] and ant colony optimization [13] to solve the energy-efficient EV routing problem. The routing algorithms were validated using real driving data from the FIAT 500e EV. The energy-efficient routing problem was approached by Artmeir et al. [14] from a graph theory angle. They extended the Bellman-Ford algorithm to propose a generic shortest path algorithm with a worst case complexity of O(n3). An A* routing algorithm with an O(n2) complexity was developed by Sachenbacher et al. [15] considering the battery capacity and the regenerative braking. The static charging EV routing problem was studied by Siddiqi et al. [16], using PSO without taking into account the regenerative braking effect. An energy efficient routing algorithm for EV was presented by Baum et al. [17] and tested on Europe and Japan road networks. The routing algorithm was based on the Customizable Route Planning (CRP) approach [18].

Only few works addressed the dynamic charging EV routing problem. Li et al. [19] used ant colony optimization routing algorithm to route a dynamic charging EV. They simulated a real world roadway network to assess the performance of the routing strategy. They simulated connected EVs and proved that the routing algorithm can reduce the total travel time, the energy consumption, the recharged volume of electricity and the corresponding cost.

In this paper, PSO is applied for the first time to solve the energy efficient routing problem for dynamic charging EV. The next section will present the particle swarm optimization algorithm that we used to solve the dynamic EV routing problem.

3 Applying PSO to Routing of Dynamic Charging EV

Particle swarm optimization is a population-based stochastic optimization technique inspired by bird flock (and fish school), as described by Kennedy and Eberhart [20]. The algorithmic flow in PSO starts with a population of particles whose positons, that represents the potential solution for the studied problem, and velocities are randomly initialized in the search space. The search for optimal position is performed

by updating the particle velocities, hence positions in each iteration/generation in a specific manner as follows. In every iteration, the fitness of each particle's position is determined by some defined fitness measure and the velocity of each particle is updated by keeping track of two "best" positions. The first one is the best position (solution) a particle has traversed so far. This value is called pBest. Another "best" value is the best position (solution) that any neighbor of a particle has traversed so far. This best value is a neighborhood best and is called nBest. When a particle takes the whole population as its neighborhood, the neighborhood best becomes the global best and is accordingly called gBest. The PSO algorithm relies on a path encoding algorithm to find the shortest path in a network. Ammar et al. [21] modified a path encoding algorithm for PSO and solved the shortest path problem. We used their work to find an energy efficient path for a dynamic charging EV. The particle fitness value is the state of charge (SoC) of the vehicle at the end of the trip (endSoC). The following pseudo code explains how to calculate the fitness value for routing a dynamic charging EV.

```
Function calculatePathFitness
endSoC = vehicle SoC at the start of the path
       for (each link in the path)
              calculate the consumed energy by the vehicle
              consumedEnergy = consumedEnergy(link)
              chargedEnergy = 0
              if the link contains a charging infrastructure
                     chargedEnergy = chargedEnergy (link)
              linkEnergyCost = consumedEnergy + chargedEnergy
              endSoC= endSoC - linkEnergyCost
              if endSoC < = 0
                     return 0
              else if endSoC > maxBatteryCapacity
                     endSoC = maxBatteryCapacity
              endIf
       endFor
return endSoC
```

The following pseudo code describes the implemented PSO algorithm for routing dynamic charging EV.

```
Initialize the particle population (priority and velocity vector
for each particle) randomly.Evaluate fitness of each particle
{
  Construct a path from particle priority vector.
  If it is a valid path
       fitness = calculatePathFitness
       Return fitness
  Else
       fitness = 0
       Return fitness
}
```

```
Calculate pBest and nBest for each particle.
Iteration_Count = 1;
Do
{
       Calculate velocity of each particle.
       Apply velocity clamping on each dimension if necessary.
       Update position of each particle.
       Evaluate fitness value of each particle.
       Update pBest for each particle if its current fitness
       value is better than pBest.
       Update nBest for each particle, i.e., choose the particle
       with the best fitness value among all the neighbors as
       the nBest for a specific neighborhood topology.
       Iteration_Count = Iteration_Count + 1;

While (Iteration_Count < Maximum_Iterations)
}
```

The next section will present the results of simulating the routing of dynamic charging EVs based on an energy-efficient PSO routing algorithm. The simulation is done using MATSIM traffic simulator.

4 Simulation

In order to verify validity of our approach, we set up a simulation environment exploiting MATSIM, an open source traffic simulator able to simulate also EVs and dynamic charging [22]. MATSIM was used to simulate 10 dynamic charging EVs with a battery capacity ranging from 11 to 20 KWh in a road network of 15 nodes and 23 links. The simulated road network is artificial. The simulation setup has been proposed to the literature state of the art [19, 22]. The motorway length is 283 km, 95 km of the road network have dynamic charging lanes (33% of the total network length). The dynamic charging lane can transfer a power of 15KW to the vehicle. The simulated dynamic charging EVs should travel a distance ranging from 50 to 160 km at a speed of 47 km/h and the trip is started with a fully charged battery. None of the simulated EVs could reach its destinations without dynamic charging. The PSO used 30 particles and 100 iterations to find the energy-efficient route. The average time for PSO to find the energy efficient route was 1.5 s. All the suggested energy-efficient paths contain roads with dynamic charging lanes and the EVs reached their destinations without running out of energy. PSO was implemented in java on a pc with a 1.7 GHz processor, Ubuntu 64 bit operating system and 4 Gb Ram.

Table 1 shows the mean (and standard deviation) state of charge (SoC) at the beginning of the trip, and the mean (and standard deviation) SoC at the end of the trip. Also values about consumed and dynamically charged energy are reported.

The present work has several limitations and is only a first step for more in depth research regarding dynamic charging EV routing. The present work does not compare the PSO algorithm against shortest path algorithm and least time path algorithm like Dijkstra and A-star. A driver will not accept to spend a lot of time to reach its

Table 1 Average energy results for the 10 simulated EVs and the standard deviation values are between brakets

Energy values	Mean value (standard deviation)
Start SoC	16 KWh (3)
Dynamically charged energy	35 KWh (9)
Consumed energy	37 KWh (10)
End SoC	14 KWh (3)

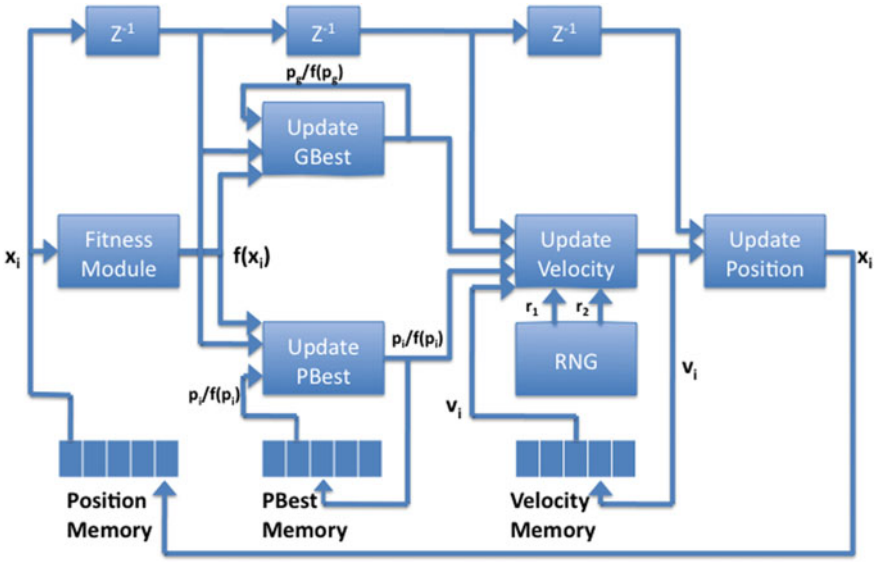

Fig. 2 Implementation of PSO on FPGA

destination so several parameters will be considered in the next steps. In this work we supposed that all drivers who travel in road with a charging lane are willing to charge their vehicles. This is not always the case since some roads may have a dedicated charging lane for drivers who want to charge their vehicles and a lane for those who don't want to charge. The willingness of the driver to charge the EV should be taking in consideration also because of its cost. The simulated road network is artificial and further research should simulate urban traffic and inter-city traffic.

5 Conclusion and Future Work

Dynamic charging is a new frontier for EVs. This new technology requires an innovation also in terms of routing algorithms. In this paper, we propose the use of the PSO algorithm, which is able to deal with negative cost links. We have presented

very preliminary results, showing that the routing algorithm is able to provide, in reasonably short time, good quality results in terms of routing, and satisfying the constraint of keeping the battery at a safe charge level.

In a future work, we will simulate more realistic traffic scenarios, considering traffic of thousands of vehicles during 24 h in a real road network. The effect of the routing algorithm on the travel time, the energy consumption, recharged volume of electricity and recharged electricity costs will be addressed. A performance comparison should also be performed with other algorithms, such as ant colony. We intend also to implement the PSO on an FPGA circuit [23] and use it with a GPS device (Fig. 2).

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A Thermoelectric Powered System for Skiing Performance Monitoring

Matteo Nardello, Pietro Tosato, Maurizio Rossi and Davide Brunelli

Abstract Pervasive and wearable devices are becoming more and more common and important in the growing market of Internet of Things. Still the implementations of these devices are often not energy aware, lacking in optimization and ignoring the possibility of energy harvesting. Here we present a novel prototype of wearable device, conceived for skiing monitoring, that exploits the potential of thermoelectric harvesting in a mountain climate environment.

Keywords Energy harvesting · Thermoelectric energy · Autonomous embedded system · Bluetooth low-energy · Internet-of-things

1 Introduction

The world of wearable applications received in the last years many attentions by research groups, belonging to different disciplines (e.g. biomedical, electronics [1] and health care [2]) because it is challenging designing with constrained resources. The business of wearables is expected to grow exponentially in the future [3], in conjunction with IoT revolution, thanks to the availability of low-power electronic microcontroller. At the moment, the complexity of these objects does not meet the requirements of energy neutrality, due to the lack of self-sustainable electronics. Despite that, some implementations that integrate energy harvesting solutions

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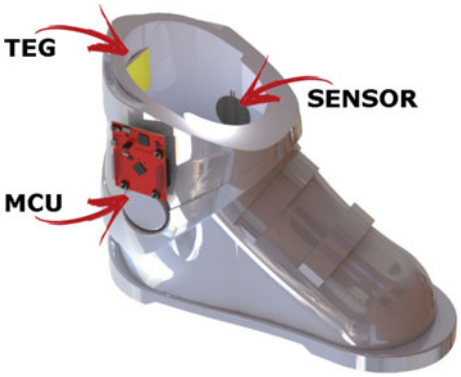

Fig. 1 Render of the prototype with real size components. A real prototype will be realized in future work

to extend battery lifetime or even try to become energy neutral can be found in literature [4], even with some predictors for energy intake [5]. For instance, [6] matched the power provided by human heat (thanks to thermoelectric generators) to ultra-low-power electronics in a smart wrist band. Many other contributions that exploit thermoelectric generators (TEG) can be found, proving the interest to integrate TEGs in wearables [7].

In this paper, we introduce the design of a smart device for monitoring skiing activities, directly embedded in the boots, able to provide information about the intensity of the forces on the boot along curves. To meet low-power consumption constraints, piezoelectric sensors are used for force sensing. Moreover, the device integrates a thermoelectric generator that greatly improves battery life by exploiting the temperature gradient between the inner of the boot and the cold mountain environment (Fig. 1). The rest of the paper is organized as follows: Sect. 2 presents the system design and the description and characterization of all the components. Result discussion is provided in Sect. 3. Finally, Sect. 4 concludes the work.

2 Implementation

The system consists of three functional blocks, as depicted in Fig. 2. The first part deals with the power management of the system, and includes the thermoelectric generator connected to the Energy Harvester circuit, based on a LTC3108 ultra-low voltage step-up converter from Linear Technologies [8]. For storing energy, a supercapacitor bank is used. The second part consist of the platform used to develop the application, a CC2650 ARM Cortex-M3 + Bluetooth Low Energy transceiver from Texas Instruments [9] along with two piezoelectric sensors, used for detecting the movement of the skier. Last block is the Android application, in charge of receiving and showing data coming from the system.

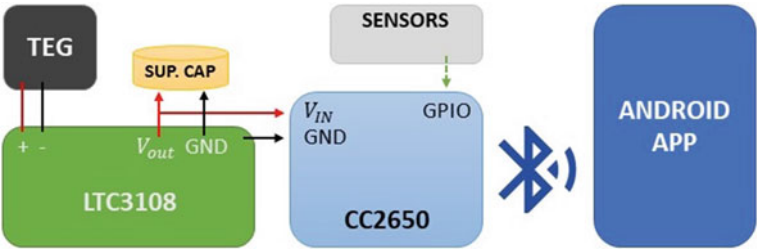

Fig. 2 Block scheme of the proposed solution

2.1 Thermoelectric Generators and Energy Harvesting

A Thermoelectric generator (TEG) is a special device, made of several pairs of P/N junctions, that generates electricity from heat flows thanks to the Seebeck effect, as shown in Fig. 3. The P/N pairs are connected electrically in series, but thermally in parallel, providing electrical current at a suitable output voltage that is then shifted to an adequate voltage level. The power generated is used to power electronics or to charge energy reservoirs by the energy harvesting circuit. The TEG module has been chosen among many ones tested. It is a TEC1-12706, a 4×4 cm squared cell TEG, extensively characterized as following. The test bench for the characterization of the TEG modules is built around a heated plate maintained at constant temperature with an ad-hoc PID controller to set a constant temperature difference between the two side of the TEG placed on the plate, eventually using air ventilation and heatsink; to complete the setup a precision resistor of 1 ohm is used to measure current output of the TEG, while the load is tuned using variable resistors. The aim of such setup is to primarily quantify the energy provided by a TEG in a typical skiing scenario and also identify the maximum output power in function of the impedance of the upcoming harvesting circuitry. The electrical circuit of the measurement system, used for the characterization, is shown in Fig. 4.

Figure 5 shows the output power at different loads, with a temperature gradient of 15 °C, which emulates an average working condition (i.e. temperature gradient between the inner of a ski boot with respect to the ambient temperature), as described in [10]. Once evaluated the maximum power point, additional energetic characterization of the TEG was performed. For simulating the worst operating scenario, according to the literature [10], a test with a temperature gradient of 10 °C was used. A time interval of 20 min is considered, according to the time needed to complete a downhill skiing. A typical long term experiment is presented in Fig. 6, that shows the power generated over time by the TEG. The average power generated is 8.6 mW.

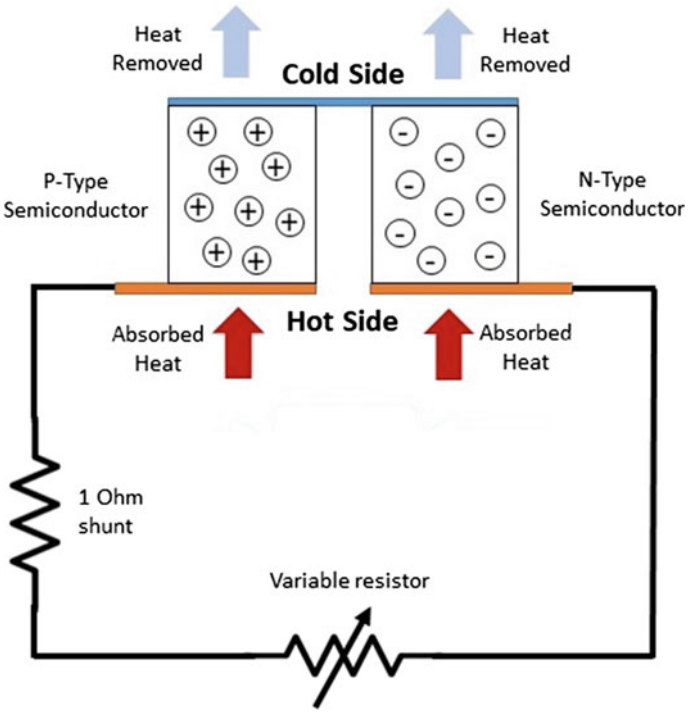

Fig. 3 Working principle of a thermoelectric generator and load setup

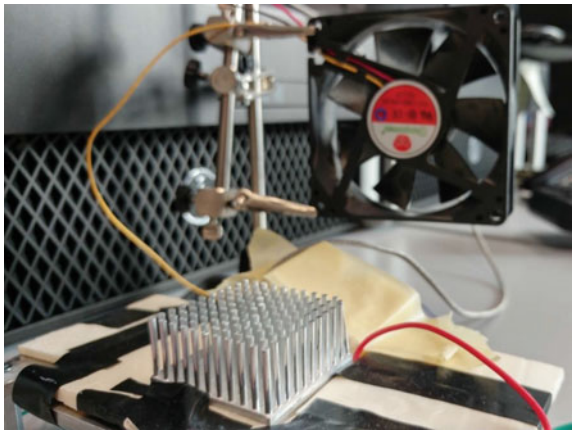

Fig. 4 Cooling system used to provide the right thermal gradient at the TEG surfaces

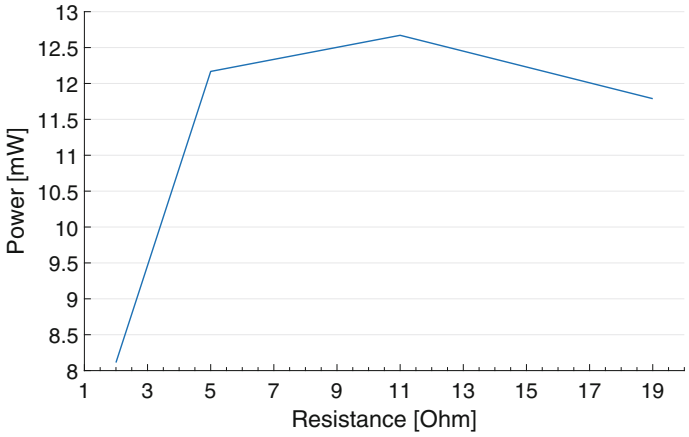

Fig. 5 Power characterization at different load conditions

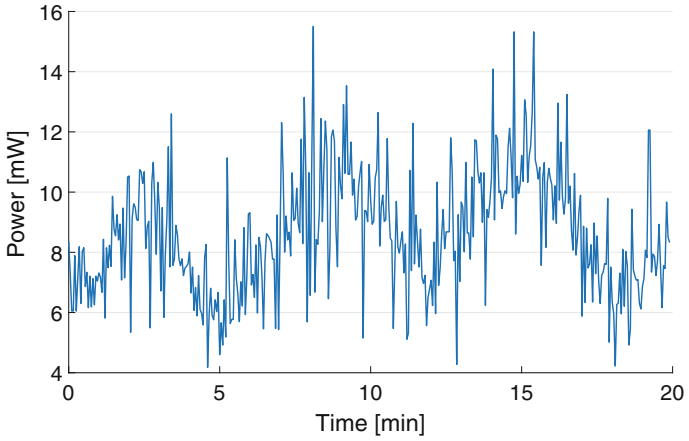

Fig. 6 Output power with 10 °C temperature gradient

2.2 CC2650 Application

For a faster prototyping, a LaunchPad™ [9] CC2650 by Texas Instruments was used. The CC2650 combines a 2.4 GHz RF transceiver, 128 KB flash memory, 20 KB of SRAM and a full range of peripherals. The device features an ARM Cortex-M3 series processor that handles the application layer while Bluetooth low-energy protocol stack is autonomously managed by a dedicated ARM Cortex-M0 processor. All the software implemented works on a real-time operating system.

Sensors Implementation. To monitor skiing performance and the way to tackle turns, two piezo-resistive sensors have been placed on each side of the boot, for measuring the pressure generated by the skier on each side. The CC2650 features a 12-bits ADC that is used to acquire data from the sensors with a fixed sampling rate. Moreover, the operations are managed by the dedicated Sensor Controller Engine inside the CC2650, which allows to keep the MCU in low-power mode thus saving power.

Bluetooth Data Transmission. Bluetooth service running on TI-RTOS is configured in read mode. The data sent consists of arrays containing the history of the sensors output with the corresponding timestamps. The board is configured to send data through BLE only on request by the user. In this way, the board does not have to keep the connection alive thus decreasing the power consumption.

2.3 Android Application

For showing the data collected by the device, an Android application was developed. The main purposes are: (1) Establish a BLE connection with the microcontroller; (2) Request the data when needed; (3) Receive, parse and plot the data coming from the CC2560. When the user flushes the information from the CC2650, all the received data are plotted ordered in a timeline. Figure 7 shows an example of the graph created by the android application, whereas positive points represents a pressure on the left sensor (i.e. the skier has turned left) while negative points a pressure on the right sensor, meaning the skier has turned right (Fig. 1).

3 Discussion and Results

Experimental characterization has been done in terms of power consumption and autonomy.

Power consumption considerations. As previously mentioned, the system operates using the energy harvested from the TEG and stored in the super-capacitor (SC). The choice of the SC capacitance is obtained by the energy balance $E = C * (V_i^2 - V_f^2)/2$, where C is the capacitance of the SC (unknown), V_i and V_f are the initial and final working voltages (3.2 and 2.7) and E is the energy used by the board during skiing activity. In our setup, 3F was used with a 2-series capacitor bank.

To address the power consumption needed by the board for collecting data from sensors and sending them via Bluetooth, a 20 min test has been setup and both idle and working power consumption has been collected. The average power consumption values for the two operating modes are summarized in Table 1. As expected, the most energy hungry activity is the BLE transmission, however it lasts only for 0.3 s after the user button is pressed, so the average power consumption of the microcontroller is

about less than 1 mW. Thus, the board power consumption is adequately compensated by a single TEG.

Typical application scenario. To test the energy performance of the system, the voltage charge of the SC is monitored in working conditions (data acquisition and BLE transmission), with a temperature difference of 10 °C (worst condition) for a duration of 20 min (typical time needed to ski down a slope and to climb up with a lift). Results of the test are summarized in Fig. 8. As can be noted from 0 to 6 min there is a negative slope, indicating that the capacitor is discharging. This is caused by the fact that the characteristic curve of a discharging super-capacitor has the highest discharge rate at the beginning, so the power supply from the TEG is not enough to balance the losses. However, this initial discharge is only of about 0.1 V. After this settling time, the TEG is capable of balance the super-capacitor discharge and the system reaches the energetic autonomy. The super-capacitor voltage remains constant at a value of about 3 V. This means that the TEG is enough to provide the required power to the board at least for an entire day assuming that the TEG is working with

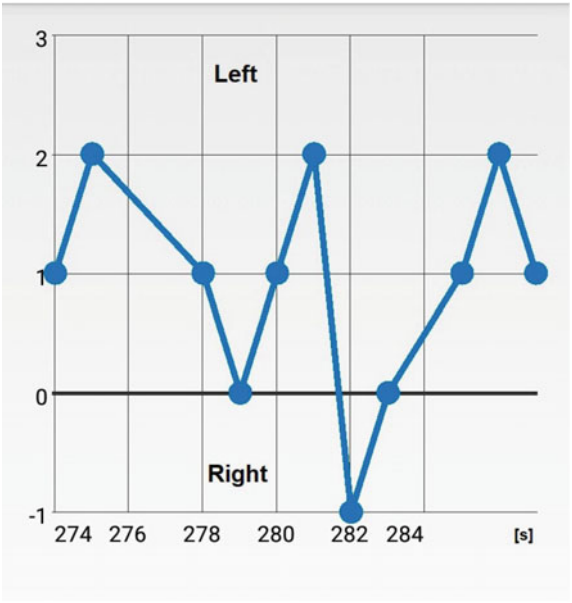

Fig. 7 Application screenshot

Table 1 Power consumptions measured on the prototype

Mode	Power consumption [mW]
Sensing	0.9
BLE TX	3.1
Average	1.0

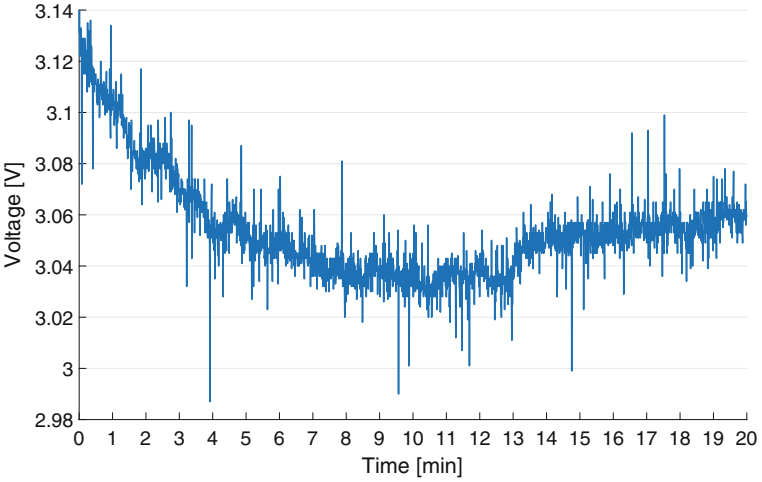

Fig. 8 Super-capacitor voltage trend of the complete system

a minimum temperature gradient of 10 °C.

Cold start and autonomy. We have evaluated the ability of the TEG to fully charge the super-capacitor, starting from 0 V (cold start). The duration of the test, as shown in Fig. 9 was about 11 h, with a fixed temperature gradient of 10 °C, to simulate the worst-case scenario. As can be noted the charging curve shows a linear trend, with a charge rate of 0.25 V/h. In the case the TEG does not produce energy the super-capacitor energy buffer can still provide quite long autonomy. Results show that the system can operate for about 3 h before shutting down, verified by the discharge curve in Fig. 10. This is enough to cover half day of skiing.

4 Conclusion

A complete embedded device for skiing monitoring was developed and implemented, thanks to an hardware-simulated evaluation of the energy offered by a TEG in the mountains climate conditions. Energy harvesting design enhances the monitoring system with good autonomy and enables to use BLE connections to the user smartphone.

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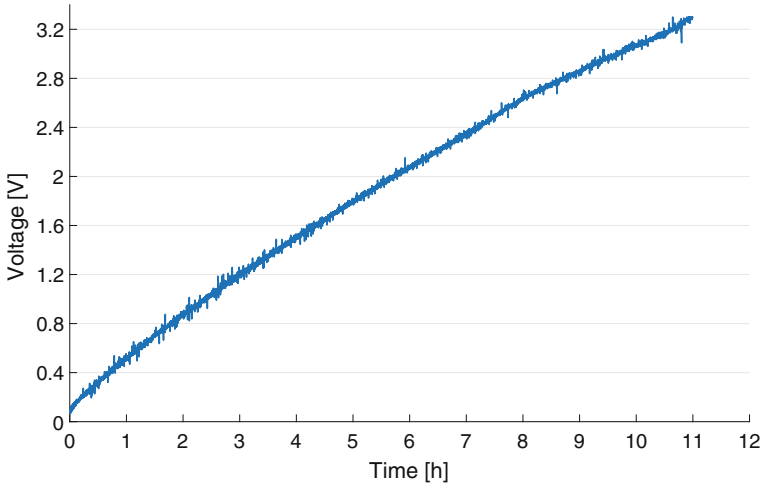

Fig. 9 Super-capacitor charge with the TEG

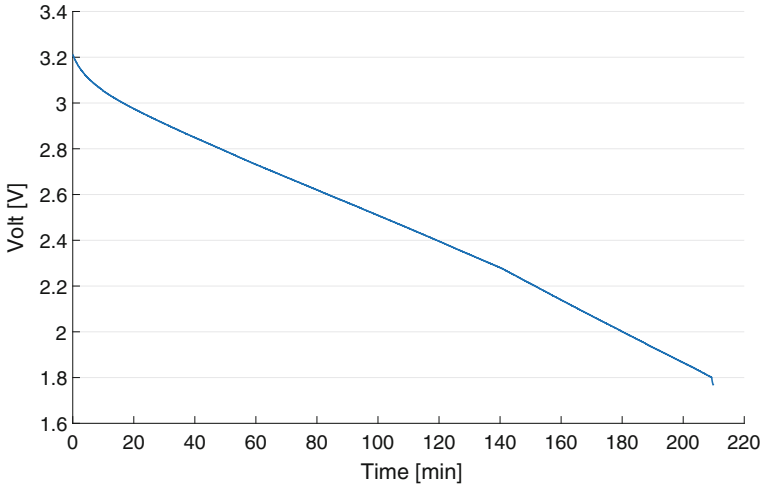

Fig. 10 Autonomy of the system without the TEG and with the super-capacitor fully charged

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