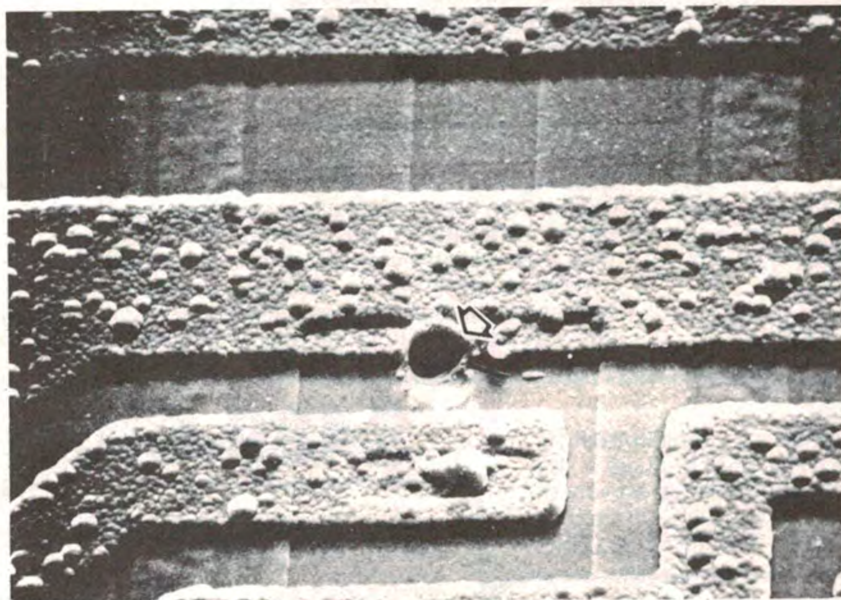
Electrostatic discharge — nemesis of electronic systems

D.E. Frank

Electrostatic hazards to electronic equipment are known to be present at manufacturing facilities during the assembly and testing of electronic systems as well as during shipment and handling at the user's facilities. In order to protect these systems, it is necessary to understand the nature of electrostatic discharge (ESD), how it is generated, and how it is transmitted to electrostatic discharge sensitive (ESDS) components. Additionally, it is necessary to understand which parts are ESDS, how they are damaged, and the subsequent effect on the respective system.



Close up view (x1000) of electrostatic damage in an op-amp. (See the series of pictures on pages 16-17).

What is ESD?

OUR MOST common conception of electrostatic discharge is the miniature lightning bolt or shock we receive in periods of low humidity when we walk across a carpet or slide across vinyl seatcovers and then discharge to a door knob or door handle. In essence, however, most static electricity is subliminal or occurs at values well below our perception level of 1500 to 2000 volts.

Static electricity is generated whenever two substances are rubbed together, separated, or flow relative to one another (such as a gas or liquid over a solid). This static electricity (electrical charge at rest) is stored on non-conductive materials and tends to remain in the localised area of contact awaiting the opportunity to discharge to the first available ground source. In the case of conductive materials, the charge is rapidly distributed over the entire surface and the surface of other conductors which come in contact.

The Triboelectric Series (Table 1) shows the charge relationships of many materials. Note that cotton is identified as a reference material, being at mid-point of Table 1. It tends to absorb moisture, thereby rendering it somewhat conductive. However, when cotton is rubbed against another material, it has the ability to produce a static charge.

Materials listed above cotton tend to assume a positive charge by giving off electrons in a friction separation situation, while those listed below cotton become negatively charged by acquiring electrons. When any two materials experience separation or rubbing, the material listed highest on the table will become positively charged, and the material listed lower will accept the negative charge.

For the sake of simplicity, let us define the cause of common static as the flow of materials and people within an environment. Materials include all components, packaging, and other raw materials which make up our finished product. People carry and generate charges, and it all takes place within a defined environment made up of facilities and equipment. The environment is not limited to a plant, but can be defined as a package, or many plants as in a transport situation.

Static, as it manifests itself in our environment, is actually a symptom. If we can impose control on the elements which create static as an end result, we can control the generation of a myriad of problems caused by static.

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It is the author's intent to present an understanding of ESD, to explain how various materials and situations generate ESD, and to discuss ESD sensitive devices in depth. In the discussion of ESD sensitive devices, an effort has been made to present a thorough "physics of failure" analysis to provide insight into the design and structure of ESD sensitive devices as well as the failure modes and effects. Those individuals not desiring an in-depth technical treatise may review Tables 2 and 3, and also the discussion in paragraphs entitled "Detecting ESD Damage" and "Protecting Your Equipment".

Means of Static Generation	Electrostatic Voltages 10 to 20% Relative Humidity	65 to 90% Relative Humidity
Walking across carpet	35 000	1 500
Walking over vinyl floor	12 000	250
Worker at bench	6 000	100
Vinyl envelopes for work instructions	7 000	600
Common poly bag picked up from bench	20 000	1 200
Work chair padded with polyurethane foam	18 000	1 500

Ref. U.S. Department of Defense DOD-HDBK-263 (tables III and IV) 2 May, 1980.

Table 2. Typical electrostatic voltages

ESDS devices

Typical ESD voltages are shown in Table 2, and the ranges of susceptibility of ESDS devices are shown in Table 3. Parts of devices can be destroyed (hard failures) or simply degraded or made intermittent (soft or upset failures) due to exposure to electrostatic discharge. Parts are susceptible to damage when an ESD occurs across their terminals. ESDS parts can be destroyed by an ESD where one pin is connected to a high voltage source and other pins are ungrounded. In other words, a hard ground connection is not required to destroy an ESDS part.

MOS large scale integration devices in hermetic packages with non-conductive lids could be damaged by spraying the lids with canned coolant, despite there being no ground path connected to the part.

MATERIALS	
AIR	
HUMAN HANDS	
ASBESTOS	↑ Increasingly Positive
RABBIT FUR	
GLASS	
MICA	
HUMAN HAIR	
NYLON	
WOOL	
FUR	
LEAD	
SILK	
ALUMINUM	
PAPER	
COTTON	
STEEL	
WOOD	
AMBER	
SEALING WAX	
HARD RUBBER	
NICKEL COPPER	
BRASS SILVER	
GOLD PLATINUM	
SULFUR	Increasingly Negative ↓
ACETATE RAYON	
POLYESTER	
CELLULOID	
ORLON	
SARAN	
POLYURETHANE	
POLYETHYLENE	
POLYPROPYLENE	
PVC (vinyl)	
KEL-F (CTFE)	
SILICON	
TEFLON	

Table 1. Triboelectric series

ESDS parts installed in assemblies normally have their leads connected to a sufficient mass of conductive material, such as printed circuit board (pcb) runs and wiring, which may provide the required ground to result in damage from an ESD. In such cases, however, the voltages required are normally higher than those needed when one or more pins or the part case is grounded.

Assemblies and equipment containing ESDS parts are often as sensitive as the most sensitive ESDS part which they contain. Incorporation of protective circuitry in these assemblies and equipment can provide varying degrees of protection from ESD applied to their terminals. Such assemblies and equipment, however, can still be vulnerable from induced ESD caused by strong electrostatic fields or by contact of pcb electrical connections or paths with a charged object.

Intermittent or upset failures can occur on certain types of parts, such as LSI memories and chips, either prior to or after lidding and sealing. Such failures can also occur when equipment is in operation, characterised by a loss of information or temporary distortion of its functions. No apparent hardware damage occurs and proper operation resumes automatically after the ESD exposure or, in the case of some digital equipment, after re-entry of the information by resequencing the equipment.

Upset can also be the result of an ESD spark in the vicinity of the equipment. The electromagnetic pulse generated by the spark causes erroneous signals to be picked up by the equipment circuitry. Upset can also occur by the capacitive or inductive coupling of an ESD pulse or by the direct discharge of an ESD through a signal path providing an erroneous signal.

While upset failures occur when the equipment is operating, catastrophic failures can occur any time. Catastrophic ESD failures can be the result of electrical overstress of electronic parts caused by an ESD, such as: a discharge from a person or object, an electrostatic field, or a high voltage spark discharge (see Figure 1).

Some catastrophic failures may not occur until some time after exposure to an ESD, as in the case of marginally damaged ESDS parts, which require operating stress and time to cause further degradation and ultimate catastrophic failure. Only certain part types seem to be susceptible to this latent failure process.

There are some types of catastrophic ESD failures which could be mistaken for upset failures. For example, an ESD could result in aluminium shorting through a SiO_2 dielectric layer. Subsequent high currents flowing through the short, however, could vaporise the aluminium and open the short. This failure may be confused with upset failure if it occurs during equipment operation, but the damage due to the ESD would cause a latent defect that will probably reduce the operating life of the part.

Parts that are very susceptible to ESD upset are any within logic families that require small energies to switch states or small changes of voltage in high impedance lines. Examples of families that are sensitive would be NMOS, PMOS, CMOS, and low power TTL. Linear circuits with high impedance and high gain inputs would also be highly susceptible, along with RF amplifiers and other RF parts at the equipment level; however, design for RFI immunity can protect these parts from damage due to ESD high voltage spark discharge.

To protect parts sensitive to ESD high spark discharge at the equipment level requires: good radio frequency interference (RFI)/electromagnetic compatibility (EMC) design, buffering of busses, proper termination of busses, shielding of buss conductors, and the avoidance of penetrations of the equipment enclosure that lead to sensitive parts. ▶

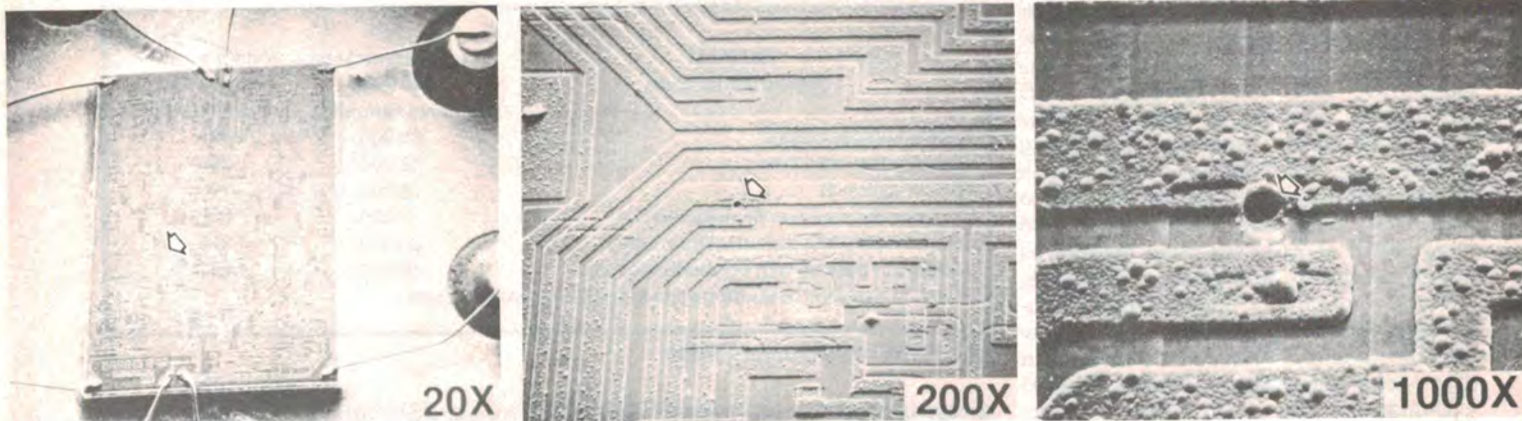


Figure 1. **Static discharge damage in an op-amp integrated circuit (arrows show location of damage).**

Failure mechanisms

Typical ESD failure mechanisms are divided into the two following categories. Those in the first category, thermal secondary breakdown, metallisation melt and bulk breakdown, are power dependent. Those in the second category, dielectric breakdown, gaseous arc discharge, and surface breakdown, are all voltage dependent. All of the above are applicable to microelectronic and semiconductor devices. Metallisation melt and gaseous arc discharge are evident in film resistors, and bulk breakdown is typical of piezoelectric crystals.

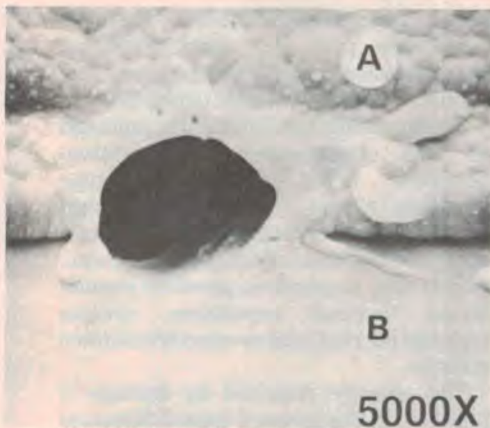
Besides these catastrophic failure mechanisms, un-encapsulated chips and LSI MOS integrated circuits have exhibited temporary failure due to gaseous arc discharge from positive charges deposited on the chip as a by-product of gaseous arc discharges within the package between the lid and the substrate.

Thermal secondary breakdown is also known as avalanche degradation. Since thermal time constraints of semiconductor materials are generally large compared with transient times associated with ESD pulse, there is little diffusion of heat from the areas of power dissipation, and large temperature gradients can form in the parts. Localised junction temperatures can approach material melt temperatures, usually resulting in development of hot spots and subsequent junction shorts due to melting.

For junction melting to occur in bipolar (P-N) junctions, sufficient power must be dissipated in the junction. In the reverse bias condition, most of the applied power is absorbed in the immediate junction area with minimal power loss in the body of the part. In the forward bias condition, the junction in-

CLASS 1: SENSITIVITY RANGE 0 TO <1000 VOLTS
Metal Oxide Semiconductor (MOS) devices including C (Complementary), D (Double-Diffused), N (N-Channel), P (P-Channel), V (V-Groove) and other MOS technology without protective circuitry, or protective circuitry having Class 1 sensitivity
Surface Acoustic Wave (SAW) devices
Operational Amplifiers (OP AMP) with unprotected MOS capacitors
Junction Field Effect Transistors (JFETs) (Ref.: Similarity to MIL-STD-701: Junction field effect, transistors and junction field effect transistors, dual unitized)
Silicon Controlled Rectifiers (SCRs) with I_o <0.175 amperes at 100° Celsius (°C) ambient temperature (Ref.: Similarity to MIL-STD-701: Thyristors [silicon controlled rectifiers])
Precision Voltage Regulator Microcircuits: Line or Load Voltage Regulation <0.5 percent
Microwave and Ultra-High Frequency Semiconductors and Microcircuits: Frequency >1 gigahertz
Thin Film Resistors (Type RN) with tolerance of <0.1 percent; power >0.05 watt
Thin Film Resistors (Type RN) with tolerance of >0.1 percent; power ≤0.05 watt
Large Scale Integrated (LSI) Microcircuits including microprocessors and memories without protective circuitry, or protective circuitry having Class 1 sensitivity (Note: LSI devices usually have two to three layers of circuitry with metallization crossovers and small geometry active elements.)
Hybrids utilizing Class 1 parts
CLASS 2: SENSITIVITY RANGE >1000 TO ≤4000 VOLTS
MOS devices or devices containing MOS constituents including C, D, N, P, V, or other MOS technology with protective circuitry having Class 2 sensitivity
Schottky diodes (Ref.: Similarity to MIL-STD-701: Silicon switching diodes [listed in order of increasing trr])
Precision Resistor Networks (Type R2)
High Speed Emitter Coupled Logic (ECL) Microcircuits with propagation delay ≤1 nanosecond
Transistor-Transistor Logic (TTL) Microcircuits (Schottky, low power, high speed, and standard)
OP AMPs with MOS capacitors with protective circuitry having Class 2 sensitivity
LSI with input protection having Class 2 sensitivity
Hybrids utilizing Class 2 parts
CLASS 3: SENSITIVITY RANGE >4000 TO ≤15,000 VOLTS
Lower Power Chopper Resistors (Ref.: Similarity to MIL-STD-701: Silicon Low Power Chopper Transistors)
Resistor Chips
Small Signal Diodes with power ≤1 watt excluding Zeners (Ref: Similarity to MIL-STD-701: Silicon Switching Diodes [listed in order of increasing trr])
General Purpose Silicon Rectifier Diodes and Fast Recovery Diodes (Ref: Similarity to MIL-STD-701: Silicon Axial Lead Power Rectifiers, Silicon Power Diodes [listed in order of maximum DC output current], Fast Recovery Diodes [listed in order of trr])
Low Power Silicon Transistors with power ≤5 watts at 25°C (Ref: Similarity to MIL-STD-701: Silicon Switching Diodes [listed in order of increasing trr], Thyristors [bi-directional triodes], Silicon PNP Low-Power Transistors [Pc ≤5 watts @T_A = 25°C], Silicon RF Transistors)
All other Microcircuits not included in Class 1 or Class 2
Piezoelectric Crystals
Hybrids utilizing Class 3 parts

Table 3. List of ESDS devices by part type



Detailed view of the 6-micron (0.0002") diameter hole created in aluminium metallisation (A) and silicon dioxide substrate (B) by static discharge.

hibits lower resistance. Even though a greater current flows, a greater percentage of the power is dissipated in the body of the part. Thus, more power is generally required for junction failure in the forward bias condition.

For most transistors, the emitter-base junction degrades with lower current values than the collector-base junction. This is because the emitter-base junction normally has smaller dimensions than any of the other junctions in the circuit. For reversed polarity signals, only a very small microampere current flows until the voltage exceeds the breakdown voltage of the junction. At breakdown, the current increases and results in junction heating, due to the nucleation of hot spots and current concentrations. At the point of second breakdown, the current increases rapidly due to a decrease in resistivity and a melt channel forms that destroys the junction. This junction failure mode is a power-dependent process.

Metallisation melt failures can occur when ESD transients increase part temperature sufficiently to melt metal or fuse-bond wires. Theoretical models exist which allow computation of currents that can cause failure for various materials as a function of area and current duration. Such models are based on the assumption of uniform area of the interconnection material. In practice, it is difficult to maintain a uniform area, and the resultant non-uniform area can result in localised current crowding and subsequent hot spots in the metallisation. This type of failure could occur where the metal strips have reduced cross-sections as they cross oxide steps. Normally due to shunting of the currents by the junction, this failure requires a larger power level at higher frequencies than is required for junction damage at lower frequencies. Below 200 to 500 MHz, the junction capacitance still presents a high impedance to currents, thereby shunting them around the junction.

Bulk breakdown results from changes in junction parameters due to high local temperatures within the junction area. Such high temperatures result in metallisation alloying or impurity diffusion, resulting in drastic changes in junction parameters. The usual result is the formation of a resistance path across the junction. This effect is usually preceded by thermal secondary breakdown.

Dielectric breakdown occurs when a potential difference is applied across a dielectric region in excess of the region's inherent breakdown characteristics, and a puncture of the dielectric occurs. This form of failure is due to voltage rather than power and could result in either total or limited degradation of the part, depending on the pulse energy. For example, the part may heal from a voltage puncture if the energy in the pulse is insufficient to cause fusing of the electrode material in the puncture. It will, however, usually exhibit lower breakdown voltage or increased leakage current after such an event, but it will not exhibit catastrophic part failure.

This type of failure could result in a latent defect resulting in catastrophic failure with continued use. The breakdown voltage of an insulating layer is a function of the pulse rise time, since time is required for avalanching of the insulating material.

Gaseous arc discharge occurs in parts with closely spaced, unpassivated, thin electrodes. Gaseous arc discharge can cause degraded performance. The arc discharge condition causes vaporisation and metal movement, which is generally away from the space between the electrodes. The melting and fusing do not move the thin metal into the interelectrode regions. In melting and fusing, the metal flows together and flows or opens along the electrode lines. There can be fine metal globules in the gap region, but not in sufficient numbers to cause bridging. Shorting is not considered a major problem with passivated thin metal electrodes.

On a SAW band pass filter device with thin metal of approximately 0.4 micron and 3.0 microns (1 micron = 1×10^{-6} metres) electrode spacing, operational degradation was experienced from ESD. When employing thicker metallisation such as 1.35 microns, this gaseous arc discharge in an arc gap at typically 50 microns can be used for protection to dissipate incoming high voltage spikes.

For LSI and memory ICs with passivation/active junction interfaces susceptible to inversion, gaseous arc discharge from inside the package can cause positive ions to be deposited on the chip and cause failure from surface inversion. This has been reported to occur especially on parts with nonconducting lids. A special case of this is UV-EPROMs with quartz lids, where failures can be annealed by neutralising the positive charge with ultraviolet light through the quartz lid.

Surface breakdown occurs at perpendicular junctions, and is explained as a localised avalanche multiplication process caused by narrowing of the junction space charge layer at the surface. Since surface breakdown depends on numerous variables, such as geometry, doping level, lattice discontinuities, and unclean gradients, the transient power which can be dissipated during surface breakdown is generally unpredictable.

The destruction mechanism of surface breakdown results in a high leakage path around the junction, thus nullifying the junction action. This effect, as well as most voltage sensitive effects like dielectric breakdown, is dependent upon the rise time of the pulse and usually occurs when the voltage threshold for surface breakdown is exceeded before thermal failure can occur.

Another mode of surface failure is the occurrence of an arc around the insulating material. This failure is similar to metallisation gaseous discharge except that discharge is between metallisation and semiconductor.

Specific effects on circuits

Now, having identified the causes of ESD and the major types of failure mechanisms, it is important to assess how these failures manifest themselves in systems. Typical devices and their degradation thresholds are summarised in Table 4. A more detailed analysis of the physical mechanisms follows.

MOS structures are a conductor and semiconductor substrate separated by a thin dielectric. This family includes MOS field effect transistors (FETs), MOS ICs, bipolar, hybrid, linear and digital ICs and MOS capacitors. Or more basically, the family includes any dual dielectric system or semiconductor with metallisation crossovers. The newer devices in this area — the VMOS (vertical groove MOS), the HMOS (high density MOS), the HEX MOS, and some of the prototype GaAs MESFETS (gallium arsenide metal semiconductor field effect transistor) — approach 1 micron or less compared with today's chip geometries of 4 to 5 microns (see Figure 2). Needless to say, as these ▶

DEVICE	TEST RESULTS	
	THRESHOLD,[1] VOLTS	DEGRADATION CRITERIA[2]
Diodes		50% drop in V_R at I_R = 5 μA
1N459	> 3000	
1N916	3000	
T1551	450	
1N4151	> 3000	
Zener Diodes		50% drop in V_R at I_R = 5 μA
LVA356	> 3000	
Transistors		50% drop in $V_{(BR)CBO}$ at I_R = 5 μA
2N2222	1000	
2N2369A	460	
2N2432A	620	
2N2540	1450	
2N2907	1200	
2N3117	1000	
2N3570	380	
2N4251	460	
2N4872	1200	
2N5154	> 3000	
Junction Field-Effect Transistors		50% drop in $V_{(BR)GSS}$ at I_G = 5 μA
2N2608	320	
2N3112	530	
2N3971	160	
2N4118A	140	
Metal-Oxide Semiconductor Transistors		I_G>5 μA at V_{GS} = 22 V
GI MEM 520c (chip)	58	
Complementary Metal-Oxide Semiconductor Integrated Circuits		> 0.5 μA input at 10 V or > 10% decrease in output voltage across 100-KΩ load
RCA CD4001	250	
Silicon-Controlled Rectifiers		50% increase in I_{CGO}
2N886A	680	
2N3030	1000	

NOTES:
1. Reverse-breakdown polarity.
2. Where V_R is the reverse voltage, I_R the reverse current, $V_{(BR)CBO}$ the collector/base breakdown voltage, I_B the base current, $V_{(BR)GSS}$ the gate/source breakdown, I_G the gate current, V_{GS} the gate/source voltage, and I_{CGO} the gate leakage current.

Table 4. Typical device degradation threshold

smaller geometries blend with higher purity processing, the device susceptibilities will rise and ESD transients of 20 volts will become lethal.

Differences in susceptibilities of these MOS technologies are dependent upon the gate dielectric strength and the oxide thickness. In the past, gate dielectric thickness has typically been around 0.11 micron with dielectric strengths ranging around 1×10^6 to 1×10^7 V/cm, with breakdown between 80 and 120 volts. Researchers today, however, are creating functional devices with dielectric thicknesses in the 0.06 to 0.08 micron range and breakdowns at 20 and 25 volts.

Many monolithic ICs have metallisation runs which cross over active semiconductor regions with field oxide between them serving as the insulator. These are called parasitic MOS transistors. Normally, these break down around 100 volts due to field intensification at the corners of the metallisation and weak dielectric strength of the oxide barrier. Breakdown of the oxide insulator is permanent, as opposed to breakdown of a semiconductor, which is reversible.

If very short-term overvoltages occur, a subsequent breakdown or avalanche occurs at a lower value than normal. As the punch-through short occurs, the metallisation will flow through the dielectric to create a low resistance short. However, in some instances where there is a particularly thin metallisation, such as 0.4 micron, or there is sufficient energy passed through the short, the metal will be vaporised and the short will clear but leave a cratered hole in the dielectric. Degraded performance may result but not a catastrophic failure. There is conjecture that the short in some circumstances might reappear or performance might continue to degrade.

Semiconductor junctions included in this classification are positive-negative (PN) junctions, P-type intrinsic N-type (PIN) junctions, and Schottky barrier junctions. Their sensitivity to ESD depends on geometry, size, resistivity, impurities, junction capacitance, thermal impedance, reverse leakage current and reverse breakdown voltage.

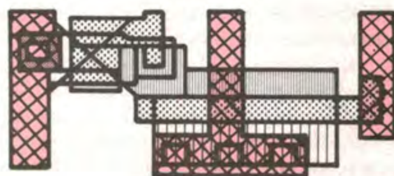
The energy required to damage a junction in the forward biased direction is generally ten times that required in the reverse biased direction. Emitter-base junctions in bipolar transistors, whether integrated circuit or a discrete transistor, are usually more susceptible to ESD damage than collector-base or collector-emitter junctions. This is primarily due to size and geometry, where the emitter-side wall experiences large energy-densities during reverse biased ESD. Because of larger areas, the collector-base and collector-emitter do not experience the same energy densities, although with the collector-base and collector-emitter it is possible to laterally forward bias the base-emitter. In this case, a current crowding at the emitter side will occur.

Junction field-effect transistors which have high impedance gates are particularly sensitive to ESD. They have extremely low gate-to-drain and gate-to-source leakage in the order of less than 1 nanoampere, and relatively high breakdown voltage of greater than 50 volts. Therefore, the gate-to-drain and gate-to-source are usually the most sensitive ESD paths. Figure 3 is a

TYPICAL CELL GEOMETRIES

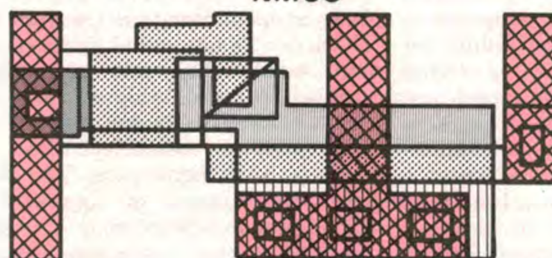
MC68000 Series

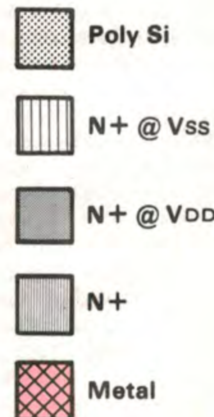
HMOS



MC6800 Series

NMOS





HMOS ADVANTAGES

Circuit densities twice standard NMOS

NMOS = 4128μ^2 Per Cell

HMOS = 1852.5μ^2 Per cell

Speed-power product four times better than standard NMOS

NMOS ≅ 4 PICOJOULES

HMOS ≅ 1 PICOJOULE

Figure 2. **Comparison of HMOS and NMOS technologies.**

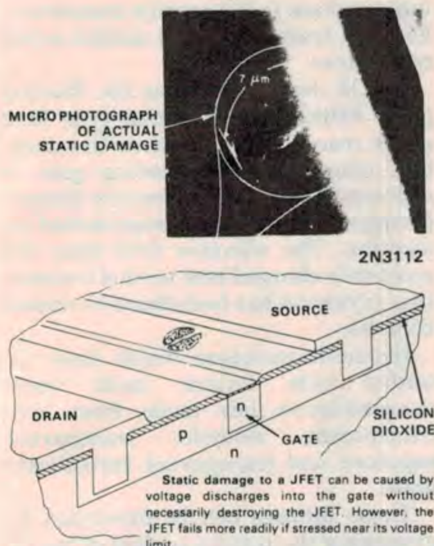


Figure 3. **Example of nondestructive ESD damage to a JFET device.**

classic example of non-destructive ESD damage to a JFET device. The device shown continued to function normally in the circuit. However, it experienced a dramatic decrease in its reverse breakdown voltage.

Schottky barrier junctions, such as the 1N57111 diode and TTL Schottky integrated circuits, are particularly sensitive to ESD because they have very thin junctions and the presence of metal increases the probability of ESD being carried through the junction.

Semiconductor junctions as sensitive ESD constituents are found not only in diodes, transistors, and bipolar integrated circuits, but also in MOS as parasitic diodes and input protection clamps. Although the input port junctions are meant to provide protection from ESD damage, the size of the protective junctions is limited due to cost and performance tradeoffs. Thus, ESD pulses of sufficient energy can damage the input protection junctions.

The temperature coefficient of extrinsic semiconductors is positive. That is, the higher the temperature, the higher the resistance. This feature prevents current crowding and hot spots from forming at low temperatures. However, in the reverse biased mode all the energy is being dissipated by the relatively large voltage drop across the relatively narrow depletion width of the junction. Due to geometrical effects, local resistance variations, and crystal defects, perfectly uniform current distribution does not occur across the junction. As an ESD occurs across the junction, the temperature at the depletion region increases quickly, and the extrinsic semiconducting material becomes an intrinsic semiconducting material, causing a sharp decrease in resistance which results in thermal secondary breakdown. The more rapid the discharge, the more uniform is the increase in temperature and therefore the current across the junction. This means that for short duration discharges of less than 10 nanoseconds, the resultant filament short is wide compared to longer duration discharges.

It is possible for spots to develop but not grow completely across the junction such that at low bias voltages they do not cause a failure condition. However, during operation at certain bias conditions, locally high current densities may exist with a corresponding highly localised large increase in temperature at the previously formed hot spot locations, such that continued growth of a filament short may occur or silicon and metallisation may diffuse through the junction via the electromigration process at temperatures greater than 200°C. Low-leakage, high-breakdown JFET and Schottky barrier junctions seem to be particularly susceptible to this failure process.

It is this same failure process that requires the breakdown test of JFETs be performed as a leakage test rather than puting the junction into breakdown. With low-leakage junctions, highly localised currents can occur during junction reverse breakdown.

With the Schottky barrier junction, metallisation is immediately available to migrate through the junction at localised hot spots. As the current filament develops across a semiconductor junction, it is analogous to putting a parallel resistor across the junction of the same value as the short. However, in some marginally formed hot spots, it may be similar to putting a zener diode and a resistor in parallel with the junction. Failure indication of filament short from a high resistance short is high leakage.

Film Resistors: Resistor material adhering to an insulating substrate comes under the ESDS constituent classification of film resistor. The degree of sensitivity will depend on the ingredients and formulation of the resistor material and size-power considerations.

Hybrid microcircuits frequently contain either thin film resistors or thick film resistors. Hybrid designs which cannot tolerate large changes in resistance, such as precision voltage regulators, are sensitive to ESD.

Thick film resistors consist of a conductive metal oxide as the resistive element, a metal additive to improve electrical performance, and a glass frit to provide a support matrix, adhesion to the substrate, and resistivity control. Such parts are particularly sensitive to ESD. Since the charge is almost always negative for thick films, electrical discharge has been considered as a possible trimming method when conventional trimming overshoots the desired resistance tolerance. It has also been found that the thick film resistance changes are heavily dependent on voltage rather than energy.

Thin film resistors, on the other hand, are more energy dependent and do not have changes greater than 5% in resistance until the energy of discharge is sufficient to cause film rupture.

In addition to hybrid microcircuits, some monolithic integrated circuits may also contain encapsulated thin film resistors, such as polysilicon resistors, as part of an input protection circuit. Discrete encapsulated resistors which contain the film resistor structure are also sensitive to ESD.

Carbon film, metal oxide, and metal film resistors are somewhat sensitive to ESD, especially at low tolerance and low wattage ratings. A frequently recurring ESD problem with resistors is with the 0.05 W metal film, part RNC50, specified at 0.1% tolerance. Putting these parts in a polyethylene bag and rubbing them on another bag is sufficient to shift the tolerance of these resistors.

ESD failure mechanisms of film resistors are not well defined. This is partly the result of not knowing the ingredients and formulations of the resistor material, which are often held proprietary by the manufacturer.

For thick film resistors, the failure mechanism has been modelled as the creation of new shunt paths in a matrix of series-parallel resistors and infinitesimal capacitors isolating metallic islands. With the application of high electric fields, the dielectric breakdown of the glass frit or other isolating dielectric material is exceeded and the ensuing rupture welds metallic particles together in a conducting path known as metallisation melt. Since this model involves a dielectric breakdown process, it is mostly voltage dependent. ▶

WATCH THAT SOLDER SUCKER

Removing integrated circuits soldered directly to a printed circuit board usually requires sucking away the solder from a reheated pad or plated through hole. That is fine for bipolar circuitry, but it can be extremely dangerous for MOS devices. Dan Anderson, president of Anderson Effects, points out that standard plastic solder suckers have been found to produce a static surge of 5000 to 10 000 V at the tip. This tip is invariably in direct contact with a device's lead when the surge occurs, resulting in a damaged or destroyed device. Anderson Effects and other firms now offer static-free metalised plastic models that produce no static charge. For more information, contact Anderson Effects Inc., P.O. Box 657, Mentone, California 92359 USA.

It appears that the ESD behaviour of resistive materials is very much a function of the number of parallel current paths or the number of capacitive couplings between parallel paths in the film structure. The nature of the glass used in the material also appears to be quite important, both because it influences the distribution of the resistive elements and because it can act as a resistive element itself. Thus, the behaviour of different thick film resistor paths to ESD can vary greatly. ESD sensitivity testing, therefore, should be specified for critical tolerance thick film resistors.

For thin film resistors and encapsulated metal film, metal oxide, and carbon film resistors, the failure mechanism is primarily a thermal, energy-dependent process modelled as the destruction of minute shunt paths. This mechanism is associated with an increasing resistance shift on the thin film and metal film type resistor which appears to be voltage dependent. This negative shift is usually not more than 5% and is typically less than 1% before changing to positive shifts as ESD voltage increases.

Some thin film resistors, such as deposited tantalum nitride on SiO_2 substrates, may be so small and power-limited that ESD voltages greater than 5000 volts from a person can melt the resistor open. For most cases, however, a shift in resistance will be the failure indicator.

Thus, for circuit designs tolerant of large resistance changes, the failure may not be critical. Generally, after exposure to an ESD, the stability of the resistor is reduced and the degree of instability is directly related to the level of ESD. Temperature coefficient changes have been known to result from such ESD exposure.

For thick film resistors, the resistance shift is negative. The resistance change can easily exceed 50% with some thick film pastes. Some exceptions to this may occur, especially at low resistance values. For thin film, metal film, metal oxide and carbon film at lower ESD levels, small negative resistance shifts of less than 5% can be experienced. At higher ESD levels, large positive shifts greater than 10% can be experienced, depending on the power rating.

Metallisation Strips. Relatively narrow, thin metallisation strips on a substrate such as SiO_2, which carry current between terminals without any other energy-absorbing element in the path, are susceptible to ESD. These metallisations may consist primarily of aluminium or gold, but can also be multi-layered. The failure mechanism is burnout from joule heating. This type of constituent is often used in monolithic integrated circuits, hybrid microcircuits and multiple finger overlay transistor construction found in switching and high frequency transistors.

Joule heating is most likely to occur when: (1) the ESD source has very low contact resistance, resulting in high currents over short time constants, and (2) a low resistance large area diode is connected by the metallisation path between the two terminals, resulting in large currents due to the low voltage drop in the diode forward biased direction.

Increasing the width or thickness of the strip will decrease ESD sensitivity. The use of glassivation and thinner SiO_2 between the strip and the silicon also reduces ESDS. The failure indicator from this failure mode is open.

Passivated field-effect structures with nonconductive lids. Various NMOS and PMOS integrated circuit designs have been found to fail from very localised high concentrations of positively charged ions on the outer passivated surface of the die.

NMOS designs fail from excessive leakage currents as a result of field inversion between N+ junctions, such as thick field parasitic transistors, intermediate field parasitic transistors, EPROM transistors, and normal select transistors.

PMOS designs, such as the floating gate, EPROM or depletion type field effect transistors, fail when the negative charge on the floating gate is overcompensated by a positive charge, giving an erroneous unprogrammed indication. The effective field from the positively charged ions needed to create this inversion has been found to exceed 85 volts.

Hermetic packages which have recorded this failure mode have nonconductive lids made from non-transparent ceramic, transparent sapphire and transparent borosilicate glass.

These failures can be prevented by grounding the bottom surface of the lid over the die or by initiating preventive measures to avoid electrostatic charging of the nonconductive lid. This failure mechanism is most common with NMOS and PMOS UV-EPROMS having transparent lids. NMOS static random access memory (RAMs) in a ceramic package, however, have also been reported to fail from the ESD failure mechanism. Unless testing shows otherwise, any LSI integrated circuit with nonconductive lids could conceivably have field effect structures which are susceptible to failure from

CONDUCTIVE WRIST STRAP PROTECTS MICROCIRCUITS.

Royston Electronics has recently introduced a conductive wrist strap that meets the latest military specifications for quick release and resistance to line voltages from accidental contact.

Military users have specified these new requirements for wrist straps to prevent static electricity damage to microcircuits while radar, avionics, computer and other equipment is undergoing repair, maintenance or inspection in base stations or the field.

The CP401A grounding strap has a wrist attachment of "Velcro" hook-and-loop tape that separates with a slight pull for safety and to prevent a worker from breaking the grounding wire by inadvertently leaving the work area while still wearing the strap.

The wrist strap is made of conductive polyester ribbon for permanent conductivity, but with built-in resistance to protect the wearer against possible line voltages.

An alligator clip at the other end of the four-foot long grounding wire can be attached to any convenient ground, draining static electricity before it can build up to levels that are harmful to microcircuits.

The wrist strap and ground wire are joined by a standard snap fastener. An extra snap fastener provides a convenient connection for grounding electric tools, bench covers or other items in the work area that must be grounded to prevent static electricity build-up.

Information on this, and the comprehensive range of other anti-static devices, is available from Royston Electronics, Melbourne (03)543-5122 or Sydney (02)709-5293.

undesirable field inversion or gate threshold voltage shifting.

Failure mechanism involves positively charged ion clusters deposited on the die as a result of air breakdown in the air gap between the die surface and the bottom of the package lid. Charging of the bottom of the lid can be induced by several means, one of which is by freeze spraying the package with canned coolant. The positive charging rate of the freeze spray impinging on the top of the lid depends on the flow rate of the coolant from the can. At low flow rates, the charging is negative and does not induce failure; at high flow rates, sufficient positive charging can occur and induce failure. The localised air breakdown in the air gap of the package causes ionised streamers to form from the die to the lid. The positive charge on the bottom of the lid drives the positive charge in the streamer toward the die surface and attracts the negative charge toward the lid. This results in very localised clusters of positive ions on the die surface. Because of the nature of the air breakdown for certain package ambients, this charge is probably identical in type to the very large ions that can be experimentally created by positive corona discharge in the air.

These localised positive charges also cause the formation of inversion layer leakage paths between N+ diffusions and shift the gate threshold voltage on PMOS depletion type transistors. The formation of leakage paths and the gate threshold shifts give rise to isolated circuit failures. This failure mechanism is recoverable by neutralising the positive charge on the outer surface of the die.

On UV-EPROMs with transparent lids, recovery is nondestructive when 2737Å (2.737×10^{-7} metres) ultraviolet light with a minimum photon energy of 4.3 eV is applied to the chip for as short as three to five seconds.

Failure indicators for this failure mode come under the general classification of operational degradation. Operational degradation will take the form of a functional failure. In the case of NMOS UV-EPROMs, certain programmed bits appear unprogrammed and certain unprogrammed bits appear programmed. In one group of failure indicators, bit failures have been organised in columns where programmed bits appear unprogrammed. In another group of failure indicators, bit failures were organised on rows where unprogrammed bits appeared programmed.

The failure indicators for PMOS UV-EPROMs are random single-bit failures throughout the memory which would read as programmed but appear as unprogrammed. Failure indicators for NMOS static RAM have been reported as random hits stuck in "1" or "0" logic state and the adjacent cell also stuck but in the opposite logic state.

Piezoelectric crystal devices, such as quartz crystal oscillators and SAW devices, can fail from ESD, resulting in operational degradation. Electrical parameters of piezoelectric crystals contained within these parts are damaged by excessive driving current. Also, the piezoelectric effect from high voltages causes mechanical stress and movement to be generated in the crystal plate. When the voltage is too great, mechanical forces cause motion in excess of the elastic limits of the crystal and crystal fracture occurs. Fracture may occur as a lifted platelet, as has been experienced in lithium niobate SAW delay lines. Such fractures, when occurring in sufficient number, will cause enough change in the operating electrical characteristics to cause failure.

Closely spaced electrodes. When employing thick metallisation, such as 1.35 microns, gaseous arc discharge in an arc gap 50 microns wide can be used as a protection device to dissipate incoming high voltage spikes. In devices with closely spaced, unpassivated, thin electrodes, however, gaseous arc discharge can cause degraded performance.

Devices that employ thin, closely spaced electrodes include SAW devices. Other parts, such as high-frequency, multiple-finger transistors, and new technology, such as very large scale integration (VLSI) and very high speed integration (VHSI), could also be degraded to failure from arc discharge between metallisation runs. Arc discharge causes vaporisation and metal movement generally away from the space between the electrodes. Melting and fusing do not move the thin metal into the interelectrode regions, but the metal pulls together and flows or opens along the electrode lines. There can be fine metal globules in the gap region, but not in sufficient numbers to cause bridging. Shorting is not considered a major problem with unpassivated thin metal electrodes.

ESD failures have been experienced on SAW band pass filters with thin metal of 0.4 micron and electrode spacing of 3.0 microns.

Detecting ESD damage

By this time, hopefully, the reader has developed an acute sensitivity to the nature of ESD and the insidious nature of ESD damage to the function of an electronic device or a black box. Although there are many thousands of users worldwide, very few have the capability — that is, trained people and facilities — to perform the failure analysis that would lead to the recognition of ESD as the culprit in numerous equipment failures. ▶

NEW MATERIAL WILL OVERCOME SPACECRAFT LOSSES

A new composite material just successfully tested in Britain will overcome a problem in space that has led to the loss of at least two satellites.

Orbiting spacecraft are bombarded by high-energy electrons that cause electrostatic charges of up to 20 000 volts to build up on the surface of the craft. As a result a spontaneous electrical discharge can occur through the outer thermal protective material.

As well as damaging the covering of the satellite, the discharge can cause false electronic signals to disrupt the operation of the craft. If this should happen while it is being manoeuvred in space, the satellite could be lost.

British Aerospace says that these dangers will be eliminated by encasing the satellite in a new composite sandwich material which dissipates the surface charge the moment it hits the spacecraft. The material, which has been patented, also eliminates electrostatic-induced interference, minimises contamination and will prolong the operational life of satellites by maintaining the thermo-optical protection.

In tests, samples of the multi-layer thermal-insulating material have successfully withstood electron energy levels of 30 000 volts at intensities up to 30 times greater than those anticipated in space.

The material has shown that the electrostatic surface potential cannot build up to operationally dangerous levels even at temperatures as low as minus 170° Celsius, where the probability of a discharge is much greater.

British Aerospace says the new material is made up of one of two types of material already used for thermal insulation. However, in this new material it is arranged in composite sandwich form along with two conductive layers of aluminium or carbon, which are earthed to the satellite's main structure.

Electrons penetrating the outer skin are captured by the first conducting layer, while the second aluminium layer on the inner side of the material captures the more highly charged particles that may have penetrated further into the surface of the spacecraft. The inner conductive layer can also act as a radio frequency shield.

The multilayer technique may find further use in protecting spacecraft equipment such as thermal control mirrors, solar arrays and the back of antenna dishes, and British Aerospace say there may be other applications on the ground.

Even with trained people and the proper tools, identifying ESD damage can be difficult. Phil Kohlhaas of 3M Static Control Systems reported at a recent seminar (hosted by Warren Yates of Electronic Products magazine) that 3M sent 100 deliberately static-damaged devices to a testing laboratory. The lab performed a 100% failure analysis — SEM (scanning electron microscope), glass removal, metal removal, the works — and in 60% of the cases, could not identify ESD-related damage that had occurred.

ESD-induced failures are often mistaken for other types of failures. This is particularly true, according to Roy Walker of IITRI/RAC, when it comes to steady-state electrical overstress failures. Agreeing with Walker, Hewlett-Packard's Kim Gray said he encountered a latch-problem in a CMOS device that appeared to result from steady-state-overstress failure; it turned out to be an ESD failure.

A lack of ESD awareness causes many people to limit ESD protection to only the most widely used susceptible devices — FETs without protection, and CMOS with double diode protection. But don't be lulled into a false sense of security if you're using bipolar devices. It's just more difficult to discern the ESD mechanism in a bipolar device than in a MOS device. Walker and others contend that there are many more ESD related problems in bipolar devices than we actually know about because of limitations of ESD failure analysis.

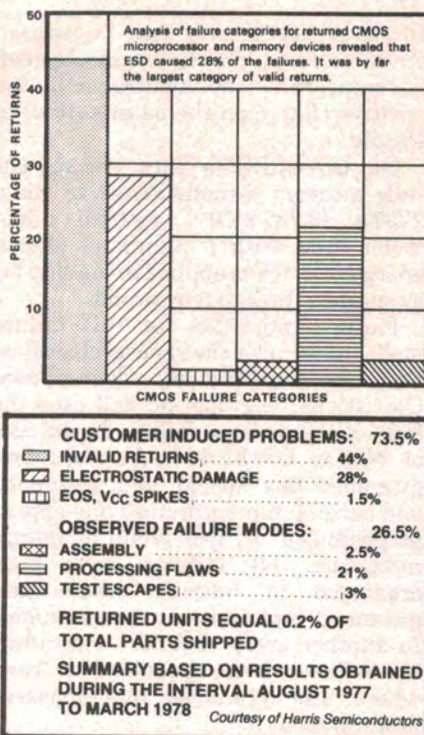


Figure 4. **Typical device degradation threshold.**

The ESD problem is big — make no mistake about that — even though it's really not possible to put a precise handle on just how big. For example, Gene Freeman presented some failure analysis data compiled by Harris Semiconductor on devices returned to them (see Figure 4). Note that ESD comprises the largest single failure mode.

Steve Halperin of Analytical Chemical Labs reported on his company's observations of equipment manufacturers. Where large boards of critical design are involved, he has seen up to a third of all boards started during a day enter a "repair and refurbish" function at some period during handling in the manufacturing facility. Cost of manufacturing failures can be prohibitive, but at least these types of problems are caught at the factory. But what about devices that are degraded by ESD but don't fail until later, out in the field? Halperin quoted figures from some computer manufacturers indicating that 70% of their field service calls were static related.

Degraded devices can become much more than just an expensive field service problem. We cannot ignore the possible substantial costs of product liability, as a failure in a critical end item system might mean substantial property losses or loss of life.

An effective plan to combat ESD requires a strong static awareness on the part of all concerned — factory assembly and test personnel, engineering, maintenance, and field service. But most of all, it requires a strong commitment on the part of top management.

Protecting your equipment

Once it is recognised that static discharge can degrade equipment per-

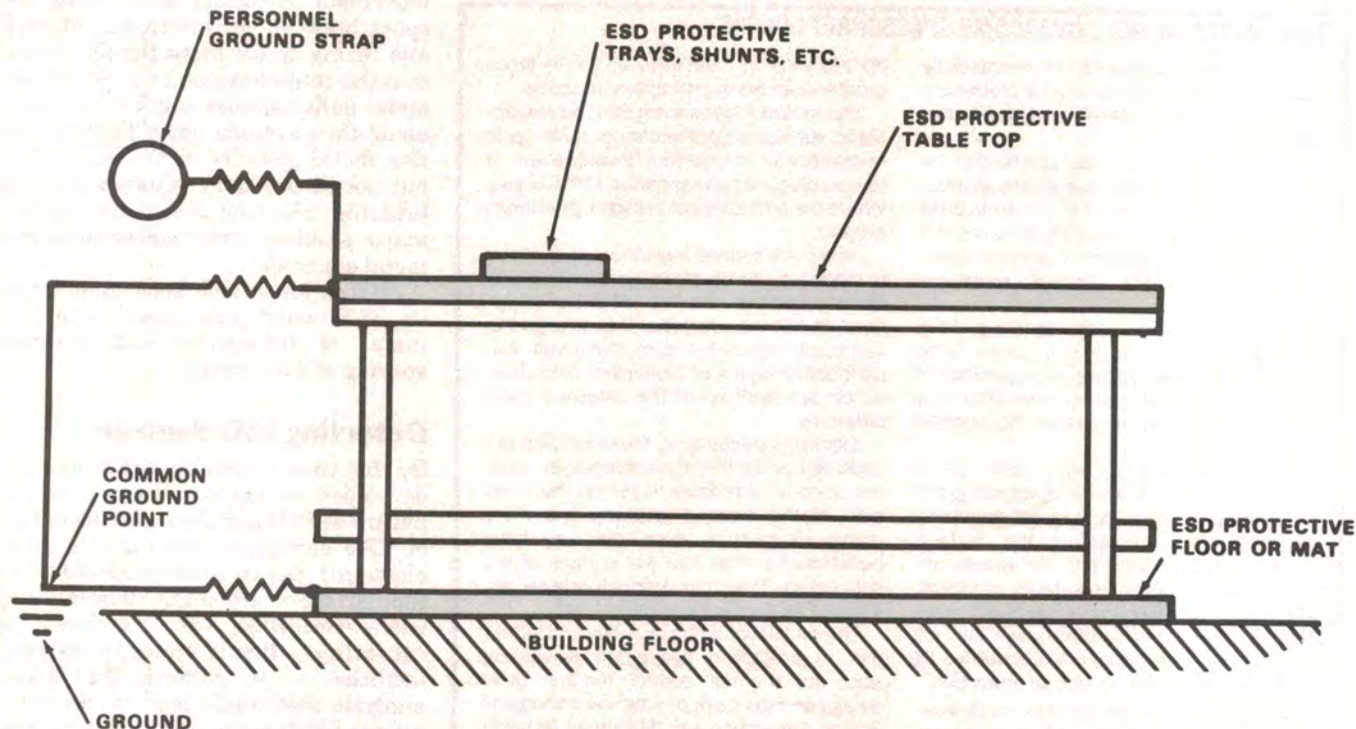


Figure 5. **Typical ESD grounded work bench.**

formance, and that in reality only the 'tip of the iceberg' can be identified as ESD, it is evident that ESD can be combatted only through protective measures. The first and most obvious key, as just stated, is top management's absolute commitment toward a total ESD program.

If management is astute enough to make this commitment, a total awareness and educational programme reaching to all individuals interfacing with the equipment is essential. After awareness is implementation, preparation of specifications and requirements to control work environments, identification and labelling of ESDS hardware, acquisition of antistatic handling equipment and work stations, and coordination of ESD programmes with both suppliers and users. ●

YOUR CHECK-LIST

1. **Identify static-sensitive parts. Manufacturers should be required to clearly mark all parts that are suspected to be sensitive to static charge. Markings should read "static-sensitive devices".**
2. **Provide procedural guidelines to all personnel involved in handling, packaging, testing, assembling, and reworking "static-sensitive devices".**
3. **Maintain good grounding techniques by keeping equipment and personnel at the same potential. Use conductive countertops, floor mattings, wrist straps, or arm sleeves, and make proper connections to a grounding source. (See Figure 5.)**
4. **Use conductive carriers for transporting, storing, and shipping static-sensitive parts.**
5. **Use neutralisers to neutralise charge on personnel, handling tools, and work surfaces.**
6. **Use a noncontacting static voltmeter to regularly monitor static charge in assembly area and on working personnel. This offers control and also keeps personnel static-conscious.**
7. **Failed parts should be treated with the same precautions; otherwise, the cause of the original failure may never be determined.**
8. **Keep all LRU assemblies stored away from high energy sources at all times (e.g: radar, laser, X-ray).**
9. **Keep connector caps on LRUs at all times whenever they are not installed. (Conductive caps are preferred.)**
10. **Never open an LRU on or remove an SRU unless at a properly equipped work station.**

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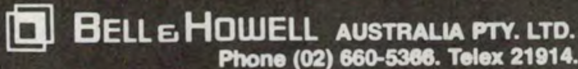

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SWITCHING POWER SUPPLIES

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