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Transistor Bias: The Secret Story

Shore up some of your shaky transistor theory by taking this tutorial.

Bias means different things to different folks. To electronics geeks, it means a steady voltage or current applied to an electrode. The bias sets the operating point, the quiescent point, for a vacuum tube or transistor. The bias applied to a device depends on the application, but it is usually set for linear operation.

Occasionally a device may need to be biased to some other point. For example, a class B stage is biased at or near cutoff and a class C amplifier is biased well beyond cutoff.

Bias comes in two flavors: fixed bias and self-bias. With fixed bias, the operating point is set arbitrarily or in accordance with conditions given in data sheets. Data sheets are available from the manufacturer or the distributor.

Two different transistors of the same type might have different h_{FE} and their collector currents would be different with fixed bias. Self-bias is a form of negative feedback in which the bias varies with the way the device operates. While the feedback is seldom large, every little bit helps to stabilize the operating point.

The desired operating point can be determined from the data sheets for a transistor or tube. The data sheet often gives a set of curves that show the relationship between the currents that exist in the device and the controlling current or voltage. Data sheets may just list the output current for various operating conditions but they don't tell you how to set the operating point. That's for you to figure out, and this article tells you how.

In lieu of more specific information from the data sheets on how to operate the device, an understanding of the device will allow you to wing it. Cut-and-try designs are sometimes unavoidable when you want to operate at some point other than what is listed. Some simple tests can give you a starting point.

If a tube or transistor is to have a linear relationship between input and output, the bias point should be chosen to place the operating point in the most linear region of the transfer characteristics. Obviously that's somewhere between cutoff and saturation, but you would like to be a little closer than that. Saturation occurs when an increase in the input does not result in an increase in the output. Cutoff occurs when a change in the input does not cause a change in the output. For junction transistors, saturation occurs when the base-emitter junction is forward-biased and the collector-to-emitter voltage is less than 0.6 V.

The collector current in a bipolar transistor, either NPN or PNP, is proportional to the base current. Since bipolar transistors are current-controlled devices, voltages are seldom shown except as limits. The difference between an NPN and a PNP is the polarity of the voltages applied and the direction of current flow. The base-emitter voltage is practically constant at about 0.6 or 0.7 volts for conducting silicon transistors and about half that for germaniums. That's a bit of information that isn't even mentioned in the data sheets. I guess the manufacturers expect everybody to know that. So now you know.

The bias provides a DC current to the base of a transistor and sets the DC operating conditions. The resistance r_b looking into the base of a common emitter stage is in the range of a thousand ohms, and is the resistance that the signal source must drive. However, when the collector current is a fraction of a mil, the base resistance is higher.

The input resistance r_e looking into the emitter of a common base amplifier is even lower, in the range of a few ohms. The bias effects are the same whether the device is operated common emitter, common base, or common collector. Collector current is proportional to base current, and the base-emitter voltage is about 0.6 V or 0.7 V.

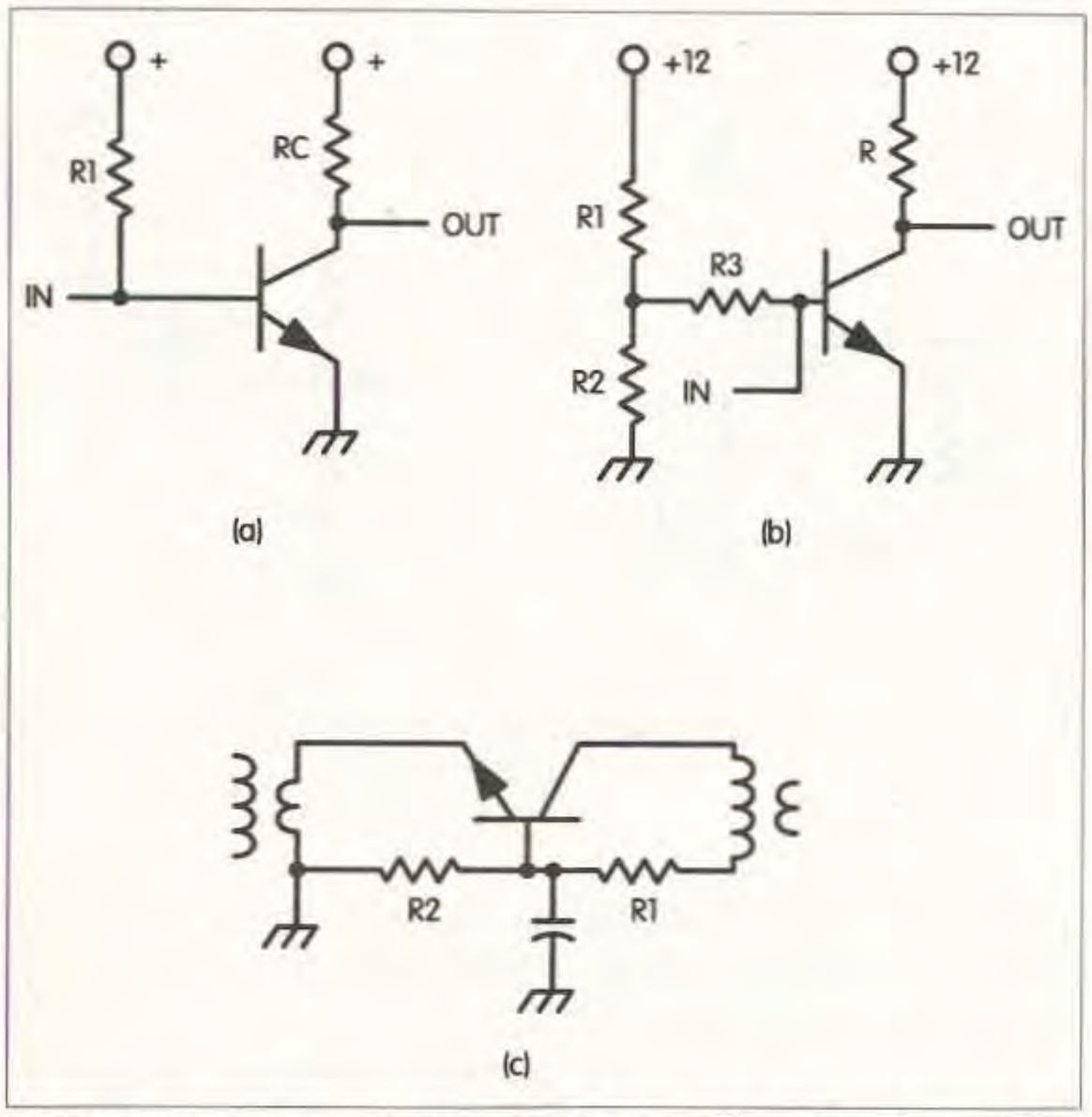

Fig. 1. *(**a**) A common-emitter amplifier can have fixed bias. (**b**) A common-base amplifier can have fixed bias. (**c**) A low resistance bias source is required when I_{CBO} is high.*

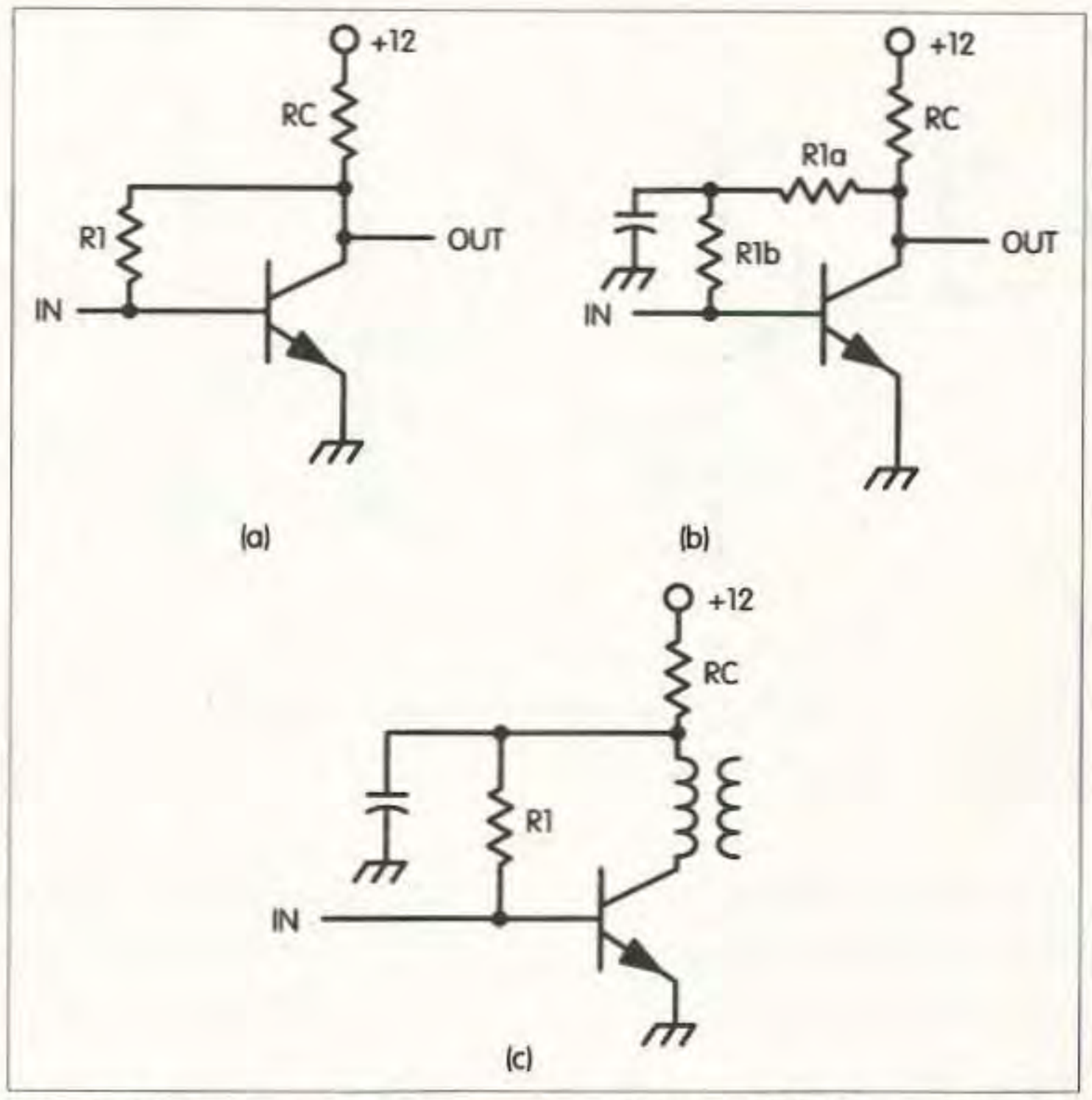

Fig. 2. *(**a**) A common-emitter can be self-biased. (**b**) Degeneration of AC in self-bias can be eliminated. (**c**) Self-bias can be obtained with a low DC resistance transformer in the collector.*

The DC operation of small transistors is quite similar, even though the AC or RF performance is quite different. Therefore, biasing considerations are the same. For example, the data sheets of the 2N3904, a small general purpose silicon BJT, lists h_{FE} as 100 to 300 when I_C is 10 mA, and 70 minimum when I_C is 1 mA, and 60 minimum when I_C is 50 mA. From these values, it can be inferred that base current will be less than 0.1 mA for 10 mA of collector current, 14 µA for 1 mA of collector current, and 0.83 mA for 50 mA of collector current. This wide variation in h_{FE} implies that the required bias is also not known precisely. Even so, the published information is a starting place. If the h_{FE} is known from measurements, bias currents are known. Otherwise, make a guess from what's given. A procedure for establishing the h_{FE} of BJTs and V_{GS} for JFETs is described later. For the moment, assume that the h_{FE} is known.

Fig. 1 shows a 2N3904 with fixed bias. Ten milliamps of collector current requires less than 0.1 mA of base current. Bias current I_B is provided by R1 and R1= (12 - 0.6)/I_B. When the supply is 12 V and I_B is 0.1 mA, R1 is about 114 k. Because h_{FE} is probably greater than 100, 120 k would be a good starting point.

At high temperatures, I_{CBO}, the collector-to-base current with the emitter open, can be a problem when the bias resistor is high. Silicon transistors have low I_{CBO}, and present no problems except at high temperatures. That is not the case with germaniums.

Limiting bias resistors to a few tens of thousands of ohms for silicon transistors reduces changes in bias with I_{CBO}. An extreme example is a divider of 47 k and 620 Ω from 12 V. The divider will provide 0.1 mA of bias current and I_{CBO} can be ignored. But, the 620 Ω will severely load the signal source. There are alternatives that produce the desired bias current from an acceptably low source resistance.

The resistance of the bias source can be reduced by using a resistive divider to obtain the bias voltage. For example, in **Fig. 1(b)**, a divider, say 3.9 k and 20 k, produces 1.9 V from 12 volts with an internal resistance of $(3.9^{-1} + 20^{-1})^{-1}$ = 3.2 k. To provide 0.1 mA to the 0.6 V base from a 1.9 V source requires a resistance of 13 k. Therefore, an additional series resistance of about 10 k is required. The resistance that loads the signal source is about 13 k in parallel with the base resistance of the transistor r_b. Resistance r_b is in the

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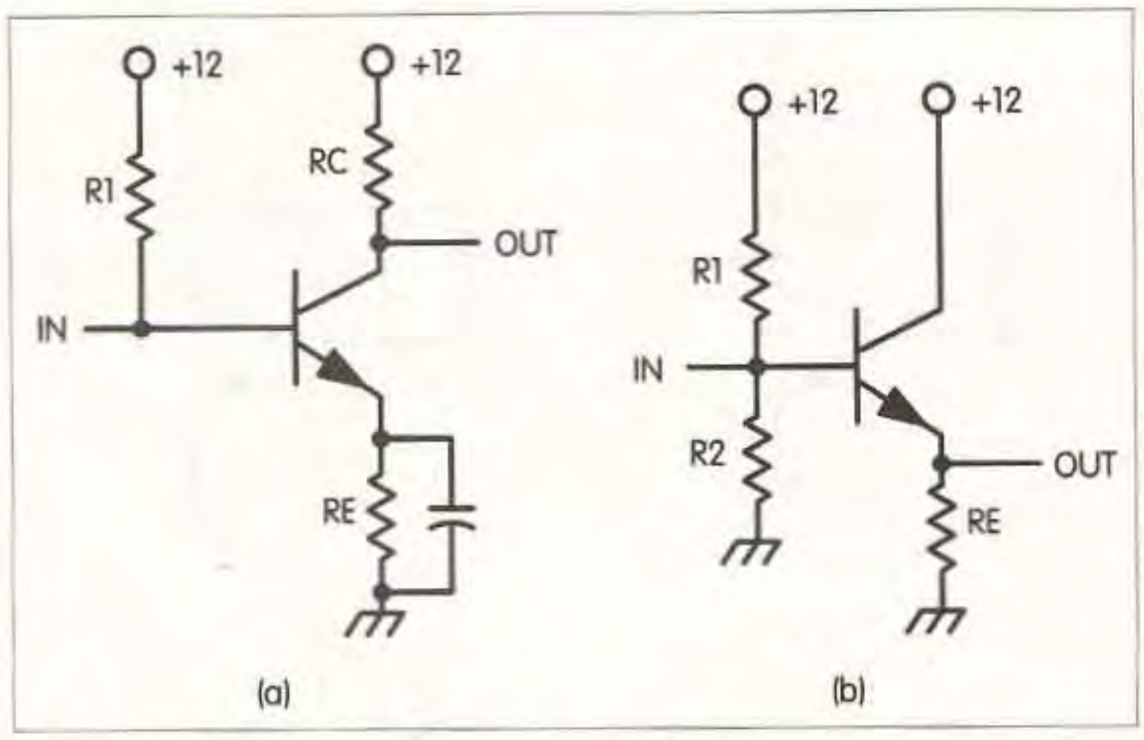

Fig. 3. *(a) Self-bias can be generated in the emitter. (b) An emitter follower has self-bias.*

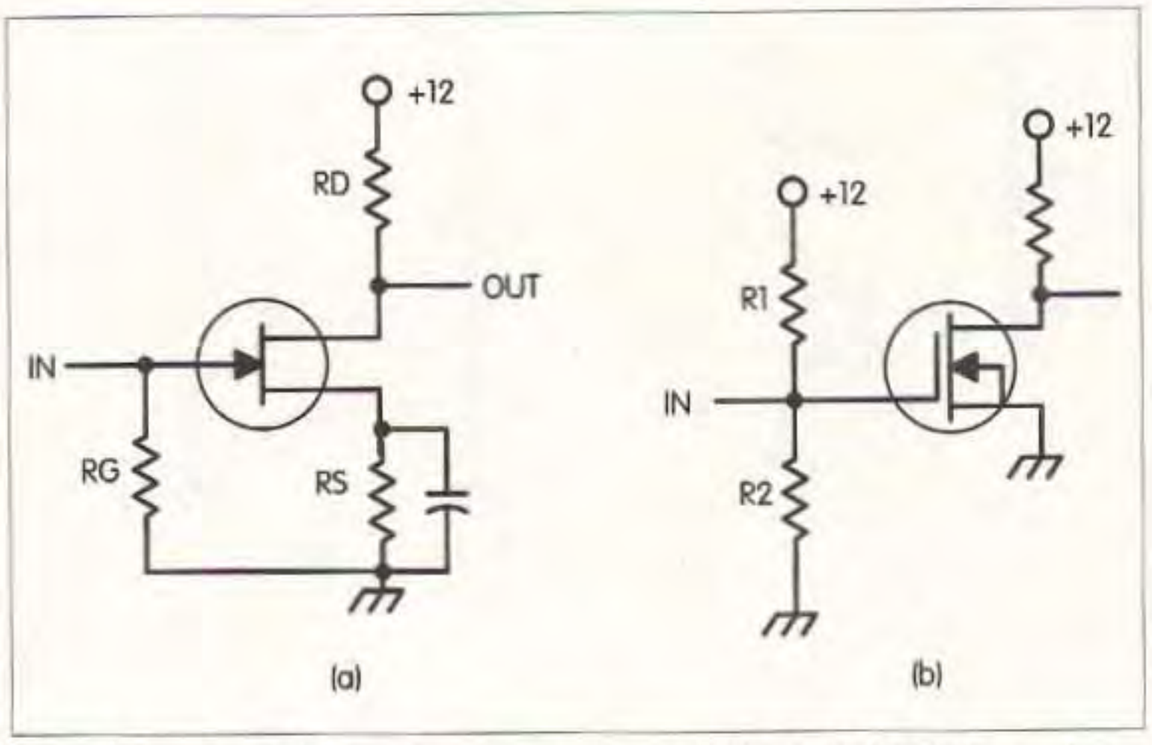

Fig. 4. *(a) An FET can be source-biased. (b) A MOSFET can have fixed bias.*

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range of 1 k, so the input is essentially driving r_b.

Biasing a common base stage is shown in **Fig. 1(c)**.

The common base amplifier is suitable as an RF/IF amplifier because there is negligible positive feedback from collector to emitter. (That is not the case for a common emitter amplifier at IF.) The resistance looking into the emitter r_e is quite low, but the interstage transformer can transform the low input impedance to the desired level. The base impedance should be essentially zero. A divider of 2 k and 27 k can produce 0.6 volts and 0.1 mA to the base. The resistor values are obtained as follows: The current in R2 is 0.6 V/2 k = 0.3 mA and the current in R1 is 0.3 mA + 0.1 mA = 0.4 mA. The voltage across R1 is 12 V - 0.6 V. Therefore, R1 is 11.4/0.4 mA = 28.5 k ≈ 27 k.

Methods of generating bias in which the bias current decreases when collector current increases with higher h_{FE} are called self-bias. Self-bias tends to make the collector current independent of the variability in a particular transistor type.

Fig. 2 shows three forms of self-bias. In **Fig. 2(a)**, the bias resistor is connected to the collector. An increase in collector current decreases collector voltage, and the bias current falls, which decreases collector current. This negative feedback tends to stabilize the operating conditions of the transistor. Unfortunately, the negative feedback also applies to AC variations and reduces the gain.

The negative AC feedback can be eliminated by splitting the bias resistor R1 into two parts and bypassing their junction for the frequency of interest as shown in **Fig. 2(b)**. The reactance of the bypass capacitor should be low compared to the parallel resistance of the two resistors, $X_C < (R1a^{-1} + R1b^{-1})^{-1}$.

In **Fig. 2(c)**, when the collector load is a low DC resistance primary of a transformer, the low DC resistance doesn't offer a significant change in DC voltage with changes in collector current. Dropping the collector voltage with a bypassed resistor can produce a meaningful change in collector voltage. The DC voltage at the collector should be half the supply voltage to allow maximum output voltage swing. Since the voltage at the resistor is bypassed, the voltage doesn't change with signal and it can be fed back to the base without degeneration.

Another way of obtaining self-bias is shown in **Fig. 3(a)**. A resistor R_E in the emitter raises the emitter voltage E_E to $I_C \times R_E$ and the base voltage raises accordingly. The voltage divider in the base produces the base voltage of E_E + 0.6 V and provides the desired bias current.

For example, if the emitter current is 10 mA and R_E is 200 Ω, E_E is 2 volts and the base is 2.6 volts. When the supply is 12 volts, the bias resistor must be

(12 - 2.6)/0.1 mA = 94 k. The voltage across R_E varies with the input and causes degeneration unless R_E is bypassed.

The capacitor used to bypass R_E must have a reactance low compared to the parallel combination of R_E and the resistance seen looking into the emitter r_e. The data sheets typically do not list a value for r_e, but it is only a few ohms. Therefore, the bypass capacitance must be quite large, typically in the range of 100 µF, to bypass 300 Hz.

Biasing of an emitter-follower is similar to biasing a stage with unbypassed emitter self-bias. An emitter-follower is shown in **Fig. 3(b)**. In an emitter-follower, the output is taken from the emitter instead of the collector. The emitter follower is characterized by a high input resistance, low output resistance, 0° phase shift, near unity gain, and excellent linearity. The good linearity and stable operating point arises from the 100% negative feedback provided by the unbypassed emitter. The bias can be obtained as shown in **5(a)** or **5(b)**.

For example, if the output of an emitter follower is to be 2 volts peak-to-peak, the minimum emitter voltage must be greater than zero when the input is minimum, say, 0.5 V. The emitter voltage will then swing from 0.5 V minimum to 2.5 V maximum around a DC level of 1.5 V. The input must swing from 1.1 V to 3.1 V. When the emitter resistance is 50 Ω, the DC emitter current must swing from 10 mA to 50 mA with an average (DC) of 30 mA. Assuming h_{FE} is 100, bias must set the base at 1.5 V + 0.6 V = 2.1 V with base current of 0.3 mA.

If R2 is arbitrarily chosen as 10 k, the voltage across R2 will be 2.1 V and the current in it 0.21 mA. The current in R1 is $I_{R2} + I_B$, or 0.21 mA + 0.3 mA = 5.1 mA and the voltage across it will be 12 V - 2.1 V = 9.9 V. R1 then must be 19 k or approximately 20 k. The output impedance is r_e (a few ohms). The load seen by the input signal is $h_{FE}R_E$, 100 x 50 = 5 k, in parallel with the bias network $(10\ k^{-1} + 20\ k^{-1} + 5\ k^{-1})^{-1}$, or about 2.8 k.

Biasing FETs is even easier than biasing BJTs, because FETs are voltage-controlled. It is more like biasing a tube. (If you're familiar with tubes.) A wag once said a tube is an N-channel depletion mode JFET with a light in it to tell you when it's good. That's a fair analogy, but there is a major difference. In a depletion mode JFET, the drain and source are relative — they can be interchanged without any change in operation. You can't do that with a tube. In the JFET, the most negative terminal is the gate. The other two terminals are drain and source, but which is which doesn't make any difference. The most positive one becomes the drain and the other one becomes the source.

In a depletion mode device, the drain current is maximum when the gate-to-source voltage V_{GS} is zero. In an N-channel device, current flows into the gate when the gate is positive with respect to the source, like a grid current in a tube. A reverse-biased gate current is in the range of nanoamps, compared to microamps of contact current in tubes.

The same biasing schemes are used with JFETs that are used with tubes. Like tubes, fixed bias needs a negative supply, which may be an inconvenience, but source bias, akin to cathode bias, is most appropriate. A resistance R_S in the source, as shown in **Fig. 4(a)**, produces a voltage that raises the source potential and makes the gate effectively more negative. The drain current I_D, which is the same as the source current, produces a source voltage $I_D R_S$. The gate must be returned to the most negative potential.

Of course, P-channel devices use negative voltages instead of positive voltages. But otherwise they act the same.

The source voltage produces negative feedback that applies to AC as well as DC current. Bypassing the source resistor eliminates the AC variations. The bypass capacitor's reactance should be lower than the parallel combination of $1/Y_{fs}$ (equivalent to $1/g_m$) and R_S at the lowest frequency of concern. Y_{fs} is typically in the range of 2000 µmhos. When the g_m is 2000 µmhos, the resistance seen looking into the source is 500 Ω, and a 1 µF can be used to bypass 300 Hz.

The drain current vs. drain voltage curves, analogous to a tube's E_P/I_P curves, show how the current responds to V_{GS}. Drain current is essentially constant like a pentode when drain voltage is greater than pinch-off. Pinch-off is approximately V_{off}, the gate source voltage needed to reduce drain current to zero. For short channel devices, a construction characteristic not mentioned in the data sheets, pinch-off is about twice V_{off}.

It's worth noting that g_m varies with drain current and is maximum at V_{GS} = 0 V. A characteristic g_{fso}, g_{fs} with gate voltage zero, is often given in data sheets, but it is seldom realizable because the N-channel gate is usually biased negative with respect to the source and consequently I_D is less than I_{DSS}.

Enhancement mode MOSFETs are a bit different from depletion mode devices. N-channel enhancement mode devices are cut off when V_{GS} is 0 V and conduct when the gate is positive with respect to the source. The gates of these devices are insulated and do not draw current when they are positive. These devices are usually characterized for use as switches but they can be biased to operate in a linear fashion.

For example, the VN2222LL, a small N-channel enhancement mode MOSFET, is linear when the gate is about 4 V positive and the signal levels are kept small. The transistor starts to conduct with V_{GS} (gate to source voltage) of about +3 volts. The drain current is 1.5 A when V_{GS} is about +10 V. When used as a switch, V_{GS} is normally held at zero and the switching voltage raises the gate above 3 V. The drain-to-source resistance is typically

only a few ohms when the gate is 10 V or more positive. Some large die MOSFETs have R_{DS} of less than 0.02 Ω, and rival mechanical relays for low contact resistance after millions of operations.

Biasing for linear operation at 4 V only requires a voltage divider of 470 k and 1 meg from 12 V. All of the biasing schemes applicable to BJTs can be used with enhancement mode MOSFETs without concern for base current.

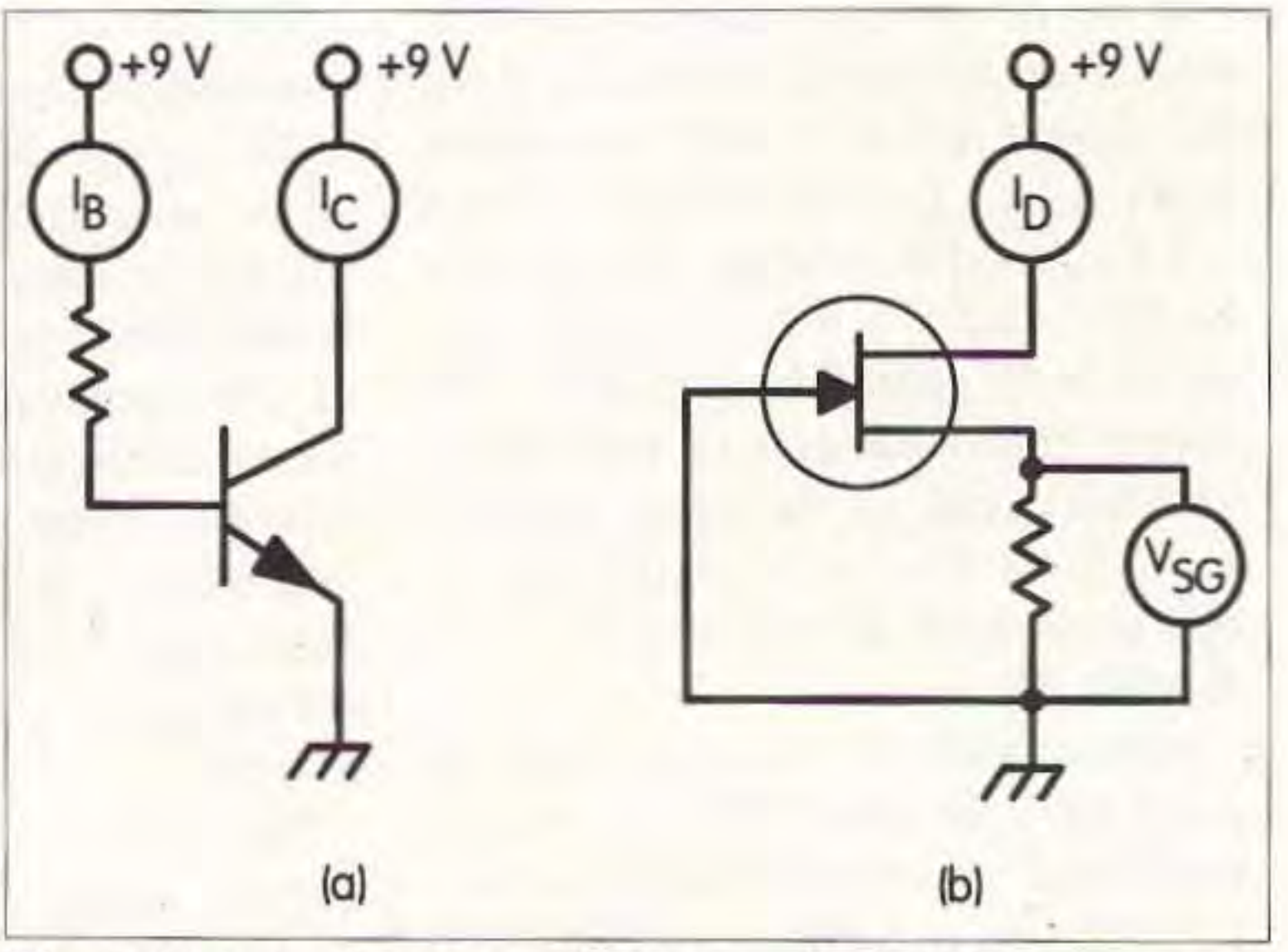

Fig. 5. (a) A simple test circuit finds h_{FE} of a BJT. (b) A test circuit for finding V_{GS}, and I_{DSS} of a FET.

If your requirements fall outside the box, you can bias the device to suit your particular needs. While the data sheets don't always have the data you want, some simple tests can usually generate the information you need.

Fig. 5(a) shows how to determine the h_{FE} of a BJT and **Fig. 5(b)** can answer the question of what bias voltage is needed for a FET to produce the I_D you want. A calculator is a great help in easing the calculations, but the measurements and calculations are simple.

The h_{FE} of a BJT can be found with the test circuit shown in **Fig. 5(a)**. The current in the base and the collector current are measured and h_{FE} is simply I_C/I_B. With h_{FE} known, the bias current required for any quiescent collector current can be calculated, $I_C = h_{FE}I_B$.

Finding the bias conditions for a depletion mode JFET are a bit more involved. **Fig. 5(b)** shows the test circuit for an FET. A known resistor in the range of 10 k or 20 k is in the source of a depletion mode JFET. The collector current I_{DSS} is measured with the resistor shorted and collector current I_D is measured with the resistor in place. The voltage V_{GS} across the source resistor is measured when the drain current is I_D.

The process for finding the relationship between I_D and V_{GS} is as follows: (1) Measure the drain current I_{DSS} with the source resistor shorted. (2) Remove the short. Measure the drain current I_D and the voltage V_{GS} across the source resistor. (3) With I_{DSS}, I_D, and V_{GS} determined, V_{off} can be calculated with the following equations.

$$I_D = I_{DSS}(1 - V_{GS}/V_{off})^2$$

where I_{DSS} is the drain current when V_{GS} is zero and V_{off} is the voltage needed to reduce drain current to zero. Rewriting this to solve for V_{GS} and V_{off} yields:

$$V_{GS}/V_{off} = 1 - \sqrt{(I_D/I_{DSS})}$$

$$V_{off} = V_{GS}/[1 - \sqrt{(I_D/I_{DSS})}]$$

With V_{off} and I_{DSS} known, I_D for various values of V_{GS} can be calculated with the first equation.

While you have the calculator warmed up, it is just a step away for finding the g_m and gain. Gain is g_m x R_L. R_L is the drain load and g_m is:

$$g_m = 2/(V_{GS} - V_{off}) = [2/\sqrt{(I_D I_{DDS})}]/V_{off}$$

Biasing of transistors is not difficult, even though the calculations to find the starting point may be a chore. Just keep in mind that BJTs are current-controlled. That is, the collector current is controlled by the base current. The resistance looking into the base is low. FETs are voltage-controlled. The drain current is controlled by the gate-source voltage. The resistance looking into the gate is essentially infinite.