I²L A New Transistor Logic Family

New techniques provide high speed with low power requirements.

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IN A seemingly endless quest for ever smaller and faster circuits, semiconductor researchers have developed a number of different transistor logic families. Among those that have already made their splash are: direct-coupled transistor logic (DCTL), resistor-transistor logic (RTL), resistor-capacitor transistor logic (RCTL), diode-transistor logic (DTL), transistor-transistor logic (TTL), and most recently metal-oxide semiconductor (MOS) and complementary-symmetry MOS (CMOS) logic.

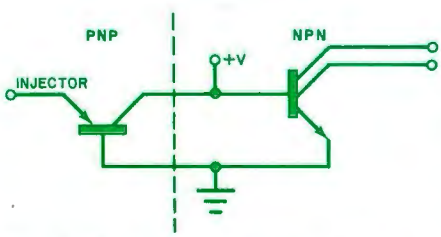

Fig. 1. The npn transistor is an inverter; the pnp serves as a current source as well as load.

Now, a promising newcomer has been added to the list. It goes under the name integrated injection logic, or I²L. Said to be as much as two years ahead of the previous state of the art, it employs the same proven manufacturing process as used for TTL. The IC's have high packaging density, have speeds approaching TTL, and consume only about a hundredth of the power of equivalent TTL devices.

Injection logic achieves its high performance by reducing a logic gate to a single complementary transistor pair as illustrated by the basic gate in Fig. 1. The vertical (npn) transistor operates as an inverter, while the lateral (pnp) transistor serves as both the current source and load. By contrast, a typical TTL gate requires six or eight transistors and must have source or load resistors.

When the I²L gate is formed on silicon, both transistors are merged into the area of a single multiple-emitter transistor. This eliminates space-consuming device isolation, which, in addition to the absence of resistors, accounts for I²L's circuit density. That density can be up to 100 times greater than is possible with TTL. For example, as many as 3000 logic gates, or 10,000 bits of memory, can be packed on a single I²L chip. The table compares several of the more important parameters for I²L and TTL devices.

Perhaps the most revolutionary attribute of I²L technology is its versatility. Furthermore, I²L circuits can easily interface with other circuits. It enables the designer to put both digital and analog circuits on the same chip. Because it uses thoroughly proven manufacturing techniques, it is low in cost and lends itself to the full range of microcircuit applications.

Evolution of I²L. The advantages of I²L came from shrinking DCTL, shown in Fig. 2, into a compact equivalent structure. The input circuit consists of three transistors in parallel. If one or more of these transistors is conducting, they act as short circuits, preventing current from flowing through the load gates. When all input transistors are cut off, current flows through the load gate transistors. This circuit action produces the common NOR logic function.

COMPARISON OF TTL AND I²L DEVICES

Parameter	I²L	TTL
Packing density	120-200 gates/mm2	20 gates/mm2
Gate delay	25-250 ns	10 ns
Power dissipation (per gate)	6 nW - 70 µW	10 mW
Supply voltage	1 - 15 V	3 - 7.3 V
Logic voltage swing	0.6 V	5 V
Current range	1 nA - 1 mA	2 mA

By replacing the three load resistors with an active current source, I²L simplifies the rather bulky DCTL. Then, the transistors with connected bases are replaced with a multiple-collector (npn) transistor. This is easy to do because all of the DCTL transistors have a common grounded emitter. In most I²L gates, a simple pnp transistor

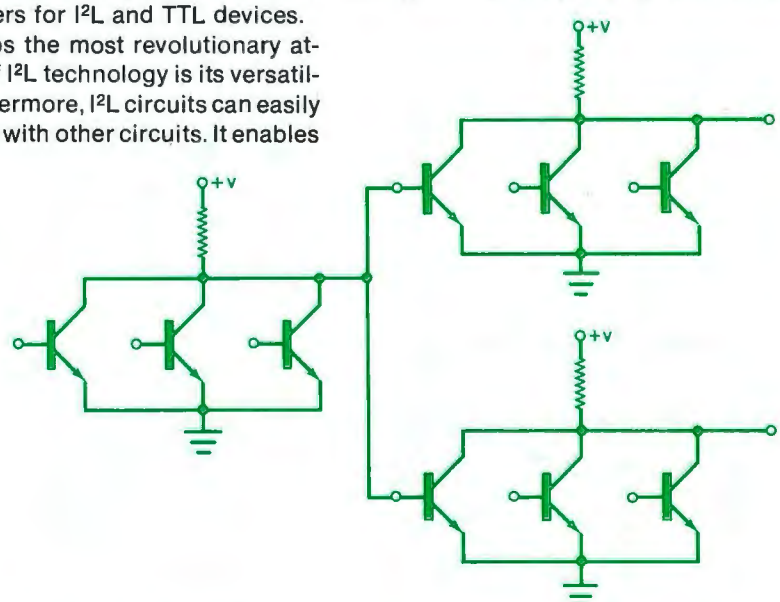

Fig. 2. A DCTL circuit which can be made smaller using I²L.

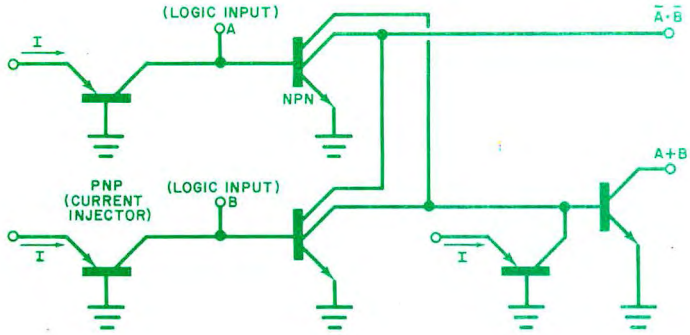

Fig. 3. A simple NAND gate using integrated injection logic.

serves as the active current source by injecting minority carriers into the emitter of the npn transistor. A light source can be used for injection in electro-optical applications.

The refinement of the DCTL gate results in the complementary transistor pair shown in Fig. 1. It can be seen that the base current of the npn transistor is common to the collector of the pnp current source, while the base of the current source is common to the emitter of the npn transistor. The emitter of the pnp transistor, called the injector, is common to all I^2L gates on a chip.

The circuit shown in Fig. 3 is an example of the simplest version of an I^2L NAND gate. Positive NAND logic is implemented by using the multiple-collector npn transistor as an inverter. Positive NOR logic can also be performed by OR'ing the I^2L gate outputs.

The npn transistor is normally biased on (low output) by the current-injector pnp transistor, which is connected between the base of the npn transistor and the external current source. Switching action is accomplished by steering the injector current. This is done by controlling the input voltage, V_{BE}, to the gate. A low input voltage of less than V_{BE} (750 mV) pulls injector current out of the input through the on, or low, output of the driving gate. Thus, deprived of its base current, the npn transistor cuts off and the output goes high. This NAND circuit is converted to NOR logic by wiring the outputs as shown in Fig. 3.

Device Construction. Because of the common elements described above, the entire I^2L gate takes up the space of a single multiple-emitter transistor when laid out on silicon. Here's how this is done:

The high density of I^2L is due in large part to its simplicity and economy of design. The n+ region in Fig. 4 serves as a common ground plane to interconnect all grounded-emitter transistor gates on the chip. The n region above the n+ region is both the emitter of the vertical (npn) transistor and the base of the lateral (pnp) transistor. The two p regions serve as the base of the npn transistor and also as the collector of the pnp transistor. The two n+ regions are the multiple collector of the npn transistor. Finally, metallized connectors are added to provide interconnection between the gates. Notice that the pnp transistor is integrated into the npn transistor. It doesn't exist as a discrete component, yet it can supply injection current for a series of npn gates.

The result of this manufacturing technique is the smallest component size of any current IC manufacturing technology. The I^2L gate is less than one-tenth the size of conventional TTL or CMOS gates. Even the latest LSI forms of TTL gates occupy four times as much space as the I^2L gate.

Two Types. Although I^2L is a young technology, two different versions are already in production. One is the isolated variety that uses a reverse-biased pn junction for component isolation. Since this completely isolates adjacent devices, it is used in I^2L chips that contain mixed functions. Such functions as LED drivers, memory decoders, current regulators, op amps, comparators, oscillators, and TTL or ECL devices can be combined on a single monolithic chip. Texas Instruments has in production an isolated I^2L digital watch chip that measures ⅛" (3.2 mm) on a side and contains logic, timing, and display drivers. The chip is approximately 25% smaller than the typical MOS versions. This chip is being used in a digital watch made by Benrus. An advantage of I^2L in this application is that cost can be reduced by using crystals operating at 4 MHz. This is not possible when using CMOS.

Also on the market is a 100-ns medium-performance TI RAM (74S209) with I^2L gates as the memory and TTL circuits as peripheral interface elements.

The second type of device in production is the nonisolated I^2L chip, used in very complex digital IC's. Isolation is not required because all circuits on the chip are I^2L devices. Consequently, higher functional density is achieved when compared to isolated I^2L chips. The first LSI digital circuit built with nonisolated I^2L technology is the Texas Instruments SBP0400 4-bit microprocessor. This chip has more than 1450 gates in a single 40-pin IC package. To date, it is the most complex standard bipolar chip in production. It has features that could be duplicated only by using 30 to 40 small- and medium-scale TTL IC's.

A Look Into the Future. As impressive as today's I^2L devices are, even better ones are coming. Right now on the way are DVM circuits, high-frequency counters, digital tuners, read-only memories (ROM's), control logic for calculators, touch-control and linear circuits for radio and TV, and circuits for telephone touch-dialing systems.

Intensive research and development continues to increase the speed of experimental devices. For example, researchers at IBM's Semiconductor Development Laboratories in West Germany are using Schottky-diode clamps on I^2L outputs to decrease gate delays. They estimate that speeds faster than 5 ns will be obtained in the near future. ◈

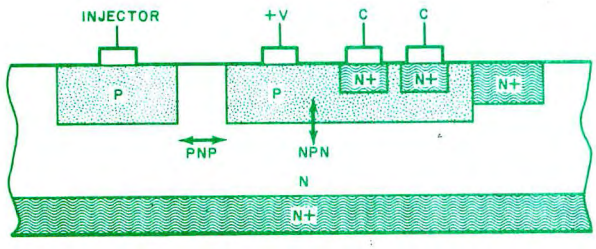

Fig. 4. Simplified diagram shows how I^2L is constructed.