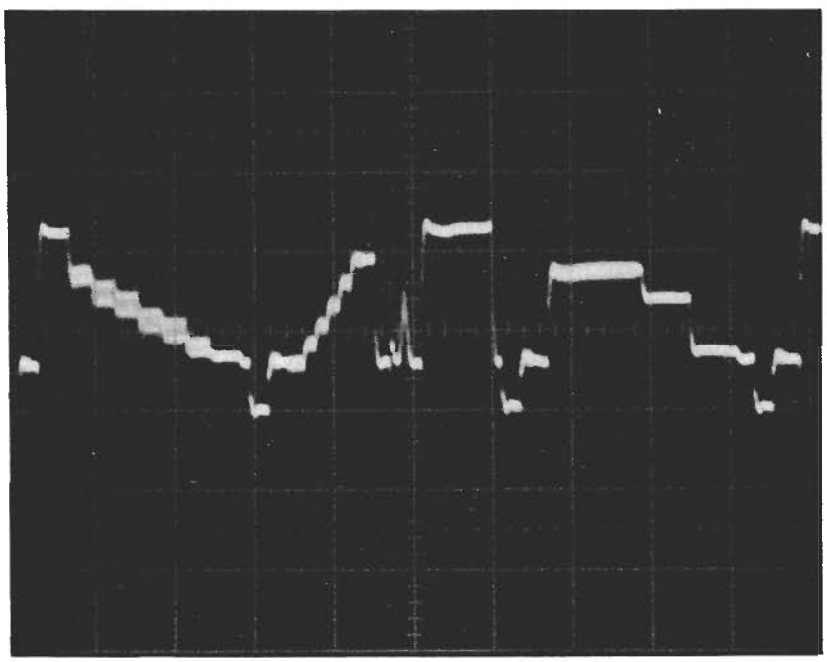
BUILD THIS

VIDEO SYNC SEPARATOR FOR YOUR



OSCILLOSCOPE

STEVE PENCE

With this oscilloscope upgrade, you can stabilize your display of video signals and see what they really look like.

IF YOU'VE EVER WORKED WITH TELEVISIONS or video recorders, you know how difficult it can be to trigger an oscilloscope to provide a really stable display—especially if you want to examine one line of video. And what's even more frustrating is that when you do finally obtain a good display, the part of the waveform you want to examine seems to be just beyond reach. It seems that no combination of position control, sweep rate, and expansion will get you just where you want to be.

If you own a triggered-sweep oscilloscope, there is a solution! We'll show you how to add a video-sync separator and delayed-trigger capability to your oscilloscope. With your upgraded oscilloscope, you'll *really* get to see those video signals.

The circuit can be broken down into four major sections:

- Input buffer/amplifier and video clamp circuit.
- Video-sync separator.
- Digital vertical-pulse separator.
- Trigger-delay section.

The block diagram of Fig. 1 shows the various sections of the circuit and how they relate to each other. The basic concept of the circuit is to extract the vertical-sync pulse from the video signal and use it to trigger a scope. However, the trigger pulse is not applied directly to the scope. Instead, it is first delayed by a user-adjustable period of time.

Since the scope will not begin its trace until it is triggered at the end of the delay time, and since we have control over the length of the delay after the trigger event (which is a vertical-sync pulse), we can examine any part of the waveform that occurs after that event in great detail.

A useful feature of this upgrade is a clamped video output. The clamp circuit forces the tips of all the sync pulses to line up at the same DC level. So even as the brightness of the scene changes and the average video-voltage level changes, the displayed waveform will remain on exactly the same baseline, making amplitude measurements much easier.

A look at the circuit

The schematic of the sync-separator circuit is shown in Fig. 2. We'll start our description of the circuit at J1, the video

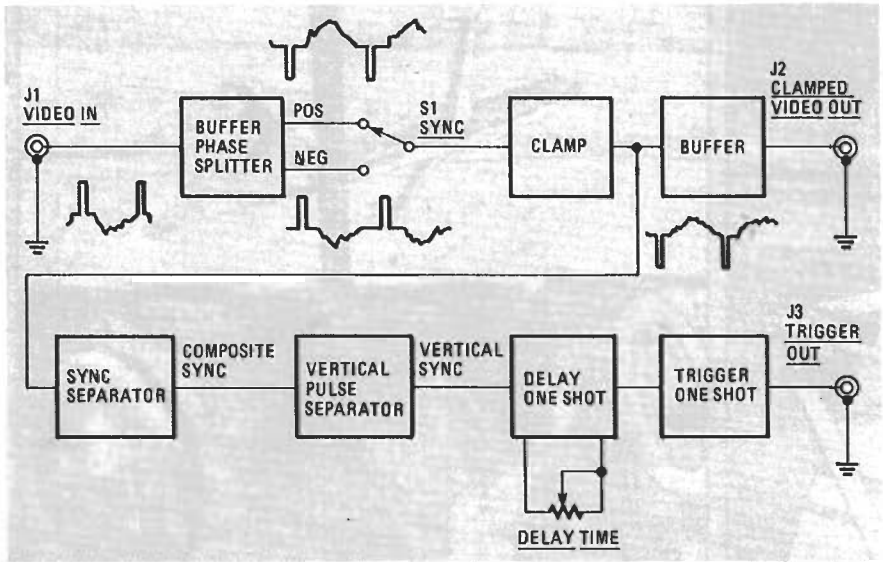


FIG. 1—THIS BLOCK DIAGRAM shows the main sections of the oscilloscope upgrade. The circuit extracts the vertical-sync pulses from a video signal and then delays it's application to the external-trigger input of the scope. Note that a clamped-video output is also available.

input. Diodes D1 and D2 provide over-voltage protection for the gate of Q1, which is a simple phase splitter. The splitter—which can provide either a normal or inverted version of the input signal—is necessary because the video-clamp and sync-separator sections that follow must always see a video signal with its sync pulses going negative. Switch S1 is used to select the appropriate polarity and send the signal on to the video clamp.

The clamp is made up of C2, D3, D4, R4, R11, and R12. Capacitor C2 couples the video signal into the clamp circuit. When the video voltage goes negative during sync-pulse time, diode D3 is forward biased, and C2 quickly charges up to the peak value of the signal. As the signal swings positive, diode D3 is reverse biased and C2 must discharge through R11 and R12. The discharge current produces a positive bias, voltage across R12 which is directly proportional to the peak voltage of the waveform.

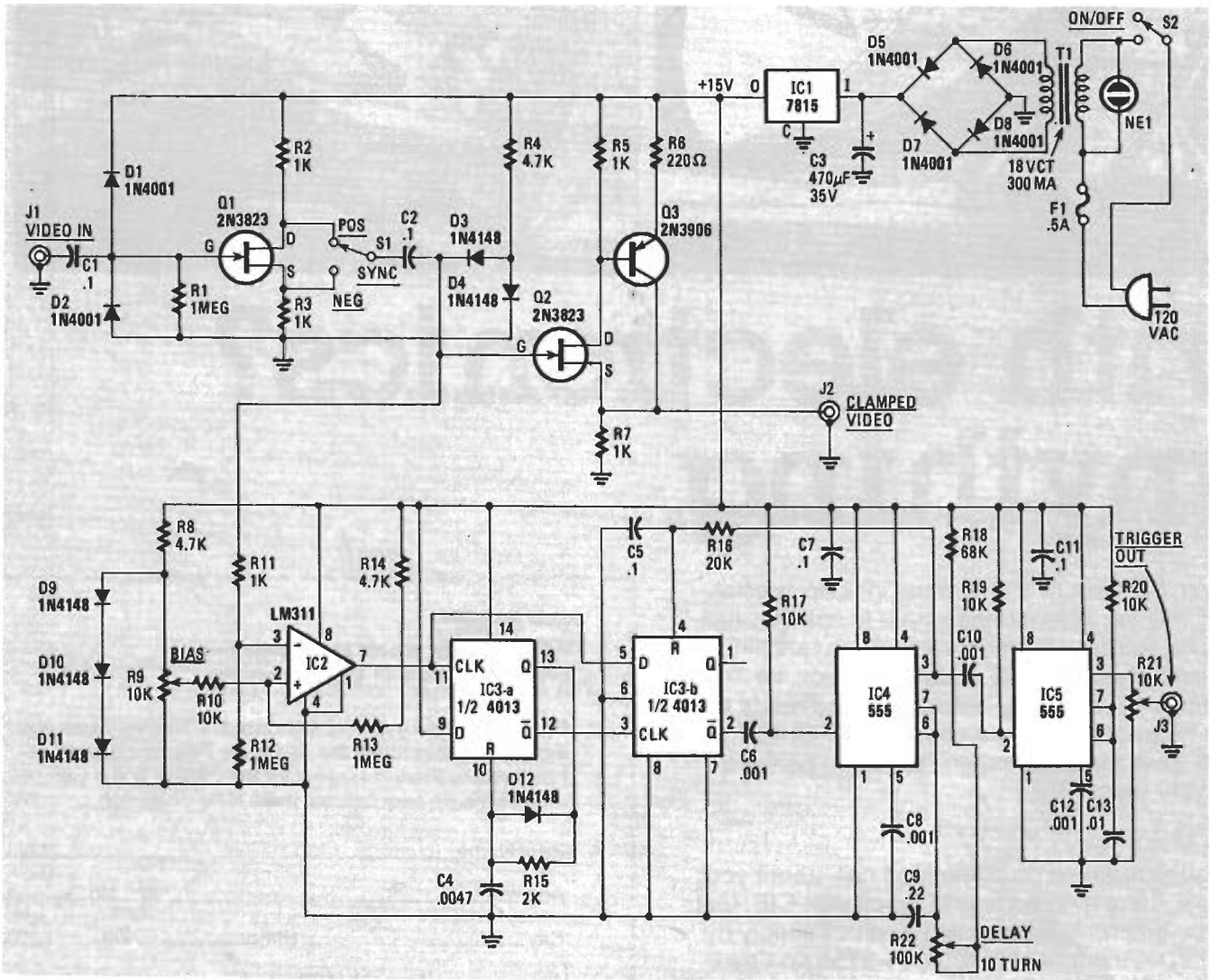


FIG. 2—SCHEMATIC OF THE SYNC SEPARATOR. The "heart" of the circuit is made up of IC2–IC5. The composite-sync output of IC2 is fed to IC3, a dual flip-flop, which outputs vertical-sync pulses. Those pulses are then delayed by IC4 and sent to IC5, which is configured as a one-shot. The output pulse of IC5, which is 100 microseconds, is sent to the scope's trigger circuit.

The C2-R12 time constant is quite long (1 second) with respect to one horizontal time period. Because of that, the bias voltage remains essentially constant for the full period of the line. The effect of the bias is to force all of the sync pulse-tips to line up at the same level. Resistor R4 and diode D4 provide a +0.6-volt reference level for D3, which prevents the clamped signal from going below ground potential.

Transistor Q2 and Q3 form a wideband high-input-impedance buffer/amplifier that couples the clamped video output to the oscilloscope's vertical-input channel.

As we go through the discussion of the rest of the circuit, you'll find it helpful to study the timing diagrams of Figs. 3 and 4.

IC2 is a straightforward differential comparator that separates the sync pulses from the video information. The bias voltage on pin 2, the non-inverting input of IC2, is set by trimmer potentiometer R9. With the bias voltage properly set, the output (pin 7) will switch or change state only during the sync-pulse time, effectively stripping off the video and leaving only composite-sync signals, as shown in Fig. 3.

From IC2, the composite sync goes to IC3-a and IC3-b, both halves of a dual D-type CMOS flip-flop. That circuit separates the vertical-sync pulses from the horizontal by detecting the duty cycle change that occurs during the vertical-sync pulse time. Since IC2 is set up as an inverting comparator, the composite-sync pulses at its output are now positive-going. The rising edge of each horizontal-sync pulse clocks the input (pin 11) of IC3-a. Since the D input is tied to a high logic-level, those rising edges clock a high level into the Q output and a low logic-level into the $\overline{Q}$ output. When the Q output goes high, capacitor C4 begins charging up through R15. Diode D12 is reverse biased at this time and has no effect.

After about 10 microseconds, the voltage across C4, and thus the voltage at pin 10 (RESET) will be high enough to reset the flip-flop, forcing the Q output low again. That allows C4 to discharge rapidly through D12, bringing the sequence to an end. The result is that IC3-a is actually a one-shot with a period of approximately 10 microseconds—about twice as long as a standard horizontal-sync pulse.

The $\overline{Q}$ output of IC3-a drives the CLOCK input of IC3-b. That means that the rising edge seen at the CLOCK input corresponds to the end of the 10-microsecond time period. Note that the D input of IC3-b is not tied high. Instead, it is connected to the composite-sync output of IC2. As a result, whenever IC3-a is triggered by the horizontal-sync pulses, the D input of IC3-b will be low when the rising edge occurs at its clock input. Since the D input of IC3-b is low when the clock pulse occurs, no change takes place at the $\overline{Q}$ output.

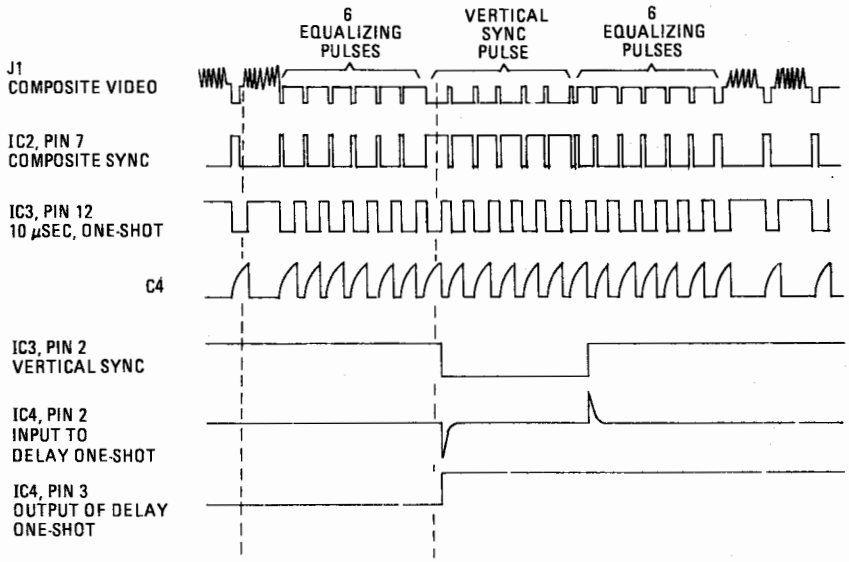


FIG. 3—THIS TIMING DIAGRAM shows how signals at various parts of the circuit are related. It should help you to follow the schematic and understand the operation of the circuit.

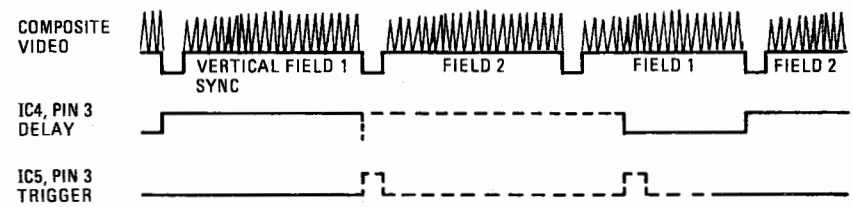


FIG. 4—TIMING DIAGRAM shows the relationship of vertical pulses to the delay and trigger output. The dotted lines indicated the range of delay that is available.

The duty cycle of a vertical-sync pulse is much wider than that of the horizontal pulses. Therefore, when a vertical-sync pulse triggers IC3-a, the D input of IC3-b will still be high at the end of the 10-microsecond period. Since the D input is at a high logic-level when the clock pulse occurs, $\overline{Q}$ of IC3b will go low. The $\overline{Q}$ output will stay low as long as the duty cycle seen at the D input is longer than that of a horizontal-sync pulse.

So, at the $\overline{Q}$ output of IC3-b we will see a negative-going pulse that corresponds to vertical sync. The falling edge of that pulse is differentiated by C6 and R17 and is used to trigger the delay one-shot, IC4. With the DELAY potentiometer R22 at minimum resistance, IC4 has a time period of 16.5 milliseconds—just about the same length of time as one complete field. With R22 at maximum resistance, the time period is 40 milliseconds, which is equivalent to approximately 2½ fields.

At the end of IC4's time period, wherever it might be set, the output at pin 3 goes low. This edge is differentiated by C10 and R19 and used to trigger the last one-shot; IC5. The period of that monostable is fixed at 100 microseconds. The pulse is routed to J3 and used to trigger the EXTERNAL TRIGGER input of the oscilloscope.

Resistor R16 and capacitor C5 help reduce jitter on long delays. A slightly delayed version of the DELAY one-shot's output is applied to the RESET input (pin 4) of IC3-b. That guarantees that no spurious pulses will appear at its output until well after the delay period.

A minimum time delay of 16.5 milliseconds is used to ensure that the scope is not triggered on consecutive fields. If that were allowed to happen, the display would show the even and odd fields superimposed on one another.

Building the sync separator

The sync separator/trigger delay can be built as a free-standing, self-contained unit. Of course, you also have the option of installing the circuit inside an oscilloscope. The layout of the circuit is not critical, and if you're careful, you can build it on perforated construction board and use point-to-point wiring. Using a printed-circuit board is a better way to go, however. A foil pattern for a single-sided board is shown in Fig. 5. (See the Parts List for information on availability of a pre-etched and drilled board.)

Figure 6 shows a parts-placement diagram, including both on-board and off-board components. Figure 7 shows a photograph of the author's prototype that can be used as a guide. As indicated in the parts-placement diagram, be sure to con-

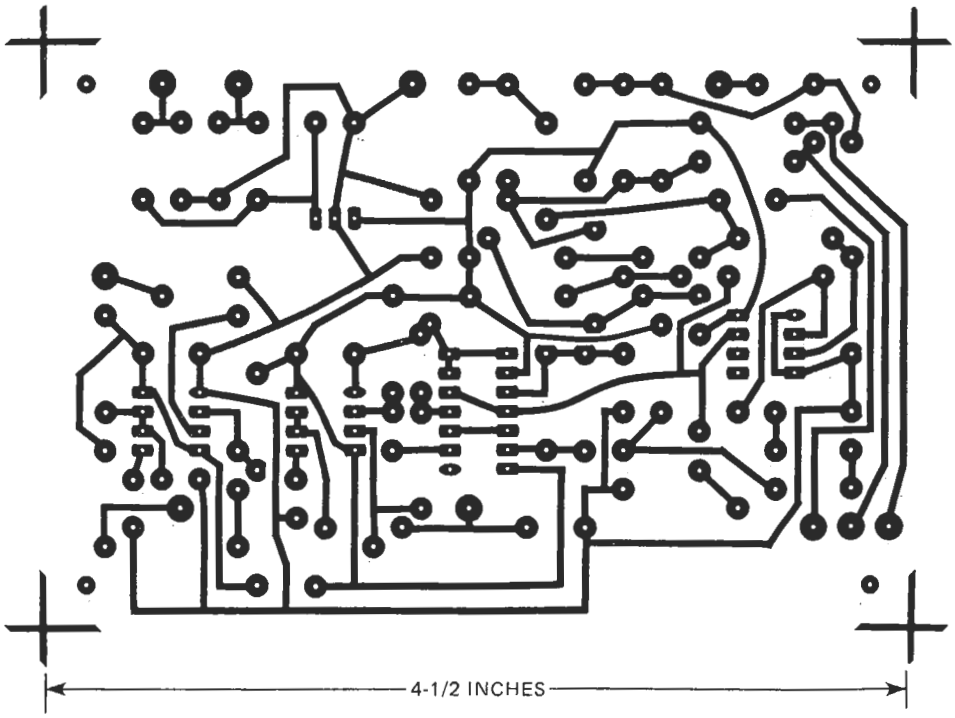


FIG. 5—THE SINGLE-SIDED BOARD is small enough to fit inside many oscilloscopes.

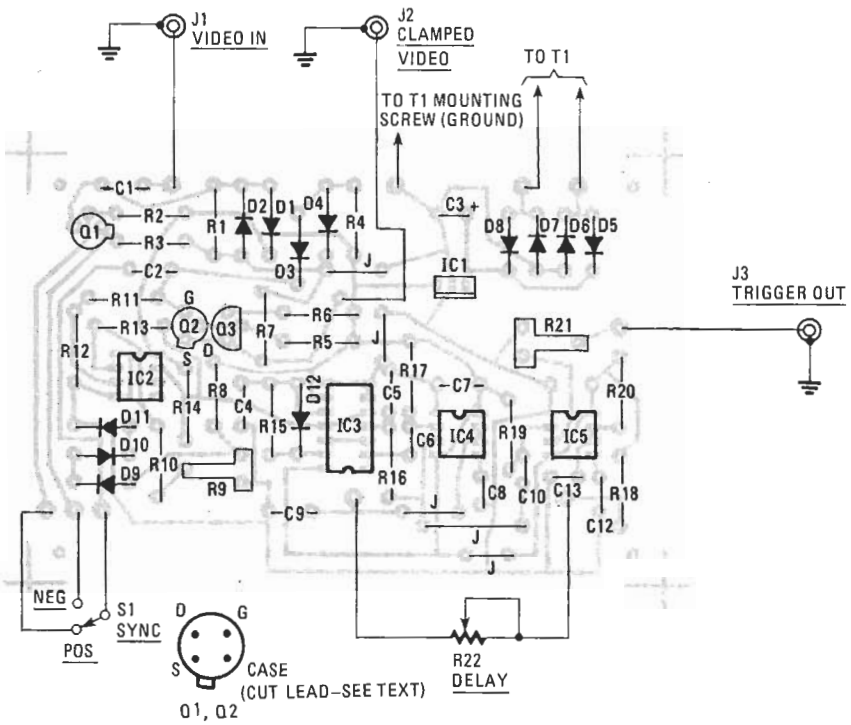


FIG. 6—PARTS PLACEMENT DIAGRAM. Note that before you install Q1 or Q2, you should cut the case lead. Also note that the board's ground should be connected to a transformer mounting screw.

Resistors, ¼-watt, 5% unless otherwise noted
R1, R12, R13—1 megohm
R2, R3, R5, R7, R11—1000 ohms
R4, R8, R14—4700 ohms
R6—220 ohms
R9, R21—10,000 ohms, trimmer potentiometer
R10, R17, R19, R20—10,000 ohms
R15—2000 ohms
R16—20,000 ohms
R22—100,000 ohms, ten-turn potentiometer

Capacitors
C1, C2, C7, C11—0.1 μF, ceramic disc
C3—470 μF, 35 volts, electrolytic
C4—0.0047 μF, 10%, polyester film
C5—0.1 μF, 10%, polyester film
C6, C8, C10, C12—0.001 μF, 10%, polyester film
C9—0.22 μF, 10%, polyester film
C13—0.01 μF, 10%, polyester film

Semiconductors
IC1—7815 15-volt regulator
IC2—LM311 comparator
IC3—4013 dual D-type flip-flop
IC4, IC5—555 timer
Q1, Q2—2N3823
Q3—2N3906
D1, D2, D5–D8—1N4001
D3, D4, D9–D12—1N4148

Other components
F1—fuse, ½ amp
J1–J3—Female BNC jack
NE1—neon lamp, 110 volts
S1—SPDT toggle switch
S2—SPST toggle switch
T1—110:18 volts AC, 300 mA
Miscellaneous: fuse holder, line cord, printed-circuit board, ground lug, case, etc.

The following are available from Elephant Electronics, Box 41770-P, Phoenix, AZ 85080: A complete kit (DT-1) consisting of all items listed above, $49.95. The printed-circuit board is available separately for $12.95. Arizona residents must include 6% sales tax.

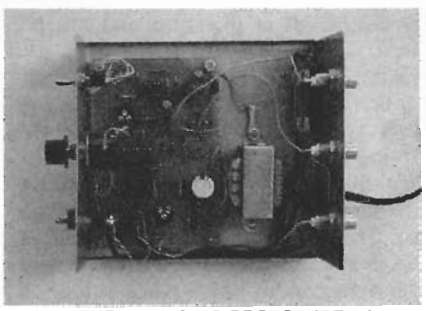


FIG. 7—THE AUTHOR'S PROTOTYPE, shown here with its top removed, was built as a stand-alone unit. If you want to use a smaller box, you might consider using a wall-mount transformer.

nect a wire from the board's ground to one of the transformer's mounting screws. Don't forget to install the 5 jumper wires on the PC board.

Be careful when installing IC3. It is a CMOS type and is therefore static-sensitive. Note that it's also oriented opposite to that of all the others.

The case lead of transistors Q1 and Q2 should be cut off prior to their installation. The proper lead is pointed out in the parts-placement diagram.

Checkout and setup

After the unit is assembled, apply power and check the power-supply voltage. If that's correct, proceed by connecting a source of video to the input. An ideal source is the video output of a VCR. If you don't have a VCR or other video source available, then the output of your TV's video detector will do nicely. Determine whether the sync pulses are positive- or negative-going and set the SYNC switch accordingly. Connect the CLAMPED VIDEO output of the project to the vertical input of the oscilloscope. You

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