Store & Record Non-repetitive Analog Signals

Analog/Digital Storage CRO Adapter

Here we describe additional circuitry to the Digital Storage CRO Adapter, of the November 1980 issue, which enables analog signals of up to 100kHz to be stored. The conversion allows the unit to operate in either Analog or Digital storage format. The extra controls and Printed Circuit Board required are designed to be easily accommodated within the existing case. Also featured is a revised PC board for the November Digital Storage CRO Adapter.

by JOHN CLARKE

In the November 1980 issue, we presented an article on a Digital Storage Adapter and in this we mentioned the advantages of digital storage over the methods used in conventional storage oscilloscopes. The device was capable of storing digital signals, with two channels available. The first channel had tracer or marker pulses to enable the period of the waveform to be measured.

Similarly the Digital/Analog Storage CRO Adapter in displaying of analog signals on an oscilloscope, incorporates a tracer, however, only one channel is available. The majority of the circuitry from the Digital Storage CRO Adapter is utilised with the extra circuitry to produce a complete circuit for analog signal storage. Reversion to the digital storage mode is achieved at the flick of a switch.

Processing of the analog signal for storage in a digital memory is implemented with 8-bit Analog-to-Digital (A-D) conversion techniques. Here the analog signal is converted to a binary representation of discrete analog levels. With 8-bits there are two to the power eight or 256 discrete levels to represent the analog voltage levels. For example 00000000 represents a zero voltage level, 10000000, half full scale, and 11111111, full scale.

To retrieve the stored digital signal, Digital to Analog (D-A) conversion reverses the process. The most common D-A method being to use an R/2R weighted ladder network. This is easy to implement in either discrete or IC form. The IC package has refinements over the R/2R ladder network, having current switches and a reference amplifier. The IC has the extra advantage of lower capacitance and consequently a faster settling time over a discrete R/2R ladder.

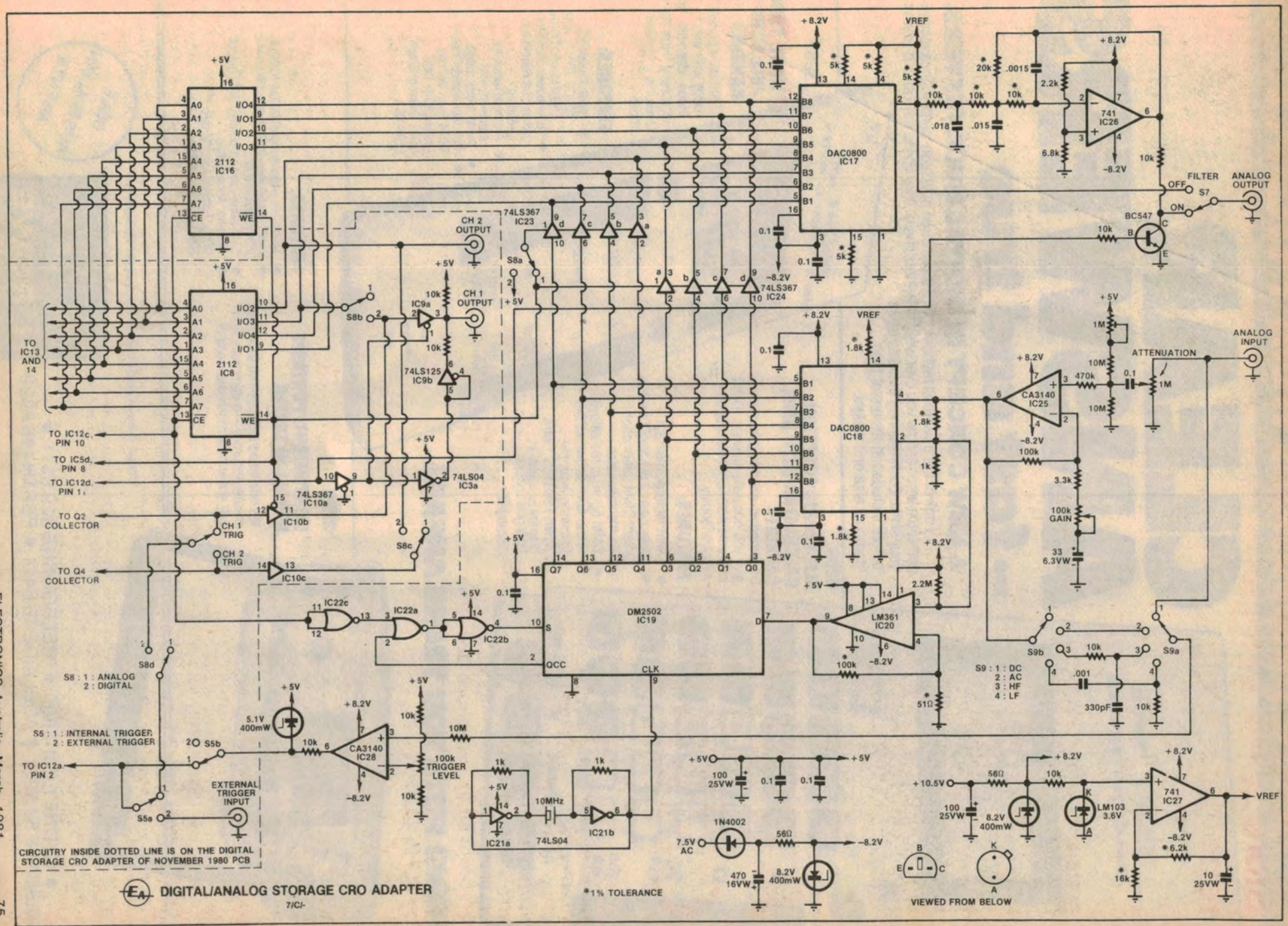
There are several ways in which A-D conversion can be done and usually involve a comparator which compares the incoming signal with the analog signal derived from an A-D and D-A converter operation.

The error signal resulting from this comparison informs the A-D converter of what steps need to be taken to reduce the error.

In the case of an "up counter A-D converter", the counter starts at zero and counts up in binary until the comparator changes state and stops the counter. This method can be slow since the maximum time to reach the correct conversion could be 256 counts for an 8-bit converter. Consequently continuous "up/down counters" are used in preference to the up counter since gradually changing signals (a sine wave) will need only a small up or down count correction to the bit pattern. However, in adverse conditions such as converting a square wave, the maximum count of 256 is still required.

A much faster method which converts in almost as many clock cycles as the

At right is the complete circuit diagram of the Analog Storage section.



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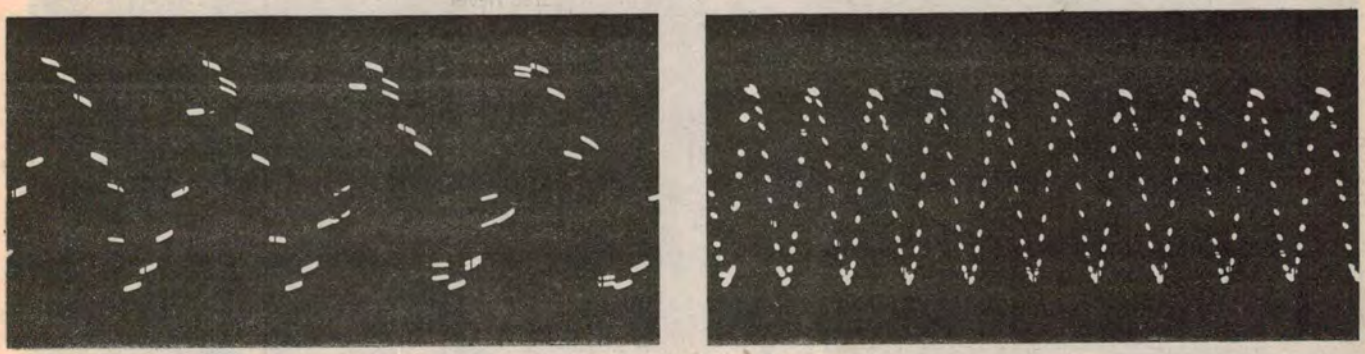
number of bits, is with the Successive Approximation Register or SAR. This method involves some clever logic and begins conversion by setting high, the most signifigant bit (bit 8) and the rest of the bits low. This is the mid-way voltage point (2.5 volts for a 5 volt converter).

If the input signal is higher than the A-D, D-A conversion, then the comparator signals the SAR to keep the most significant bit (bit 8) high and to then continue the conversion. However, if the signal is lower than the A-D, D-A conversion, then the comparator signals the SAR to bring the most significant bit low again and continue the conversion. So already the SAR has determined whether the incoming signal is higher or lower than the midway voltage in only one clock cycle. The next step is to set the next significant bit (bit 7) high and to test for a higher or lower voltage than the A-D, D-A conversion.

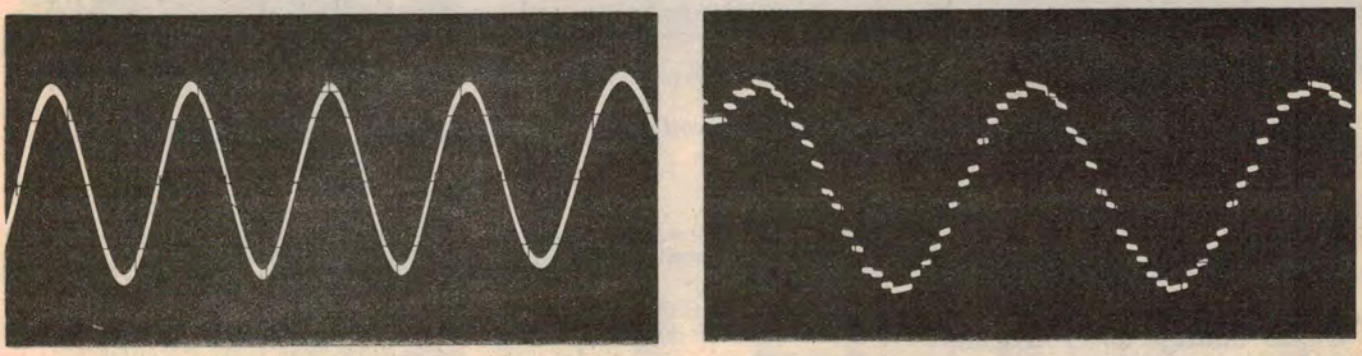
The SAR continues with this successive approximation comparison until the last bit (bit 1) is compared. As can be seen, the digital conversion takes only eight cycles plus the setting up time of the SAR.

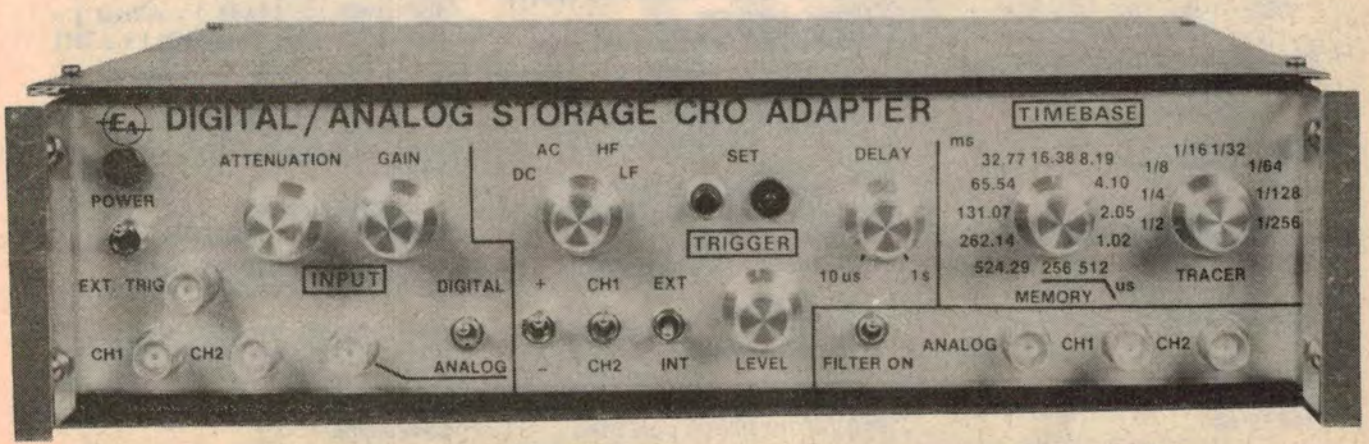
Generally, during digital conversion of an analog signal, the sampled signal should remain within ± a Least Significant Bit, LSB, to avoid errors in conversion. For a 0-5V, 8-bit converter, the incoming signal needs to remain within 5/256=19.5mV during the conversion time. With a 0.9us conversion time (which is the conversion time of our A-D converter) this represents a maximum incoming signal slew rate of 21.7mV/us, corresponding to 1kHz for a triangular waveform and about 700Hz for a sine wave.

As can be expected, at higher slew rates (higher frequencies) the resolution of the A-D conversion becomes less. For example, 7-bit resolution occurs with a triangular 2kHz waveform, and 4-bit resolution at 16kHz. To get around this problem a Sample and Hold, S and H, circuit is generally used which holds the

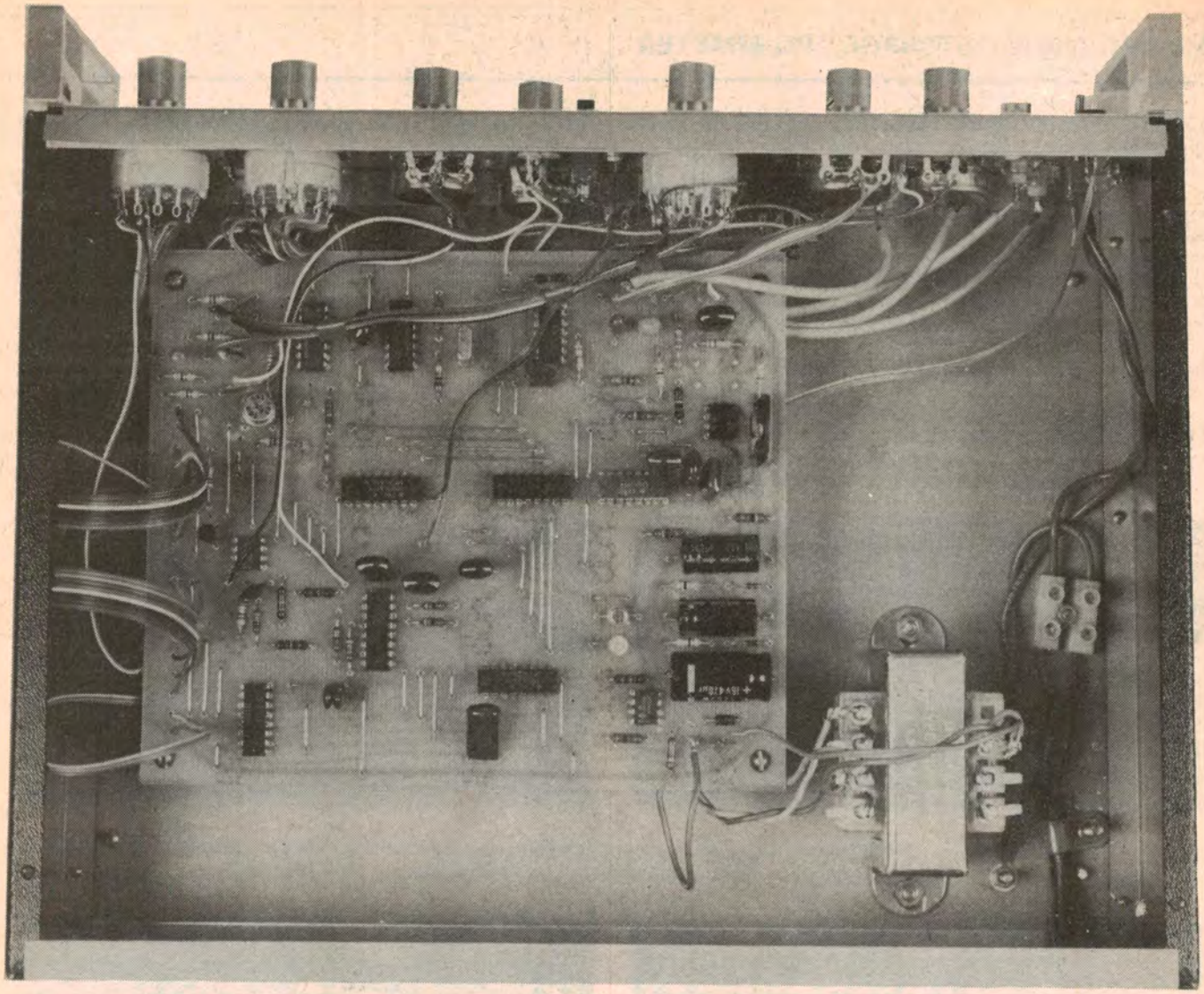


The above photograph shows a 100kHz sinewave, captured in memory and displayed without low pass filtering. Below left is the same waveform after filtering. At top right is a 20kHz and below right a 1kHz sinewave, both unfiltered.





Complicated to behold, the Adapter is relatively straightforward to use and much cheaper than a Storage Oscilloscope.



Not visible in this photograph is the Digital Storage PC board which is stacked below the Analog PC board.

PARTS LIST:

NB: These parts are in addition to those listed for the Digital Storage CRO Adapter in November 1980.

1 Printed Circuit Board 141 × 174mm coded 81dc3a.
1 Scotchcal panel
4 knobs
2 BNC panel sockets
1 DPDT switch
1 4PDT switch
1 2-pole, 4 position rotary switch
1 10MHz crystal

SEMICONDUCTORS
1 1N4002 100PIV rectifier diode
1 5.1 volt 400mW zener diode, 1N751 etc
2 8.2 volt 400mW zener diodes, 1N756 etc
1 LM103 3.6 volt voltage reference or 3.6 volt 400mW zener diode 1N747 (See text)
1 BC547 NPN transistor
2 DAC0800 8-bit digital to analog converters
1 DM2502 8-bit successive approximation register
1 LM361 high speed comparator
2 CA3140 FET input operational amplifiers
2 741 operational amplifiers
1 2112 256 × 4 static RAM, 450ns access time

LOW POWER SCHOTTKY TTL
1 74LS02 quad two input NOR gates
1 74LS04 hex inverter
2 74LS367, Tri-state hex buffers

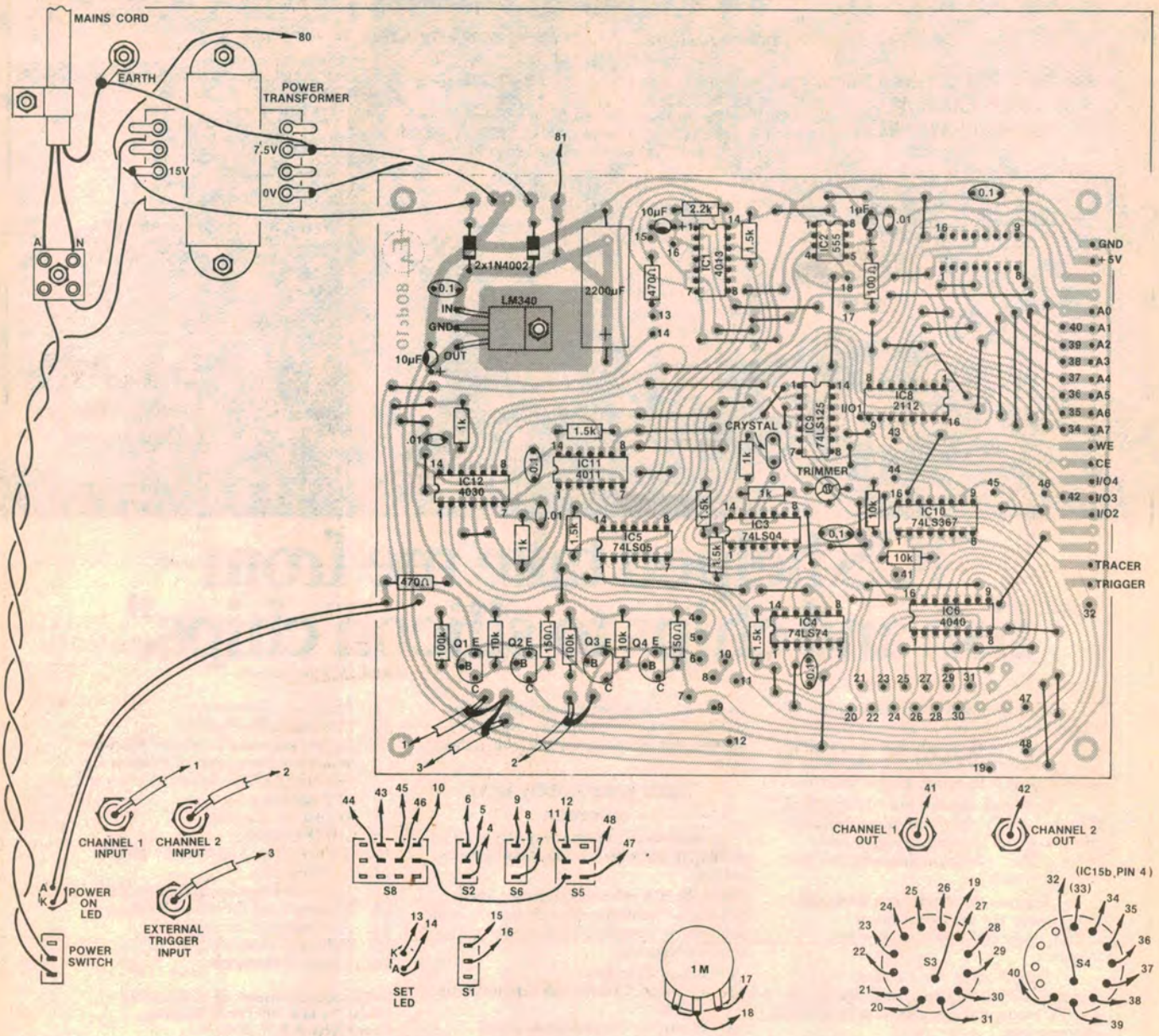
CAPACITORS
1 470uF/16VW pigtail electrolytic
2 100uF/25VW pigtail electrolytic
1 33uF/6.3VW tantalum electrolytic
1 10uF/25VW PC electrolytic
10 0.1uF metallised polyester
1 .018uF metallised polyester
1 .015uF metallised polyester
1 .0015umetallised polyester
1 .001uF metallised polyester
1 330pF disc ceramic

RESISTORS (¼W, 5%)
3 × 10MΩ, 1 × 2.2MΩ, 1 × 470kΩ, 1 × 100kΩ, 8 x 10kΩ, 1 x 6.8kΩ, 1 x 3.3kΩ, 1 x 2.2kΩ, 3 x 1kΩ, 2 x 56Ω.

RESISTOR (¼W, 1%)
1 × 100kΩ, 1 × 20kΩ, 1 × 16kΩ, 3 × 10kΩ, 1 x 6.2kΩ, 4 x 5kΩ, 3 x 1.8kΩ, 1 x 51Ω.

POTENTIOMETERS
1 × 1MΩ large vertical trimpot
1 x 1MΩ linear potentiometer
2 x 100kΩ linear potentiometer

NOTE: Ratings are those used on the prototype. Components with higher ratings may generally be used providing they are physically compatable.



This diagram shows the connections and changes necessary to the original PC board published in November 1980 for wiring to the Analog PC board. The Veroboard additions published in January 1981 should be added to this.

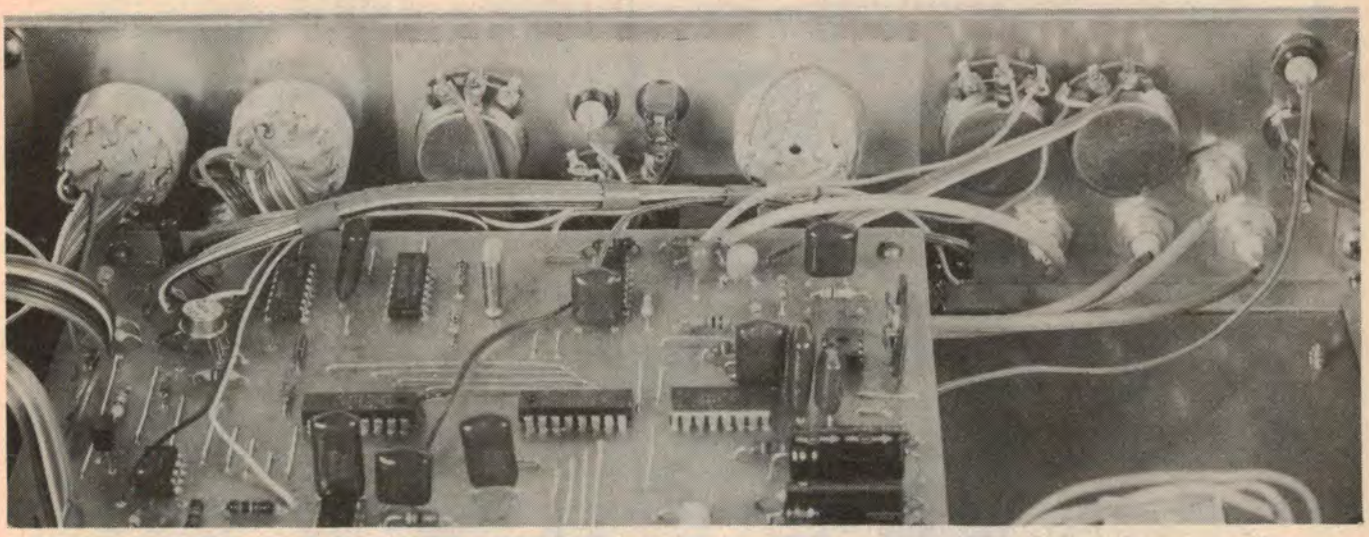
analog signal steady during the conversion time. This method is only relevant, however, if the S and H acquisition time is faster than the conversion time of the A-D converter. No common S and H circuits are faster than the 0.9us of our A-D converter.

A problem associated with the stored A-D conversion of a signal and replayed D-A signal, as is with any sampling methods, is that if the sampling frequency is not at least twice the sampled analog signal, strange results can occur. For example, with a 100kHz signal sampled into memory at 50kHz (½ the sampled frequency) the replayed signal will appear as a 25kHz signal. A solution to this is to provide a very sharp cut-off filter at the input to the D-A converter, to prevent higher frequency signals entering the converter. This will need to have various cut-off frequencies depending upon the sampling rate. Due to the large number of filters required, we did not provide for this "Anti-Aliasing" feature.

Refer now to the circuit, the description of which should be read in conjunction with the Digital Storage CRO Adapter circuit description in the November 1980 issue. We used an 8-bit SAR and two D-A converters in IC form. The D-A converter, IC18, in conjunction with the SAR, IC19 and the high speed comparator, IC20, form the A-D converter. With a clock provided by a 10MHz crystal and two inverters, IC21a and IC21b, the A-D conversion time is nine clock cycles or 0.9us.

The 8-bit memory to store the A-D conversion is comprised of both the 4-bit memories of IC16 and IC8, the latter being located on the Digital Storage CRO Adapter PC board. The memory is loaded with data from the SAR via Tri-state buffers, IC23 and IC24. At the beginning of storing a signal in memory, the memory address counter is at zero count. During the loading of each memory location, the SAR is stopped by gate IC22a when memory ICs are enabled and the SAR conversion complete signal is true.

At every memory location, the SAR



This photo shows details of the front panel wiring.

SPECIFICATIONS

INPUT/OUTPUT: — one channel with 2kHz low pass filter and tracer

SENSITIVITY: — 160mVp-p for 0-5 volt conversion (up to 20kHz only, see text)

INPUT IMPEDANCE: — 1 Megohm

TRIGGERING: — Positive and negative edge triggering. AC/DC/HF rej/LF rej

TRIGGERING LEVEL: — adjustable from 4.5 volts to 0.5 volts

MINIMUM RESOLVABLE FREQUENCY: — 1.9Hz for a timebase setting of 524.29ms

MAXIMUM RESOLVABLE FREQUENCY: 8-bit resolution; 700Hz sine wave; 1kHz triangular wave; 7-bit resolution; 1.4kHz sine wave; 2kHz triangular wave; 2-bit resolution; 42.8kHz sine wave; 64kHz triangular wave

NOTE: These specifications refer to the Analog storage mode only.

converts to the new digital code representing the incoming analog signal at that point in time. When loading is complete, signalled by the ripple carry of IC14, the 256 × 8-bit locations are filled and the Tri-state buffers go into their Tri-State or high impedance state.

After the digitally represented signal has been stored in memory, the memory is in the read state and with the D-A with the address counter continuously and sequentially cycling through the addresses of the memory, a repeating waveform is presented at the output of the D-A converter.

It should be noted that the SAR and the memory address counter for the memory operate on different clocks. The memory address counter clock operates from the oscillator located on the Digital Storage CRO Adapter PC board and has a maximum clock rate to the memory address counters IC13 and IC14, of 2MHZ. The clock for the SAR will therefore allow for complete A-D conversion between successive memory locations provided the memory address counter clock is not set to greater than 1MHz.

The analog output from the D-A converter, IC17, is switchable to a filter with S7. The filter is a third-order low-pass and has a cut-off frequency of about 2kHz. By adjusting the memory timebase of the stored waveform, an optimal setting will be found for filtering. Since this timebase is adjusted after storage, a tracer is provided to enable the measurement of the waveform period. The tracer pulses generated from IC12d are taken to the base of the BC547 at the output of the filter. Consequently the filtered output signal is brought to ground on every tracer pulse.

Note that the operational amplifier, IC26, at the heart of the filter, is biased higher than the ground point with the 2.2kΩ and 6.8kΩ at pin 3 to keep the output signal well above ground making the tracer more distinctive.

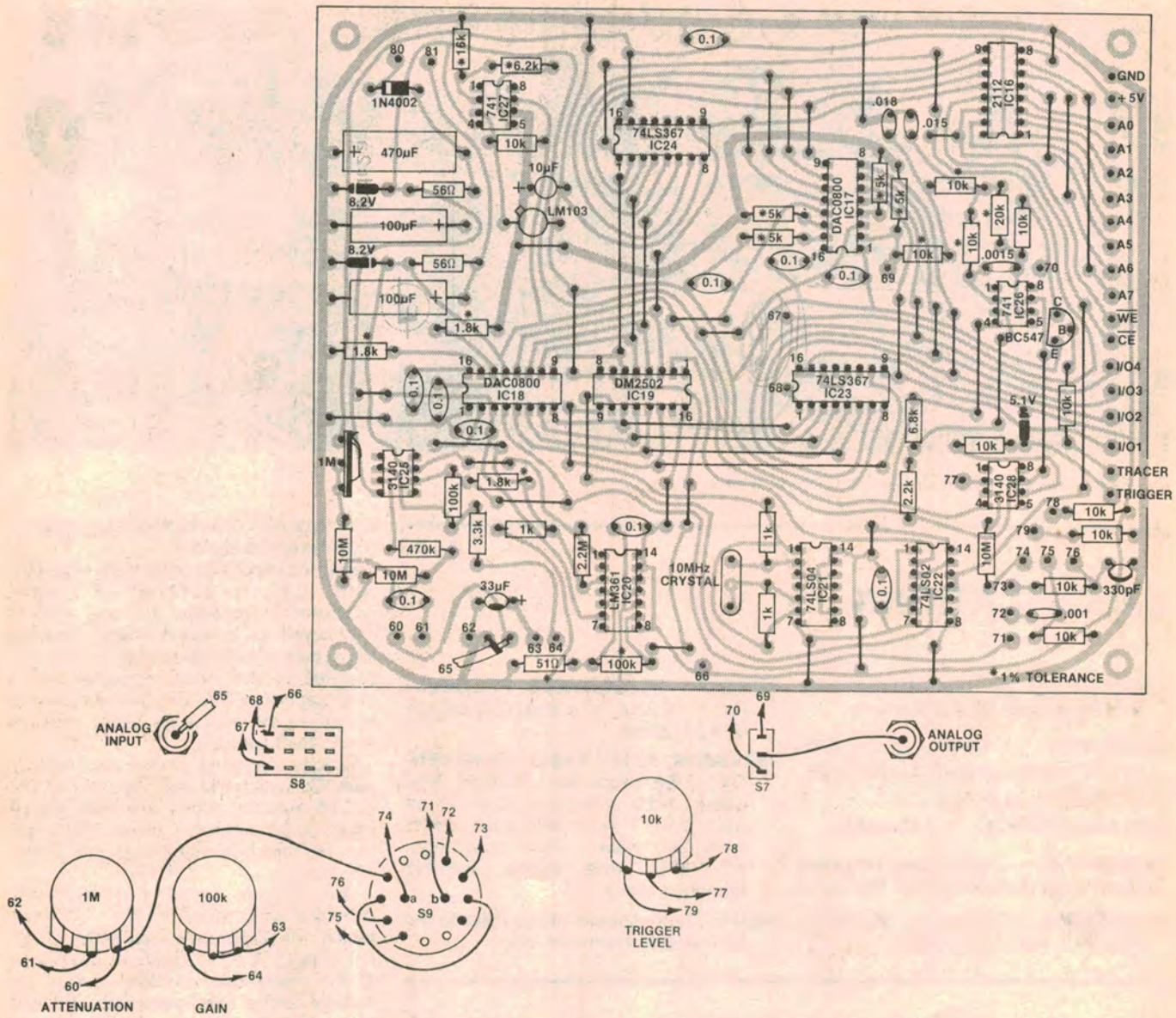
Input to the A-D converter is provided with IC25, a CA3140 FET input operational amplifier. This op amp is connected as a non-inverting amplifier for a high input impedance and is AC-coupled to the incoming signal with a 0.1uf capacitor. The amplifier is biased to about −1.5V with two 10MΩ resistors and a 1MΩ trimpot.

Various triggering modes are available with the switch S9a and S9b: that of DC, AC, HF rejection and LF rejection. The HF rejection filter cuts off above 50kHz and the LF rejection filter cuts off below 1.5kHz.

The trigger level potentiometer provides adjustment for the voltage at which the operational amplifier, IC28, will trigger. A zener diode at the output of the operational amplifier clamps the voltage swing from zero volts to +5.6 volts, suitable for the trigger input of IC12a.

The power supply for this analog storage circuit is derived from the digital storage PCB. The +10.5 volts is filtered with a 100uF capacitor and regulated with an 8.2 volt zener diode. This +8.2 volts supplies the positive voltage for the operational amplifiers, comparator and D-A converters. The +8.2 volts is further regulated with a 3.6 volt zener (LM103) and buffered with an operational amplifier, IC27. This provides a 5 volt reference for the D-A converters.

The LM103 reference diode is a two-terminal IC device similar to a zener diode. The breakdown characteristic is very sharp and the dynamic impedance very low. If this diode is unavailable, a standard 3.6 volt zener diode can be used with little detrimental effect to the circuit performance, in which case a 270Ω resistor will need to replace the 10kΩ dropping resistor.



This diagram shows the connections and component layout of the Analog conversion PC board.

The 5 volt supply from the digital storage PCB is filtered with a 100uF capacitor and several 0.1uF capacitors. The negative voltage for the operational amplifiers, comparator and D-A converters is obtained by half-wave rectifying the AC voltage directly from the transformer. This is regulated with a zener diode, to give −8.2 volts.

As can be seen in the circuit diagram, switching is organised to allow for digital or analog signal storage. The switches in question are S8 and S5. S5 was used in the Digital Storage Adapter to enable internal or external triggering, but in this case an extra pole is used to allow internal and external triggering for both the digital and analog inputs. S8d allows internal triggering for either analog or digital inputs.

Switches S8b and S8c disconnect the output memory data lines of IC8 from the Tri-state buffers IC10b and IC10c when in the analog storage mode and S8a keeps the Tri-state buffers of IC24 in Tri-state when in the digital storage mode. This prevents conflicts between the Tri-state buffers when in the digital or analog modes.

As mentioned previously, the circuitry for the Analog storage facility is contained within the Digital Storage CRO Adapter case, as featured in November 1980. New front panel artwork has been produced to provide for the extra controls. The Analog storage circuit is accommodated on a PC board coded 81dc3a measuring 141 × 174mm. This is the same size as the Digital Storage PC board and is stacked on it.

As mentioned in the addendum to the Digital Storage CRO Adapter in the January issue, a revised PC board pattern has been produced, coded 81dc3b and measuring 141 × 174mm.

If this new PC board is used, then the following applies. Solder all the components to the PC board in a similar manner to that described in the November issue. Note the wiring changes to the switch, S4, from the original PC board overlay.

An overlay and wiring diagram have been provided for the analog circuitry PC board, 81dc3a, and two overlay diagrams for the Digital Storage CRO Adapter: one for wiring the original 80dc10 PC board of the November issue to the 81dc3a PC board and the other for wiring the revised 81dc3b PC board. Another overlay features the 81dc3b PC

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board for when the analog PC board, 81dc3a, is not required.

Note that when the Digital PC board of either 80dc10 or 81dc3b is used in conjunction with the Analog PC board 81dc3a, an extra link near the regulator bringing out the 10.5 volts and the replacement of three links with switches, differentiates them from the overlay diagrams when the Analog PC board, 81dc3a, is not required.

Start construction by placing the links on the PC board and soldering them in place. Use the overlay to help you in construction.

Next the diodes and resistors can be soldered into place, followed by the ICs. Note the orientation of the ICs on the overlay before soldering in place since errors can be disastrous. Finally the capacitors, transistor, trimpot and crystal can be soldered in place.

Assuming the Digital Storage CRO Adapter has already been built as described in the November issue, the front panel Scotchcal artwork should be removed from the front panel after removing all the switches, input sockets, potentiometer and LED bezels. The new Digital/Analog Storage CRO Adapter Scotchcal artwork can now be placed on the front panel and the holes drilled using the artwork as a guide.

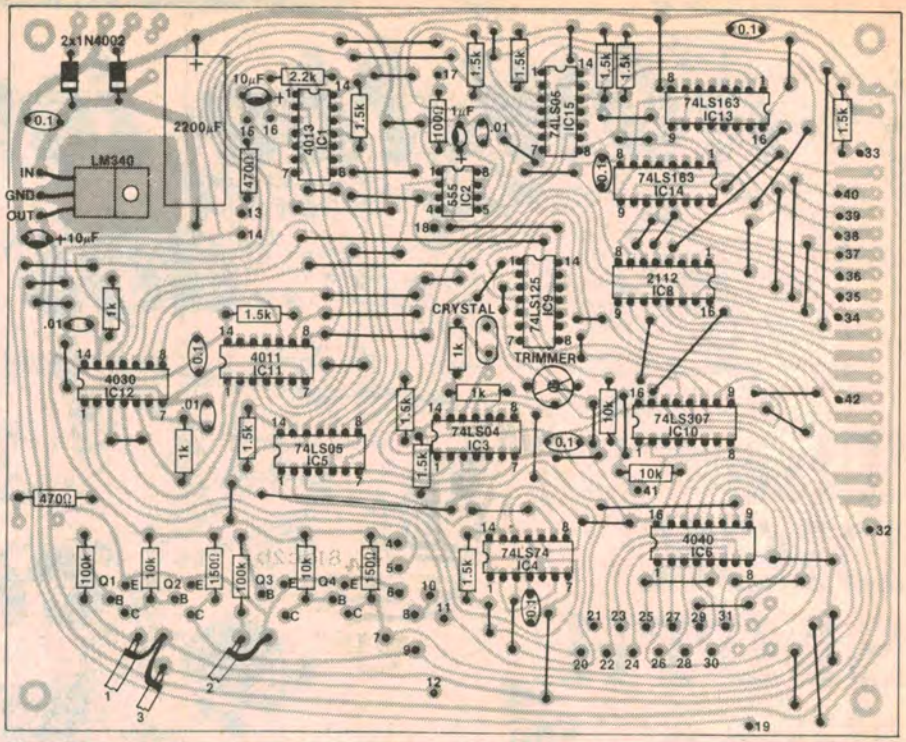
The input sockets, switches, potentiometers and LED bezels can now be secured to the front panel. Note that the single pole switch used for the internal/external triggering selection, S5, is replaced with a double pole type. The orginal switch can be used in the filter on/off position S7.

We used 13mm long tapped brass standoffs to support the lower PC board, containing the digital storage circuitry and untapped 18mm long brass standoffs between the lower and upper PC board containing the analog circuitry. This method of PC board support allows the lower spacers to be secured to the base of the case with short screws and the upper PC board held with longer screws extending down from the upper PC board through the untapped spacers to the lower tapped spacers.

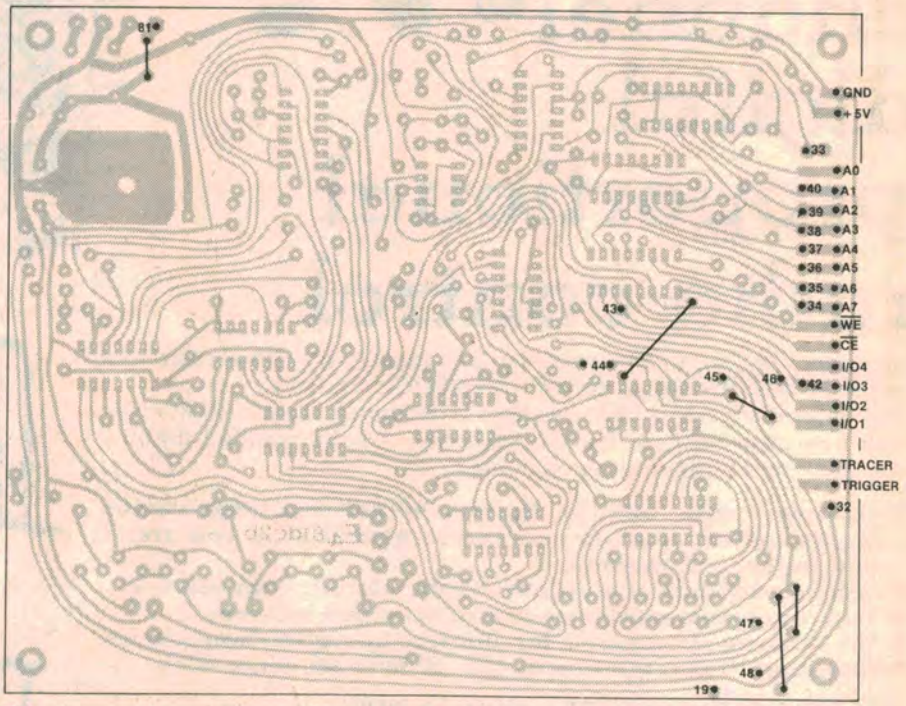
We estimate that the cost of parts for this project is approximately

$80

This is additional to the parts for the Digital Storage CRO Adapter described in November 1980.



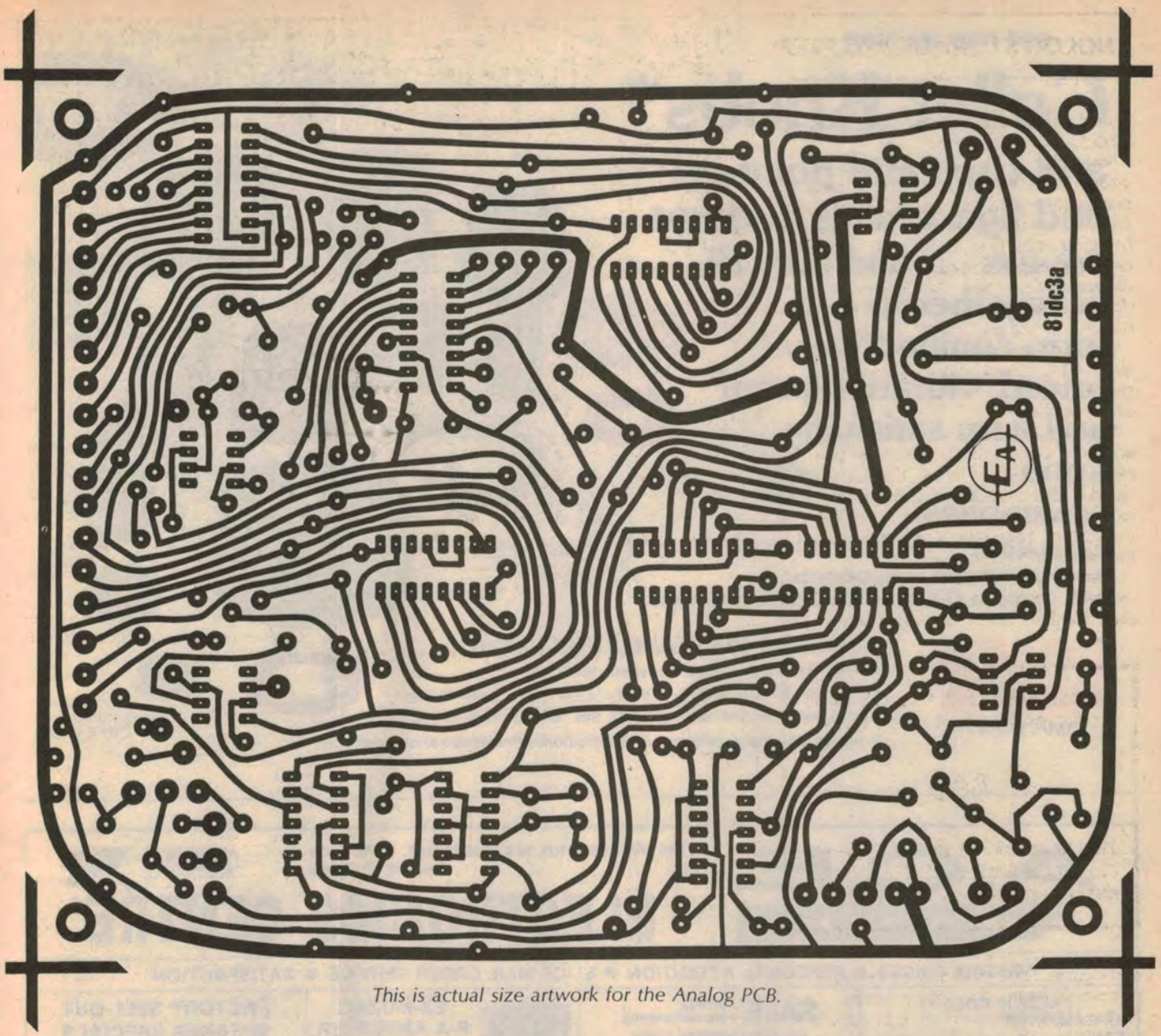
This diagram shows the component layout for the modified digital storage PCB, encompassing the modifications published in the January 1981 issue.



This diagram shows the mods necessary to the PCB above to connect it to the analog PCB. Refer also to the diagram on page 80.

Wiring of the PC boards should be accomplished by wiring the lower digital PC board first. All the relevant wires to the controls on the front panel can be run with consideration for the fact that another PC board is being stacked on top. In other words leave enough slack in the wiring. The interboard wiring such as GND, +5V, the address lines A0 to A7, WE, CE, and the data lines I/01 to I/04 plus the tracer and trigger interconnections can be soldered to the lower PC board with ribbon cable in preparation for wiring these to the upper PC board.

With the lower PC board wiring complete, the interconnecting wiring can be connected to the upper Analog PC board, 81dc3a. The wiring to the controls can also be made at this stage.

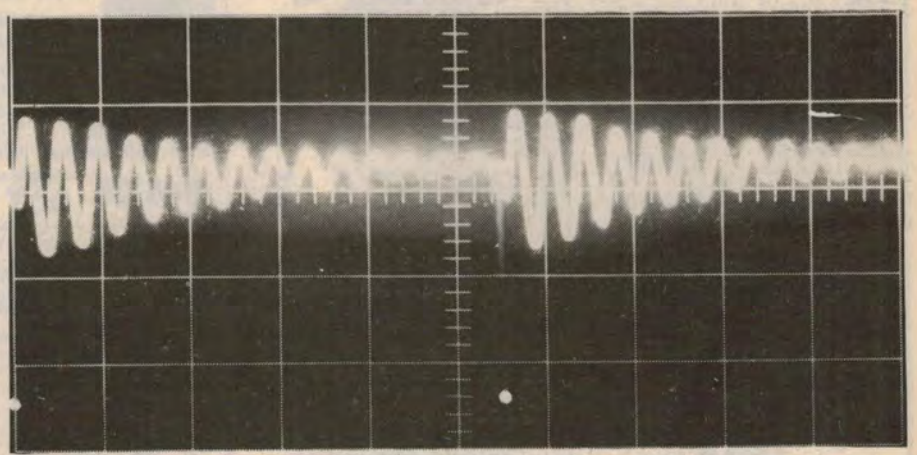


This is actual size artwork for the Analog PCB.

That completes the wiring. Setting up the analog circuitry involves adjusting the 1MΩ trimpot until the output of the op amp IC25, with no input signal connected, has an output DC voltage equal to half the reference voltage. This is done by measuring the reference voltage from pin 6 of IC27 with a voltmeter or oscilloscope and adjusting the 1MΩ trim pot until pin 6 of IC25 is set to half the voltage reference.

The adjustment is necessary to allow the incoming signal to be symmetrical about the centre of the reference voltage allowing maximum signal levels to be converted before clipping occurs. Note that the two 10MΩ resistors may require swapping around to achieve the adjustment.

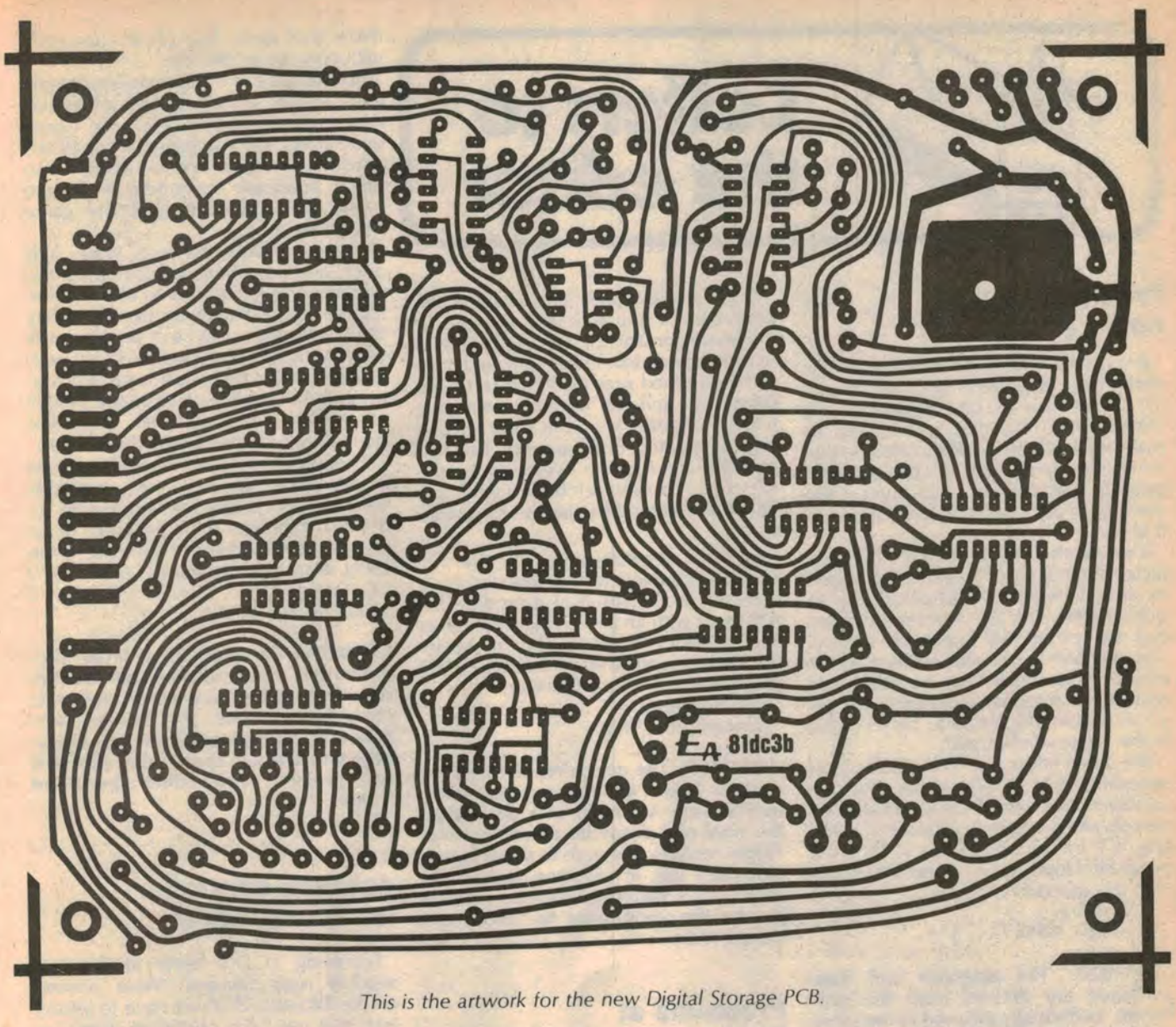
The front panel of the Digital/Analog Storage CRO Adapter is rather cluttered with the many controls. These controls have functions which are divided into three broad sections; the Input, Trigger, and Timebase. The Timebase controls were discussed in the article of the November 1980 issue as was the Set, Delay +/−, Internal/External controls of the Trigger section.



This shows the tracer superimposed on a non-repetitive waveform.

The analog signal to be stored is fed to the "Analog input" socket and the "Analog out" is connected to the oscilloscope. The Digital/Analog switch should be in the Analog position. The Attenuation and Gain controls adjust the signal level to the A-D converter.

The triggering of the signal to be stored



This is the artwork for the new Digital Storage PCB.

can be accomplished by use of the DC/AC/HF/LF Trigger selection, +/−, Int/Ext, Trigger Level as well as the Delay. Normally the AC Triggering would be used, but in some situations it may be necessary to trigger only on a low frequency, high frequency signal or a true DC level, in which case one of these can be selected.

The Trigger level control allows the adjustment of the voltage or position on the waveform where the Analog storage will begin.

For the signal to be converted correctly, the maximum voltage swing of the A-D converter must be limited to less than 5V. To do this some experimentation with the attenuation and gain controls will be necessary.

When setting the Gain and Attenuation controls, it should be noted that at the highest Gain control setting, a bandwidth of 100kHz is not available. Even so, this maximum gain setting is useful when storing waveforms at low frequencies, say below 20kHz.

Apply the signal, with the filter in the off position and a suitable timebase selected for the signal frequency. With maximum Gain (fully clockwise), the Attenuation knob should be gradually rotated from a fully clockwise (maximum attenuation) position while manually continually retriggering with the Set switch. It may be necessary to adjust the Trigger Level control for reliable triggering. At the point where clipping of the waveform just begins to occur is the correct setting. Back off the Gain control until no clipping is evident.

Once a signal has been stored successfully, the filter can be switched on and the tracer signal will appear on the oscilloscope screen along with the stored waveform. It can be important to know where the start of the stored waveform begins and this can be determined with the tracer setting at 1/256. Since with this setting the number of tracers occur only once (at the beginning and end of memory) the start of memory is to the right of the tracer.

Mentioned earlier, there is a maximum timebase limit which can be used for analog storage. This maximum is the 512us setting. On replay of the signal at this setting, the access time of the memory approaches the rate of the memory address clocking and consequently glitches in the converted waveform can result. Lowering the timebase to 16.38ms and lower settings and readjusting the CRO timebase will eliminate this problem. The filter operates at around this timebase and should be set to the highest timebase which gives no attenuation compared to the unfiltered signal.

A few comments on the availability of components: The A-D converter, the DAC0800, is available from Rifa Pty Ltd of 2 Cross Road, Hurstville, 2220, and from Semtech Pty Ltd of 1 Johnston Lane, West Lane Cove 2066, at approximately $3 each in one off quantities. The other components difficult to come by such as the 1% resistors, DM2502 SAR. the LM361 and the 2112 memories can be obtained from Radio Despatch Service of 869 George Street, Sydney 2000.