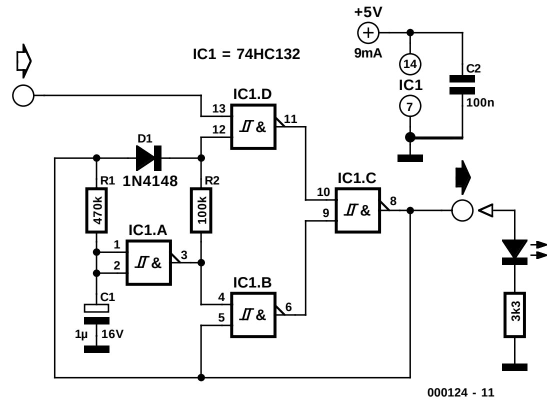
# Pulse Edge Visualiser

019

F. Rimatzki




A digital signal must have a certain duration before it can be monitored using an LED. Short pulses cause the LED to flash for an interval that is too short to be registered by our 'slow' eyes. The small supplementary circuit described here, which consists of only four two-input NAND gates in the form of a 74HC(T)132, two resistors, a diode and a capacitor, lengthens a short pulse enough that it can be clearly recognised using an LED.

The output level at pin 8 prepares the circuit for the subsequent pulse edge. If a logic '1' is present at the output, C1 will be fully charged and the output of gate 1a will be Low. The output of IC1b and pin 9 of IC1c will thus be High. The High level on pin 8, which is applied to the input of IC1d via D1, 'overrides' the Low level on pin 3 that is applied via R2, so a High level is also present at pin 12 of IC1d. The whole arrangement is stable only as long as the input signal is also High.

If on the other hand a Low level is present at the output, the capacitor will be discharged and the output of IC1a will thus be High. This means that pin 9 and pin 12 are also High (D1 is now blocking). This state is also stable, but only as long as the input signal remains Low.

The situation changes as soon as the signal level at the input changes. When a positive or negative pulse edge appears at the input, the level at either pin 9 or pin 12 (respectively) goes Low momentarily while the level at the other pin remains unchanged. As a result, the output level changes in the same direction as the input signal. A new, immediately following level change has no effect, since it can reach the output only if pin 9 and pin 12 are simultaneously High. This is true only after the expiry of a prescribed interval determined by the values of R1 and C1 (in this case, several hundred milliseconds). During this 'dead time', a change in the input level has no effect at all on the output!

The circuit is so compact and simple that it can be used for applications such as debouncing pushbutton switches or digital signals. For such purposes, it can simply be inserted in the signal path.

It can also be easily fitted into the housing of a logic tester, and if a high-efficiency LED is used, it can make even short pulses visible.

By the way, the current consumption of the circuit (around 9 mA average) is least when the input level is Low, since in this case only the gate input current and diode leakage current flow through R2. In the opposite case, a much higher current flows via pin 8, D1 and R2 to pin 3. This behaviour can easily be reversed by simply swapping D1 and R2.

Even more power savings can be realised by replacing D1 and R2 with a true OR gate. With this modification, the circuit can be left permanently connected to a power source and no on/off switch is necessary.

The pulse edge visualiser should be powered from the circuit being tested, if only because of the values of the logic levels. Pay attention to the switching speed (HC or HCT) and the thresholds of the ICs used.

(000124-1)