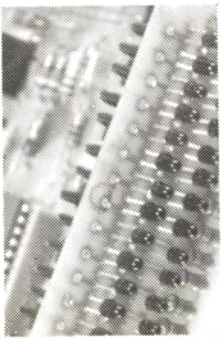
digiscope

For examining pulse trains in digital circuits an oscilloscope is an invaluable aid. However, oscilloscopes are expensive, and furthermore the analogue display capability of a conventional 'scope is rarely required in digital circuits, since only two voltage states, corresponding to logic 0 and 1, are encountered.
The Digiscope offers a low-cost alternative to the conventional oscilloscope for digital work, and displays digital pulse trains on two rows of light-emitting diodes.

E. Muller



The principle of the Digiscope is illustrated in figure 1. The digital waveform to be displayed is sampled at a number of points and the value of the waveform at the instant of each sample (logic 0 or 1) is stored in a number of latches (flip-flops). The Q and $\bar{Q}$ outputs of the latches are connected to two rows of LEDs, the upper row indicating logic 1 and the lower row indicating logic 0. The pattern displayed by the two rows of LEDs will thus correspond to the digital waveform.
This is shown in figure 1, where a digital waveform is shown together with the corresponding display on the Digiscope. Any number of samples can be taken, and obviously the greater the number of samples per cycle of the waveform the more accurate will be the resulting display. However, the cost factor must be considered, since each sample requires a flip-flop and two LEDs, and a reasonable compromise of 16 flip-flops and 32 LEDs was adopted.

Block diagram

Figure 2 shows the block diagram of the Digiscope. The memory consists of 16 D flip-flops. A 'timebase' consisting of a clock oscillator, 4-bit counter and 1-of-16 decoder 'scans' the memory, i.e. takes the clock input of each flip-flop high in turn. The input signal is connected to the D inputs of all the flip-flops, so that if the input is high when the clock input of a particular flip-flop is activated then the Q output of that flip-flop will go high. Conversely, if the input signal is low then the output of the flip-flop will remain low. The scanning of the memory by the timebase is analogous to the spot sweeping across the screen of a conventional oscilloscope, hence the term 'timebase' is used for this function.
Like the timebase of a conventional oscilloscope, the timebase of the Digiscope has coarse and fine speed controls. Fine speed control is effected by varying the frequency of the clock generator between 100 kHz and 500 kHz, whilst coarse speed control is effected by preceding the 4-bit counter by a variable frequency divider, whose division ratio can be varied from 1 to 1000 in steps of 1, 2, 5, 10, 20 . . . etc., just like a conventional oscilloscope. The timebase speed range is from 4 μs per LED i.e. 64 μs for a single scan of the complete display, to 20 ms per LED, i.e. 320 ms to scan the display.

Trigger circuit

In addition to a timebase with a wide speed range it is also important to have a reliable trigger circuit. When the digiscope is used to display repetitive pulse trains the trigger circuit ensures that each timebase sweep starts at the same point in successive pulse trains. If the timebase were not synchronised to the display in this manner then the display would appear to run in one direction or the other depending on the relative speeds of the timebase and the input signal. In addition to being triggered by the input signal the timebase may also be triggered by an external signal or allowed to free run.

Complete circuit

In order to keep the circuit as simple and cheap as possible it was decided to base the design on the 74-series TTL logic family, since this logic family is readily obtainable, inexpensive, can operate at high speeds and is capable of supplying sufficient current to drive LEDs directly. The full circuit diagram of the Digiscope is given in figure 3.
It should be noted that as it stands in figure 3, the Digiscope operates only with TTL logic. However, with the addition of one 4050 CMOS IC, being used as a level converter interface, it can be used with CMOS. The 4050 should be powered by the 5 V supply in the Digiscope, this will allow CMOS

1

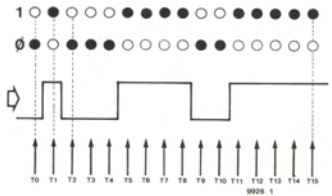
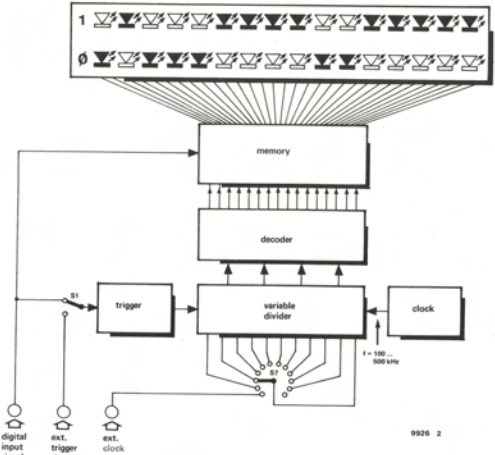


Table 1

S7 position	Approximate maximum timebase speed sec/LED (P1 = 0 Ω)	
%	1000	4 msec/LED
%	500	2 msec/LED
%	200	800 µsec/LED
%	100	400 µsec/LED
%	50	200 µsec/LED
%	20	80 µsec/LED
%	10	40 µsec/LED
%	5	20 µsec/LED
%	2	8 µsec/LED
%	1	4 µsec/LED

2



circuits with a suplly voltage of up tc about 15 V to be tested.

Since there are 6 buffer amps in one 4050, it can also be used for level conversion of the 'clock input', and 'trig. input'. Since the 4050 can only drive 2 TTL loads, it is advisable to connect 2 of the buffer amps in the 4050 parallel, since the input loading of the Digiscope is 3.

The display memory consists of 16 D flip-flops contained in 8 7474 dual D flip-flop packages, IC11 to IC18. Since the D inputs of these flip-flops present a total of 16 TTL loads and a normal TTL output can drive only 10 TTL loads it is necessary to drive the D inputs of FF7 to FF22 in two groups of 8. This is done by a pair of EXOR gates, which buffer the input signal and provide a choice of normal or inverted display depending on the position of S9. The memory is scanned by a 74154 binary to 1-of-16 decoder, IC10, which is driven by the four-bit counter, IC7. The remainder of the timebase circuit comprises the clock generator (which consists of two monostable multivibrators, MMV3 and MMV4, cross-coupled to form an astable multivibrator with good frequency stability) and the variable frequency divider consisting of

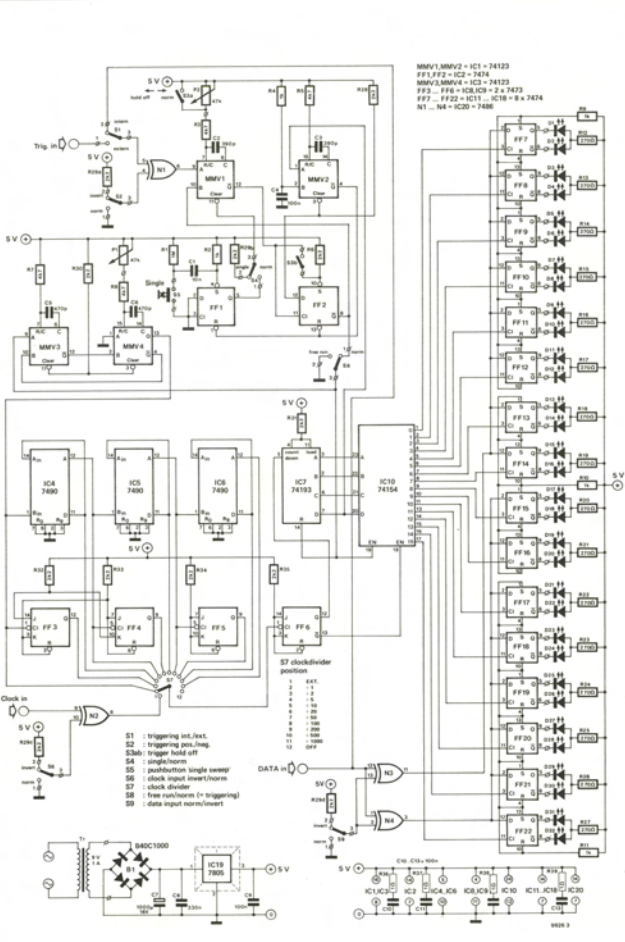
Figure 1. This diagram illustrates the principle of the Digiscope.

Figure 2. Block diagram of the Digiscope.

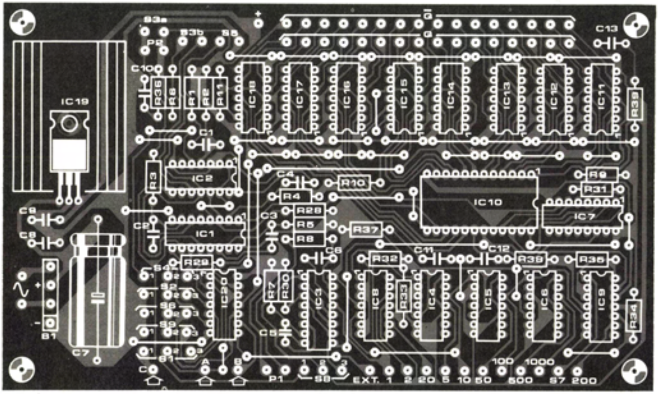
Figure 3. Complete circuit of the Digiscope. Resistors R29a, b, c and d can, of course, be replaced by a single resistor (R29) as on the p.c. board.

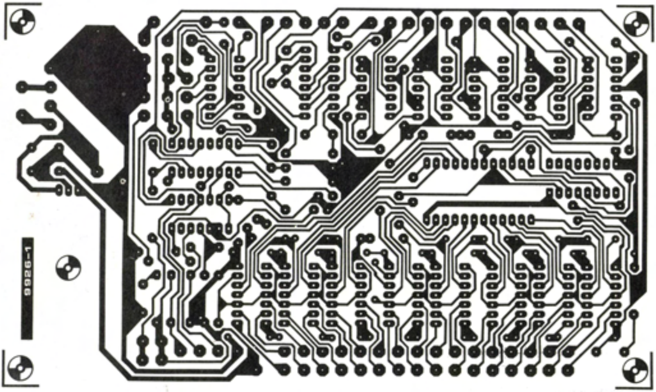
Table 1. Listing of the timebase ranges for each position of the timebase switch.

3


MMV1,MMV2 = IC1 = 74123
FF1,FF2 = IC2 = 7474
MMV3,MMV4 = IC3 = 74123
FF3 ... FF6 = IC8,IC9 = 2 x 7473
FF7 ... FF22 = IC11 ... IC18 = 8 x 7474
N1 ... N4 = IC20 = 7486
Trig. in
Single
Clock in
DATA in
IC4 7490
IC5 7490
IC6 7490
IC7 74193
IC10 74154
MMV1
MMV2
MMV3
MMV4
FF1
FF2
FF3
FF4
FF5
FF6
FF7
FF8
FF9
FF10
FF11
FF12
FF13
FF14
FF15
FF16
FF17
FF18
FF19
FF20
FF21
FF22
S1 : triggering int./ext.
S2 : triggering pos./neg.
S3ab : trigger hold off
S4 : single/norm
S5 : pushbutton single sweep
S6 : clock input inwert/norm
S7 : clock divider
S8 : free run/norm (= triggering)
S9 : data input norm/invert
S7 clockdivider position
EXT.
B40C1000
IC19 7805
IC1,IC3
IC2
IC4..IC6
IC8,IC9
IC10
IC11..IC18
IC20
9925-3

4


S3a
S3b
S5
P2
C10
R36
R6
R1
R2
R11
IC19
C13
IC18
IC17
IC16
IC15
IC14
IC13
IC12
IC11
R39
C1
IC2
R3
C4
R10
R4
R28
R5
R8
C3
R37
IC10
R9
R31
IC7
C9
C8
C2
IC1
C6
C11
C12
R29
R32
R38
R35
S4
S2
S6
S9
R7
R30
IC3
IC8
R33
IC4
IC5
IC6
IC9
R34
C5
B1
C7
S1
C
A
B
P1
S8
EXT.
100
1000
S7
200


9926-1

parts list to figures 3, 4 and 5

Resistors:
R1 = 1 M
R2,R4,R9,R10,R11 = 1 k
R3,R5,R7,R8 = 4k7
R6,R28 . . . R35 = 2k2
R12 . . . R27 = 270 Ω
R36 . . . R39 = 1 Ω
P1,P2 = 47 k

Capacitors:
C1 = 10 n
C2,C3 = 390 p
C4,C9 . . . C13 = 100 n
C5,C6 = 470 p
C7 = 1000 µ/10 V
C8 = 330 n

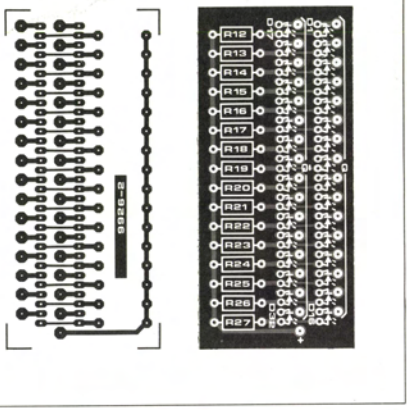
Semiconductors:
IC1,IC3 = 74123
IC2,IC11 . . . IC18 = 7474
IC4,IC5,IC6 = 7490
IC7 = 74193
IC8,IC9 = 7473
IC10 = 74154
IC19 = 7805
IC20 = 7486
D1 . . . D32 = LED
B1 = B 40 C 1000 (40 V/1 A bridge rectifier)

Miscellaneous:
S1,S2,S4,S6,S8,
S9 = switch SPDT
S3 = switch DPDT
S7 = switch single pole 11 (12-)-way transformer at least 9 V/1 A

counters IC4 to IC6 and flip-flops FF3 to FF6. The ranges covered by the timebase switch are listed in table 1. An external clock signal may also be fed in via EXOR gate N3 in normal or inverted form.

The trigger circuit comprises monostables IC1 and flip-flops IC2, and offers a variety of triggering modes. S1 offers a choice of internal or external triggering, whilst S2 selects between normal and inverted trigger signal. By switching S4 to the single-shot mode the timebase can be triggered manually by pressing S5. S3 can be used to switch to 'hold-off', in which mode the trigger pulse can be delayed for a variable period. Finally, the trigger circuit can be inhibited and the timebase allowed to run continuously by switching S8 to the 'free-run' position.

5



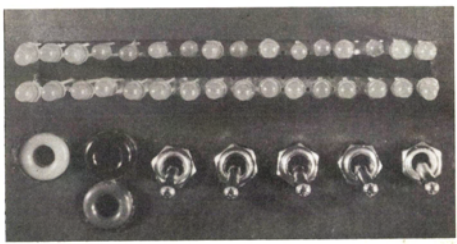


Figure 4. Printed circuit board and component layout for the Digiscope, excluding the display section (EPS 9926-1).

Figure 5. Printed circuit board and component layout for the display section of the Digiscope (EPS 9926-2).

Power supply

The Digiscope requires a stabilised 5 V power supply. The circuit of a suitable supply consisting of a transformer, bridge rectifier, reservoir capacitor and an IC regulator is also shown in figure 3.

Construction

The complete circuit of the Digiscope is mounted on two printed circuit boards. The p.c. board whose layout is shown in figure 4 accommodates all the logic circuits and the power supply, with the exception of the mains transformer, whilst the display is mounted on the board whose layout is given in figure 5. This should be connected to the main board using a 33-core ribbon cable or something similar.