Project 140

1 GHz FREQUENCY METER – TIMER

Pt. 1 Circuit Details

Lab-quality instrument offers superb performance and features at low cost.

OF THE VARIOUS QUANTITIES encountered in electronics (such as charge, voltage, current, frequency), perhaps the easiest to measure accurately is frequency. Various types of frequency-measuring equipment exist, ranging up from the simple absorption wavemeter (every ham should have one) to sophisticated multi-counter instruments which use microprocessors to calculate the measured frequency.

The earliest really accurate instruments were of the heterodyne type (such as the BC221), in which finely calibrated oscillator was tuned to zero-beat with the incoming signal. Many of these devices are still in use. In the late fifties and early sixties came the first 'digital' counters appeared, based on Dekatron tubes, which are cunning decade counter and display valves.

Integrated circuits and LED have now made possible compact, portable counters that can be held in the palm of the hand, and these can easily be built by the hobbyist. What we haven't seen however, is a design for use at UHF, where CB and mobile radio, are appearing, or which offered versatile measurement of time or period.

With these thoughts in mind, we set out to do a design study, and came up with a lab-quality instrument which should be very reasonably priced. The design is based mainly on TTL with some CMOS and ECL. We rejected LSI MOS and CMOS devices for various reasons. Although this increases board size and power consumption, the gain in simplicity of layout and trouble-shooting, as well as leading zero suppression, is well worth-while.

SPECIFICATIONS ETI – 140

Modes of operation	**Frequency, period and time**
Range	
Frequency	10Hz – 50MHz
High frequency	50MHz – 1GHz *
Period	0.1μs – 10 sec.
Time	1μs – 100 sec.
Resolution	
Frequency	1Hz
High frequency	10Hz
Period	0.1μs
Time	1μs
Display	**8 digit LED, leading edge blanking**
Sensitivity	
Normal input	20mV
High frequency input	20mV
Time inputs	0V to +3V level shift
Input impedance	
Normal input	1Meg // 15pF
High frequency input	≈75 ohms
Time input	>10k
Maximum input voltages	
Normal input	70V ac,∓ 100V dc
High frequency input	200mV ac,∓ 50V dc
Timing inputs	∓100V dc
Crystal frequency	
nominal	4000kHz
actual	3999.995kHz
Stability and accuracy	
Frequency	Depends on crystal used and initial adjustment. Oven used keeps temperature within 2° C.
Period and time	approx –0.000125%

* The upper limit of the prescaler has not been checked due to the lack of a signal source but both the preamplifier (OM335) and the divider ICs are specified up to 1GHz.

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Design Feature

When considering this instrument initially we looked at ways to reduce both cost and component count of the unit. Our initial design of the counter section used TTL for the first two stages and CMOS for the rest. It then called for four 8 bit shift registers to take the information from the counters, latch it, and provide the multiplexing for the display. Multiplexing reduces the power consumption of the displays for the same light output and the total network would have saved 10-11 packages. However the PCB layout beat us unless a plated through board is used which would have cancelled any cost saving. The increased difficulty of fault-finding, even with fewer components, also weighed against this approach.

The counter in the LSD position has to operate at over 50 MHz. The only way to obtain this performance was to make our own divide by 10 using 74S74 dual D type flip flops as the 74LS90 is only specified to 32 MHz (although one sample we had worked at 60 MHz) and the 74S90 is no faster.

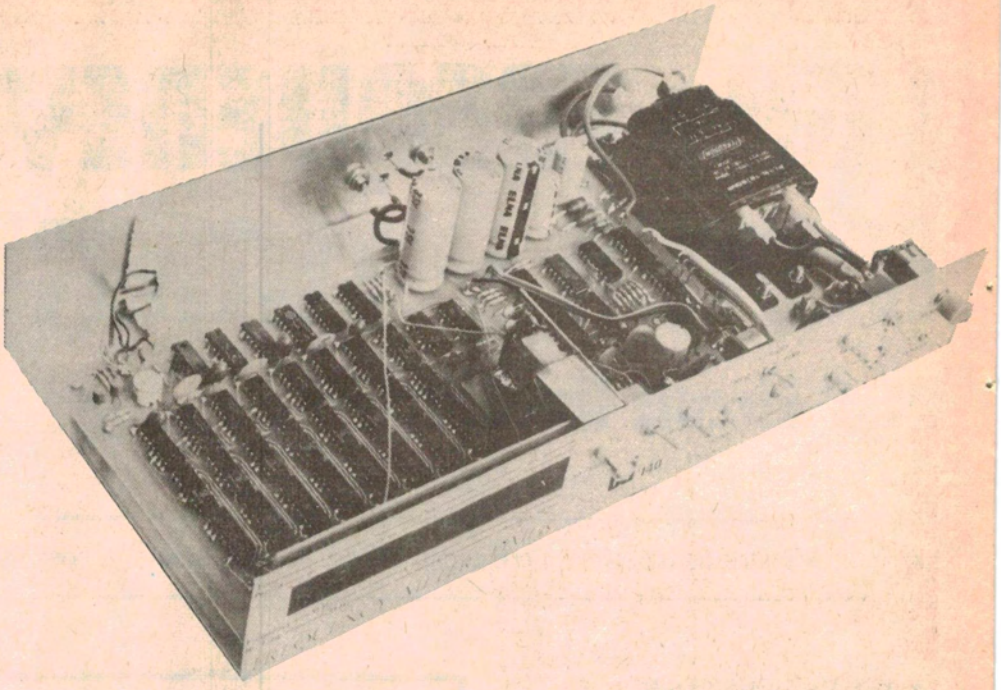
The network of 74S74's should give 60-70 MHz minimum clock rate.

Preamplifiers which can work from almost dc to 50 + MHz involving a Schmitt trigger always prove troublesome and this one was no exception. We originally dc coupled it throughout using matched FETs and a differential pair to give the correct level for the 9585 IC. This proved to have too much gain to be stable and the design shown here was the final result. Originally we used three diodes to limit the output voltage to +2v in the ECL-TTL translator but replacing it with a resistor-diode not only made it cheaper but increased the frequency response by 50% and improved stability.

Operation

The frequency and period modes are commonly known and do not require much explanation. The only extra control provided over the normal sensitivity control, is the dc shift. When measuring the frequency or period of a pulse waveform where the pulse is narrow in relation to the repetation rate, triggering problems can arise. This is due to noise pulses being counted as the average voltage is almost zero. However by using the dc shift the signal can be lifted above (or below) zero and the problem eliminated. For maximum sensitivity on normal ac signals the dc shift must be adjusted back to zero.

With the time mode intervals from 1 μs to 100 sec can be measured using



pulses or level changes, into the respective sockets. A voltage change from 0V to 3V (or +3V to 0V) is all that is necessary although up to ∓ 100V can be used. For accurate timing the pulse should have a rise time of less than 1 μs. For measuring single pulses, both inputs can be paralleled and starting and finishing on opposite edges. If it is a repetitive pulse chain the unit will time the first pulse after the release of the reset button.

Calibration and Testing

To calibrate the unit a known frequency is needed so that CV1 can be adjusted to give the correct reading. Alternatively a radio receiver can be used tuned to the PMG 12 MHz time transmission, VNG, and the 4 MHz crystal beat against it (take a wire from pin 11 of IC30, wrap it around the radio aerial and adjust for zero beat. This sets the crystal to exactly 4 MHz. However this is not the exact frequency needed (life wasn't meant...). Now feed the 4 MHz into the input and record the result. It should be about 3,999,995 Hz which is about 0.000125% low. Now measure the frequency of another crystal (*or extremely stable*) oscillator, record the reading and then adjust CV1 to give a reading 0.000125% higher (or whatever error your unit requires). As this low reading is due to the time required for the strobe-reset pulses it is independent of the crystal frequency and adjusting CV1 will not affect the reading when the counter is used to measure its own internal frequency.

Adjustment of the crystal trimmer should not be done until it is warm (allow 10 minutes) and the oven should be fixed into the chassis to prevent movement of the leads which can affect the frequency slightly. If CV1 does not have enough range the parallel capacitor should be varied.

The period mode should be checked for operation. With the time mode the display can be reset by the push button and timing can be started by shorting out the start socket and stopped with the stop socket. Starting and stopping can also be performed by switching the polarity switches from negative to positive edge triggering. It should not be possible to restart the counter before the display has been reset.

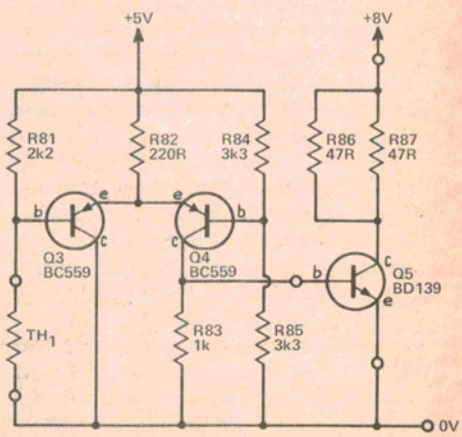


Fig. 1. The circuit diagram of the oven circuit

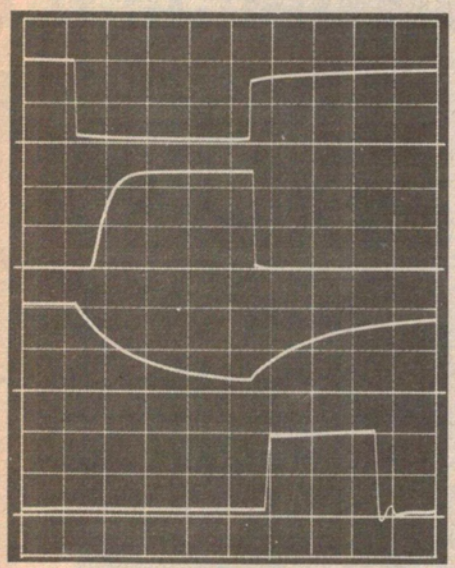


Fig. 2. Waveform diagrams showing the relationships of the strobe-reset pulses. They are, from the top down:
The output of IC37/1, pin 13
The 'strobe' pulse, i.e. the collector of Q2
The input to IC37/2, pin 10
The reset pulse on pin 5 of IC37/2
The vertical scale is 2 V/division while the horizontal is 200 ns /division. It can be seen that between the strobe pulse and the reset pulse there is a delay of about 50 ns.

The following pins are not shown on the circuit diagrams but are connected as shown below. Pins in the third * column are used as interconnections or are unused inputs terminated to some output.

	To +5V	To 0V	*
IC1	4,10,14	7	
IC2	4,10,14	7	
IC3	5	4,6,7,10	13
IC4	5	4,6,7,10	13
IC5	5	4,6,7,10	13
IC6	5	4,6,7,10	13
IC7	5	4,6,7,10	13
IC8	5	4,6,7,10	13
IC9	5	4,6,7,10	13
IC10	5	12	
IC11	5	12	
IC12	5	12	
IC13	5	12	
IC14	5	12	
IC15	5	12	
IC16	5	12	
IC17	5	12	
IC18	3,5,16	8	
IC19	3,16	8	
IC20	3,16	8	
IC21	3,16	8	
IC21	3,16	8	
IC22	3,16	8	
IC23	3,16	8	
IC24	3,16	8	
IC25	3,16	5,8	
IC26	14	7	8,9
IC27	5	2,3,6,7,10	
IC28	14	7	
IC29	14	7	
IC30	14	7	
IC31	2,4,6,7,10	11	
IC32	16	1,7,8,9,15	
IC33	16	1,8,9	1,2,3
IC34	14	7	
IC35	16	1,7,8,9	
IC36	14	7	
IC37	2,3,11,16	8	
IC38	14	7	1,2,5,6
IC39	14	7	
IC40	5,14	6,7,8	
IC41	14	7	
IC42		2,3,5,6	

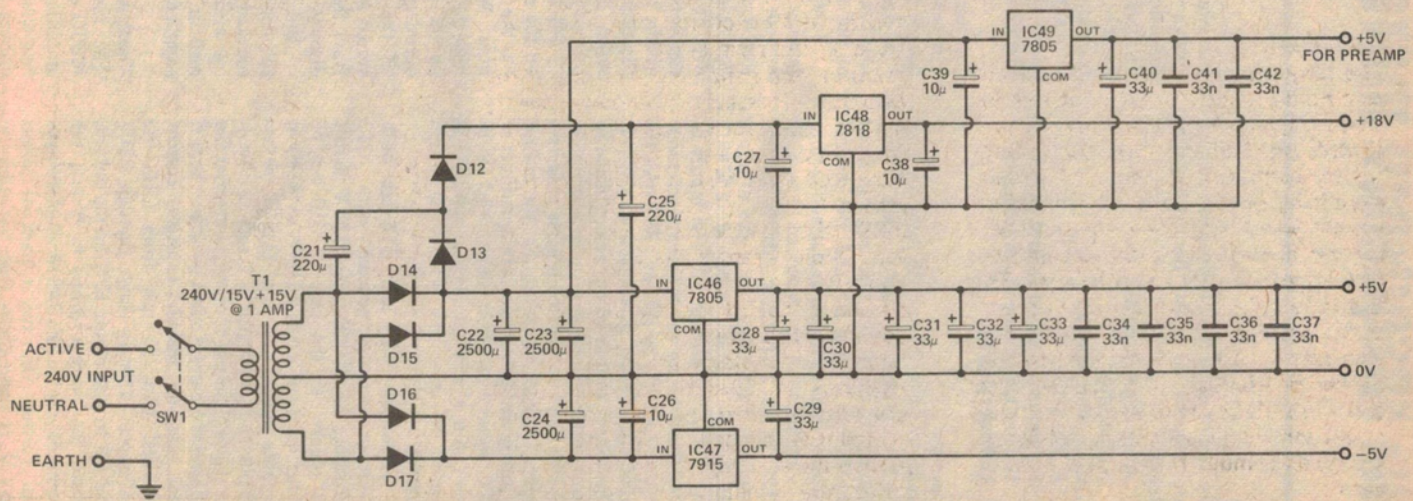


Fig. 3. The circuit diagram of the power supply

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HOW IT WORKS – ETI 140

The circuit is complex but can be sparated into sections to make the explanation clearer:

A. Input preamplifier.
B. Prescaler.
C. Counter section.
D. Time base.
E. Frequency-period control logic.
F. Time measurement control logic.
G. Power supply.

Preamp

Transistors Q6, Q7 and Q8 form the high to low impedance unity gain buffer required to allow the one megohm input impedance. Diodes D5 and D6 prevent excessive input voltages damaging the unit.

Amplification is provided by IC42 which is an ECL triple differential line amplifier. Each stage has a gain of about seven giving a total voltage gain in IC42/1 and IC42/2 of around 50. The inputs of IC42/1 are biased to the internal reference voltage (pin 11) by R91 and R92 with the input signal being ac coupled via C10,11. The voltage on pin 16 can be dc shifted to allow better triggering on pulse type inputs.

The third section of IC42 is used as a Schmitt trigger to ensure that the output is square and jitter free. As the outputs of ECL move only from about +3.3 V to +4 V (on a +5V supply), a translater is needed to drive the TTL logic which follows.

Transistors Q10 and Q12 are both constant current sources with Q12 providing about 18 mA (0.6 V across 33 ohms). As the base of Q10 can be either of two levels (3.3 V or 4 V) it supplies either 33 mA (1.1 V across 33 ohms) or 9 mA (0.3 V across 33 ohms). As the two current sources are in series the differential current must go somewhere if they are to remain constant current supplies! With 33 mA from Q10, the difference (15 mA) flows through R103 and D9 to give about +2 V on the output. When the current drops to 9 mA the clamp diodes in the 74S10 which follows the preamp clip the voltage at about -0.7 V. If these limits were not used the the two inputs Q9 and Q13 are used to disable one of the inputs. With both transistors off the prescaler output is disabled (it needs a pulldown resistor), leaving the normal input active. If the transistors are on the prescaler is operational but the dc shift on pin 16 of IC42 forces the output (pin 7) high, effectively disabling the input.

Counter Section

The counter section consists of eight decade counters, latches, decoders and the LED displays. Due to the symmetry of the network the centre four stages aren't shown on the circuit diagram.

Seven of the counter stages are the familiar 7490/7475/7447 combination (except that they are the LS versions) but the decade counter of the LSD (least significant digit), which has to work at over 50 MHz is made out of four D type flip-flops using a NOR gate to get the divide by ten function. Both the D type flip-flops and the NOR gate have to be 'S' series TTL to give 50 MHz + operation (our prototype went over 100 MHz!).

All the counters can be reset by a '1' on the reset line and counting is advanced on the positive transition of the count input. With the latches, if the strobe line is high ('1'), whatever data is presented to it by the counter will be transferred to the decoders. When the strobe line goes to a '0' the data present at that time will be stored and displayed with the information from the counters no longer affecting the display.

Due to the interconnection between the decoder IC's the leading zeros will be blanked, leaving only the right hand digit on with no input signal. To reduce the load on the 5V regulator the displays are supplied from the unregulated supply.

Timebase

The timebase is a 4 MHz crystal with IC30/1 and IC31/2 providing the necessary amplifier to make an oscillator. The frequency is adjustable by CV1. For critical applications an oven can be used, stop dividing (this is used in the time mode). This 1 MHz output is then divided to 10 kHz by IC32 (dual decade counter) and then to 100 Hz or 62.5 Hz by IC33. This IC is a dual divide by 16 counter with the AND gate IC34/1 resetting the first half (IC33/1) upon reaching decimal 10 and IC34/2 and IC34/3 resetting the second half to zero at ten if the control input to pin 13 of IC34 is high. If it is low the reset pulse is disabled and the counter will divide by its normal 16. This change in division ratio is necessary as the prescaler divides by 16 and not 10. A final division by 100 is done by IC37 to give the final timebase periods of 1 s and 1.6 s.

Frequency-Period control logic.

In the frequency mode the output of the preamp is coupled to the count input of the display section via IC28/1 and IC28/3. These need to be 74S10 (not LS) to handle the frequencies involved. The 1 sec (or 1.6 sec) time base is coupled to the monostable IC37/1 via IC36/1 and IC36/3 and is therefore triggered every one second generating a pulse 800ns wide. This is used for the strobe pulse (open and close the latches every one second). This output also disables counting during this period to eliminate any error due to the latch closing while a pulse is still rippling through the decade counters.

The output of this mono has to be buffered by Q2 as the input of the latches is equal to 32 LS TTL loads (about 15mA). This transistor causes a propagation delay of 100 ns on the leading edge and 50 ns on the trailing edge. After a delay at about 80 ns (which is to compensate for the 50 ns propagation delay of Q2) the second monostable IC37/2 is triggered giving a 250 ns wide pulse. This is the reset pulse. The process of frequency measurement is therefore to reset the counters, clock the counters at the input frequency, after 1 sec open and close the latches which displays the number reached by the counters, then immediately reset the counters and start the process all over again.

In the period mode the 1 MHz output totally wrong result. Because of this we use the RS slip flop IC38 which is set by the strobe pulse, stopping any further pulses, and reset by the 'C' output of IC35/2. This IC (IC35/2) is reset by the strobe pulse and the 'C' output does not occur for 400 ms giving a maximum reading rate of 2.5 per second. The reset pulse is not involved in this process and occurs every 10 clock pulses of the input.

Time Measurement

Separate inputs are used for time measurement with both start and stop inputs available. These inputs are buffered by IC39 with both true and complementary outputs available.

Timing is done by coupling the 1MHz output to the count input (via IC28/2, IC28/3 as per period mode), holding the latches open so the counter information is always displayed and controlling the divide by 4 (IC31) to stop and start the counting.

This control is performed by the D type flip flops IC40/1 and IC40/2, after being gated by IC41/3 and IC41/4. If the Q output of IC40/1 is a '1' and the $\overline{Q}$ output of IC40/2 is a '1', IC31 will be enabled. When the reset button is pressed IC40/1 is set to a '0' on Q, and IC40/2 to a '1' on $\overline{Q}$, disabling IC31. This also puts a high on the 'A' input of the reset monostable IC37/2. When the button is released this causes a reset pulse to occur resetting the counters (and display) to zero.

The D input of IC40/1 is normally connected to a '1' and this is clocked into the Q output on the positive transition of the input to pin 3. When this occurs counting will start. This also puts a '1' on the D input of IC40/2 and if a positive transition occurs on pin 11 (clock) the Q will go to a '1' and the Q to '0', which will stop the counting. Triggering the stop input before the start will have no effect as the D input is a '0' and once toggled no further action will occur until reset by the pushbutton. Either positive or negative edge triggering can be selected allowing the width of a pulse to be measured by feeding it to both inputs and selecting the

transistors would saturate, reducing the response to a few MHz.

Prescaler

For frequencies above 50 MHz, a prescaler is used with an amplifier IC43 providing about 26 dB gain to frequencies up to about 1 GHz and IC44 and IC45 each dividing the signal by four to give a total division by 16. To compensate for this odd division the timebase is changed from 1 sec to 1.6 sec when the prescaler is used.

As these dividers are ECL (what else at 1GHz!) a similar translater is used (Q11). To prevent interference between and this is controlled by Q3 and Q4. These transistors compare the voltages on their bases and control the drive to Q3, which, along with R86 and R87, is mounted on the crystal body to act as a heater. Also on the crystal body is the thermistor TH1 which provides the necessary feedback to Q3 to stabilize the temperature at about 70°C. The crystal is mounted in a polystyrene box to provide the thermal insulation required.

The output of the oscillator is buffered by IC30/3 before being divided by four by the JK flip flop IC31. If the JK inputs of IC31/1 are taken low the flip flop will from IC31 is gated into the count input via IC28/2 and IC28/3. The output of the preamp, after being divided by ten in IC27 then controls the strobe-reset monostables via IC36/2 and IC36/3. The result is that we count the number of one μs pulses in the time taken for 10 cycles of the input frequency. This gives the period of one cycle to 0.1 μs accuracy. Problems with flickering occur when updating a display more often than about 1/5 sec, especially 7 segment displays, as the eye cannot follow the change. This can be shown that if the display is alternating between 100 and 99 the result could appear as 188 which is a appropriate edge.

Power Supply

Four voltages are required for the unit: +5 volt for most of the logic, +8 volts unregulated for the displays (to save power disapation in the 5 volt regulator) +18 volts for the prescaler and -5 volt for the preamplifier. A separate +5 volt regulator is used for the preamplifier and prescaler to prevent any feed back via transients in the 0V line.

The regulators are standard 3 terminal regulators with the ∓8 volt supply simply fullwave rectified. The +26V for the 18V regulator is voltage tripled.

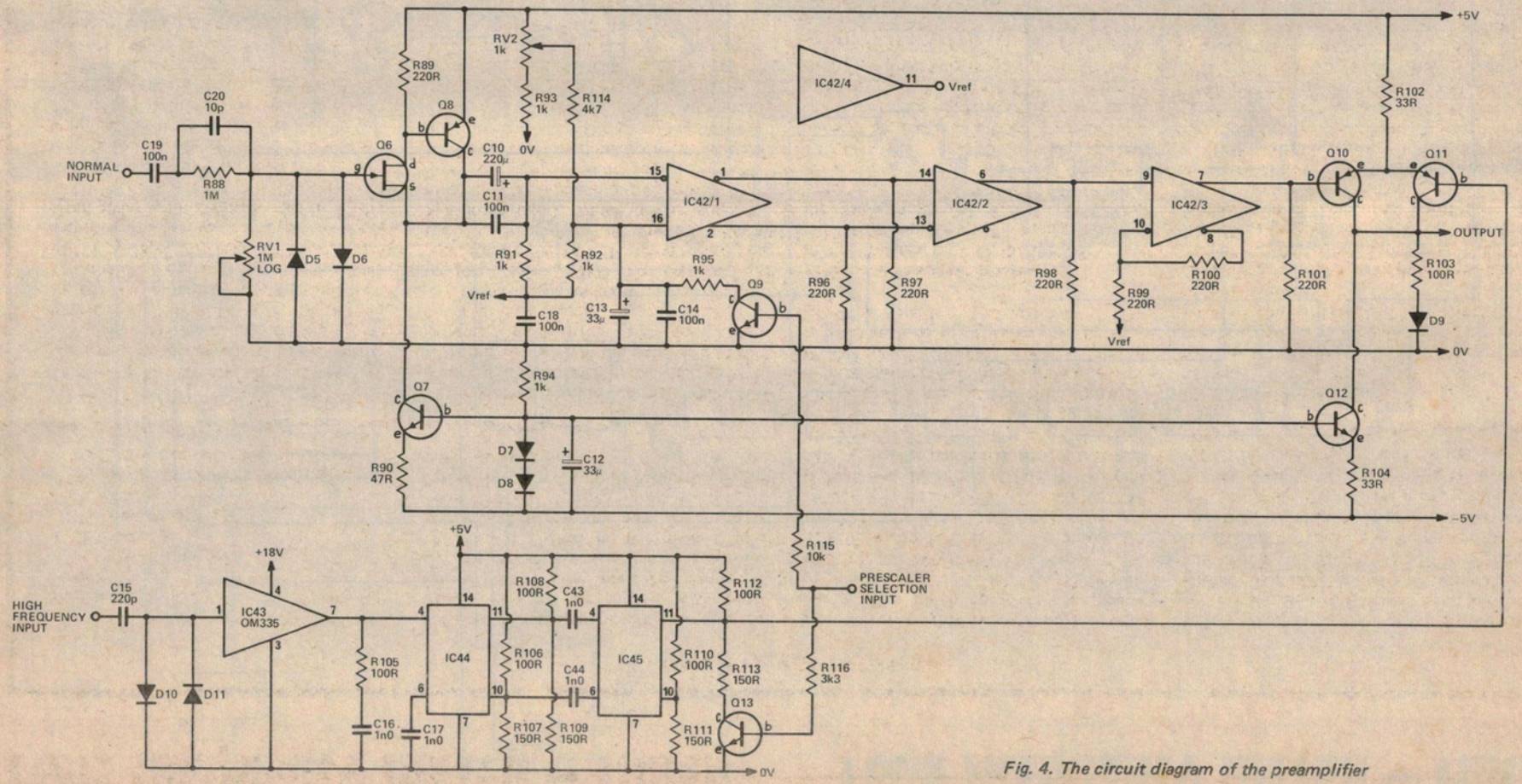

Fig. 4. The circuit diagram of the preamplifier

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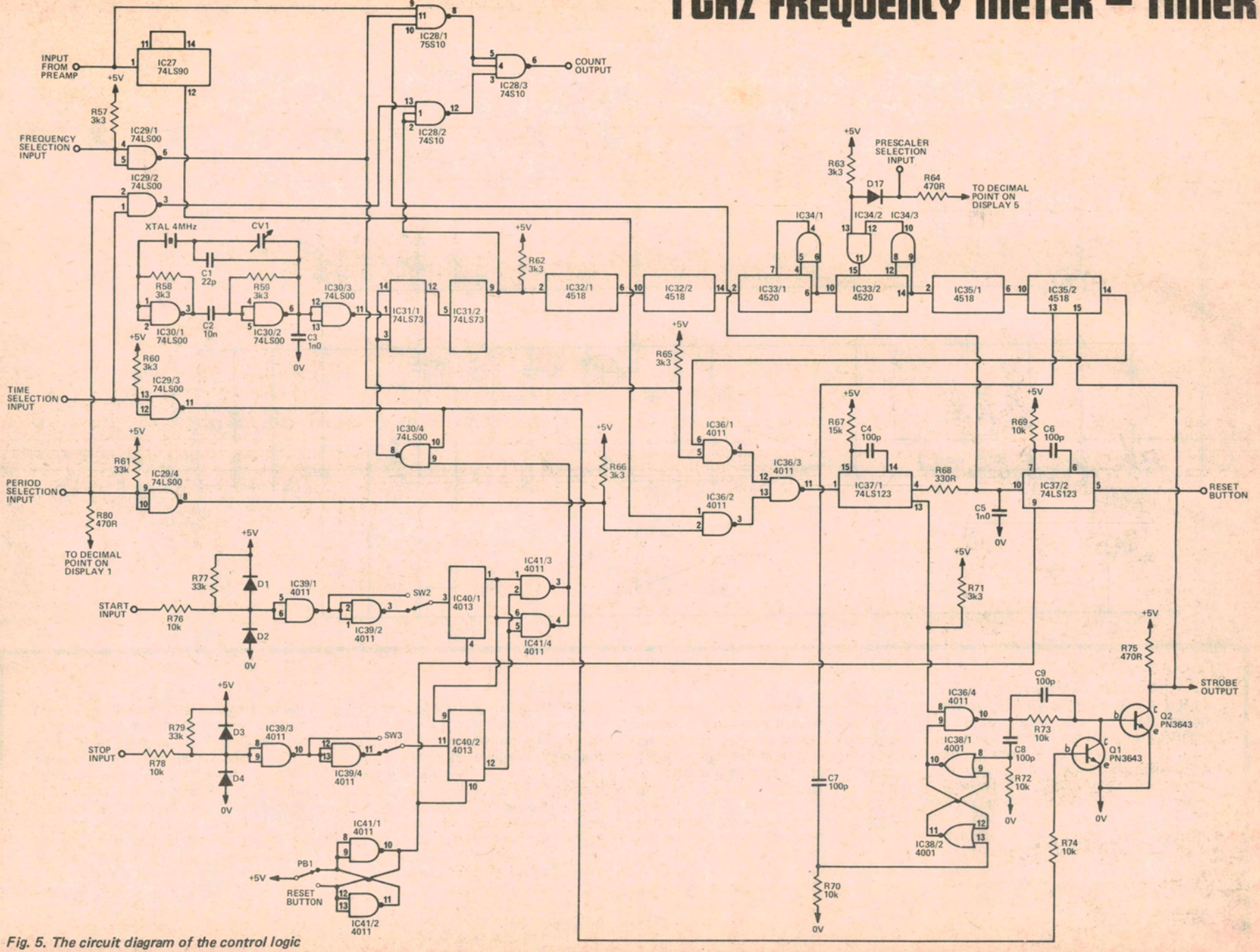
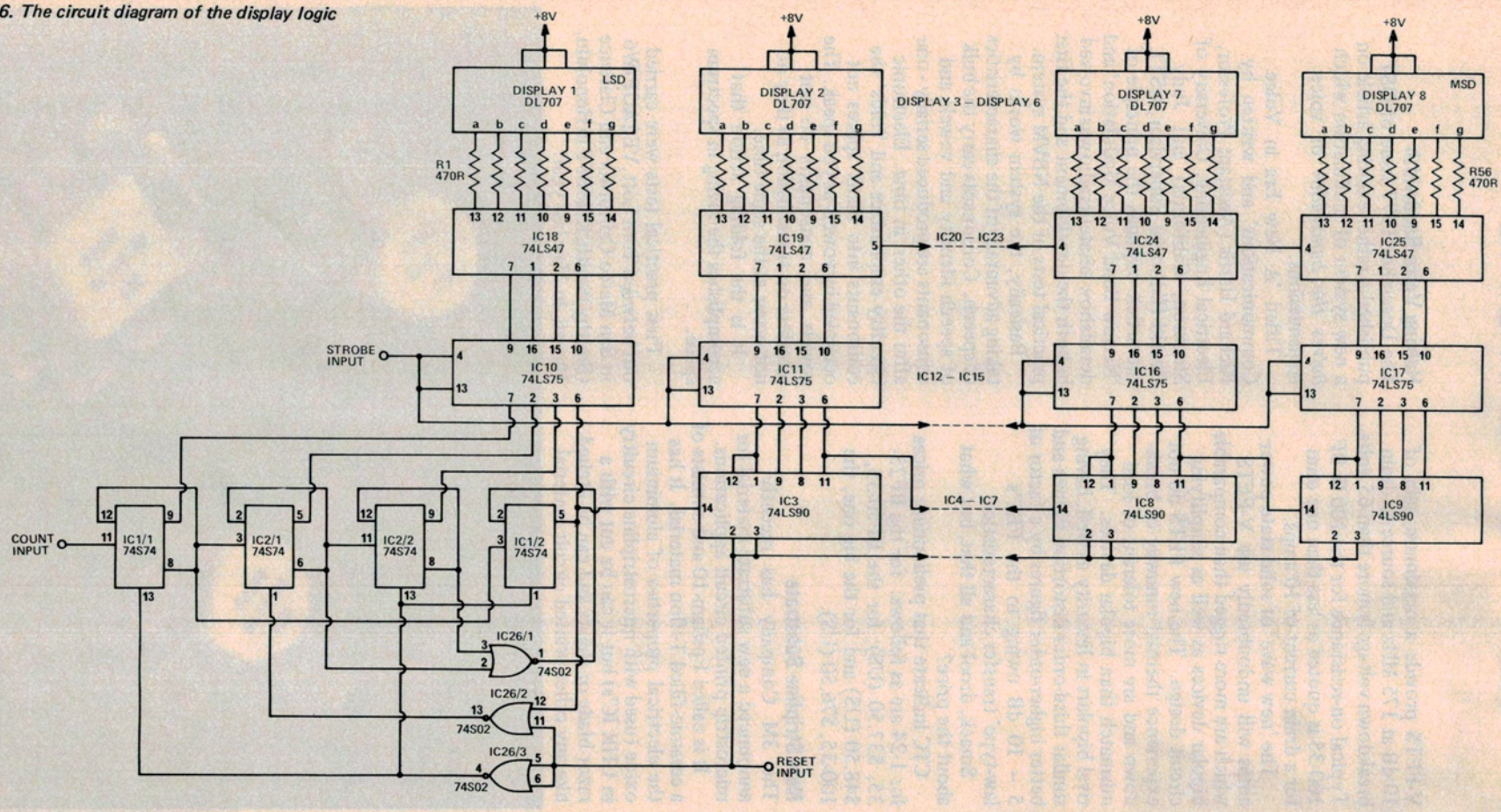


Fig. 5. The circuit diagram of the control logic

Fig. 6. The circuit diagram of the display logic



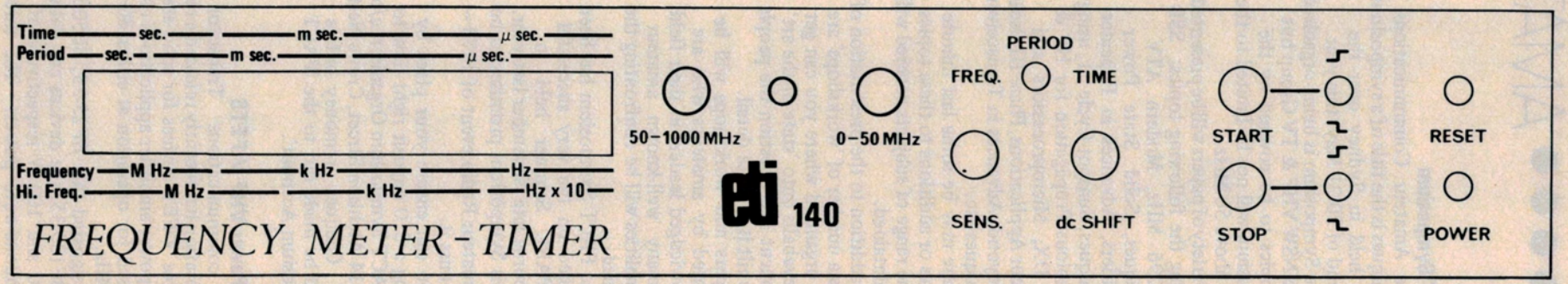


Fig. 7. The front panel artwork. Full size 320mm x 55mm