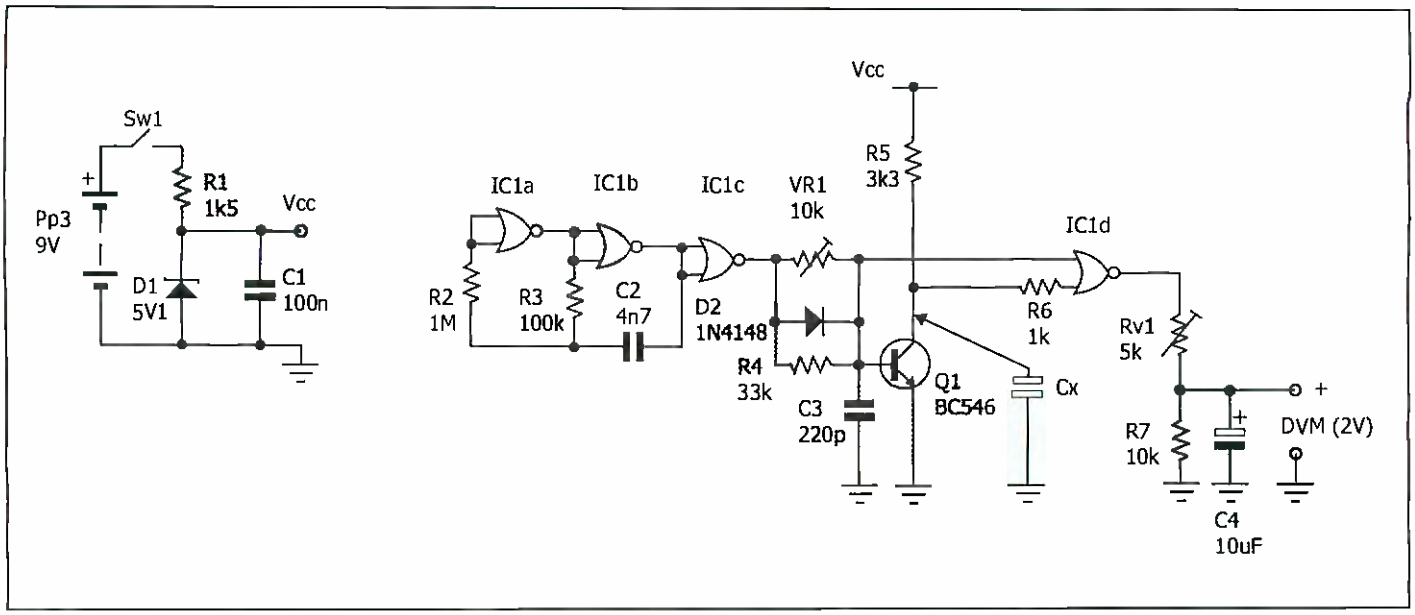
Simple One Chip CAPACITANCE METER

by John Edwards



THIS CIRCUIT IS FOR A VERY SIMPLE CAPACITANCE METER. CALIBRATION IS PROVIDED TO TRIM OUT THE STRAY CAPACITANCE SO THAT IT CAN MEASURE SMALL VALUES.

As drawn, it is for a single fixed example range of 20nF full scale, but it is easily adaptable over a wide range, and to cover multiple ranges. Details of construction are not shown.

The way it works is to use the unknown capacitor Cx to set the width of a pulse. By generating this pulse at a fixed frequency, an output is generated in which it has a duty cycle proportional to the value of Cx. This signal is then filtered and metered. The meter is calibrated to give full scale when the duty cycle is at its maximum. In this circuit, the maximum duty cycle will be 50 (that is, the pulse will be high for half of the cycle)

A PP3 is used for power, as it is easy to connect to. Measurement begins with SW1 closing, which turns the power on; a press-button switch might be best here. Vcc is set at 5.1V by R1 and zener D1, and is supplied to the 74HC02 quad NOR chip. This chip needs a decoupling capacitor C1 mounting close to it across the power pins. Three NOR gates U1a and U1b form a commonly used oscillator, with R3 and C2 as the main timing elements and U1c as an output buffer. The squarewave output 'Osc' of this oscillator drives the transistor Q1 on and off. When Osc is high, it discharges Cx with Q1, whilst forcing U1d output low via D2. When Osc goes low, the transistor is turned off, and Cx starts to charge via R5. After a slight delay set by VR1 and C3, U1d output will go high. This short delay in releasing U1d compensates for the turn-on delay of Q1, and for stray capacitance on the Cx terminals, and due to D2 it is only applied to the falling edge of Osc. When Cx voltage on rises through the logic threshold of U1d, the output of this gate will go low again, so producing a variable duty-cycle signal. The maximum duty cycle is 50 , which when averaged will give Vcc/2, This is just over 2.5V. For the circuit values given this will be when Cx is about 23nF, so VR2 and R7 form a potential divider to give a maximum output across R7 of 2.3V. Then a DVM on a 2V range can be used across R7 to measure up to 20nF with 10pF resolution. Note that polarised capacitors should be connected with the positive end towards R5.

Reducing C2 in value increases the pulse rate, and thereby reduces the value range for Cx which gives the equivalent of 2V out on the DVM. For example, changing it to 470pF will give a 2.0nF full-scale equivalent reading, increasing it to 47n will produce an effective 200nF full-scale. Alternatively, R5 can be altered. Increase it to reduce full-scale. Reducing it is not advised, as this increases the current drawn from the PP3. The circuit values give a pulse rate of around 9.25kHz, and a time period of 108us. Full scale occurs when R5 times Cx is 0.7 times this, which is 76.4us, so with R5 at 3.3k, the maximum for Cx would be around 23nF.

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