DIGITAL CAPACITANCE METER

Any test bench would love to have our hand-held capacitance meter!

MICHAEL LASHANSKY

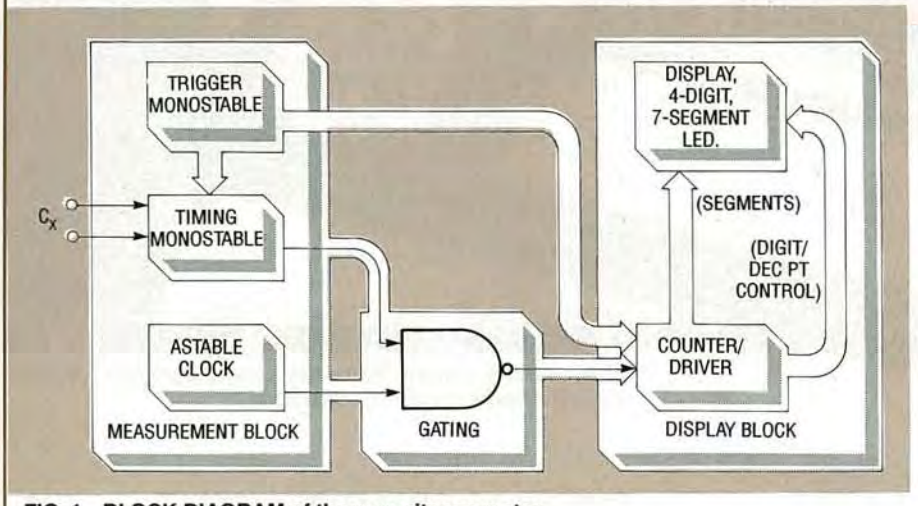

FIG. 1—BLOCK DIAGRAM of the capacitance meter.

HOW MANY TIMES HAVE YOU RUMMAGED through your parts box for a capacitor with a particular value, only to find a handful with confusing color codes or numerical markings that look like weird hieroglyphics? If you're lucky, you might find one you can decipher. Otherwise, you'll have to guess its value, and decide if you can stand a mistake. That's not too professional, but we all do it from time to time.

The problem is that most manufacturers have separate marking nomenclature for capacitors, causing total chaos for hobbyists. The military got smart and standardized their nomenclature requirements a long time ago, but consumer capacitor values are still almost impossible to read. There's been a push toward total standardization of capacitor values, but don't hold your breath.

So what do you do while the industry bickers over nomenclature? If you can't read your capacitors, you can either throw them out, or buy an expensive commercial capacitance meter. But perhaps the best solution is to build our inexpensive hand-held capacitance meter. It's accurate enough for hobbyists, uses readily available components, and can be powered from either a common 9-volt battery or 7.2-volt Ni-Cd.

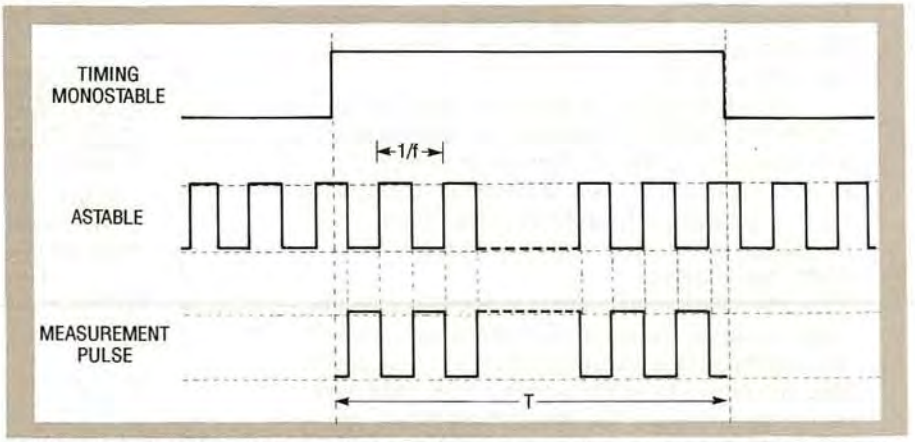

FIG. 2—TIMING WAVEFORMS of the capacitance meter. The number of astable pulses in the measurement pulse is proportional to the value of the unknown capacitor within a factor of 10.

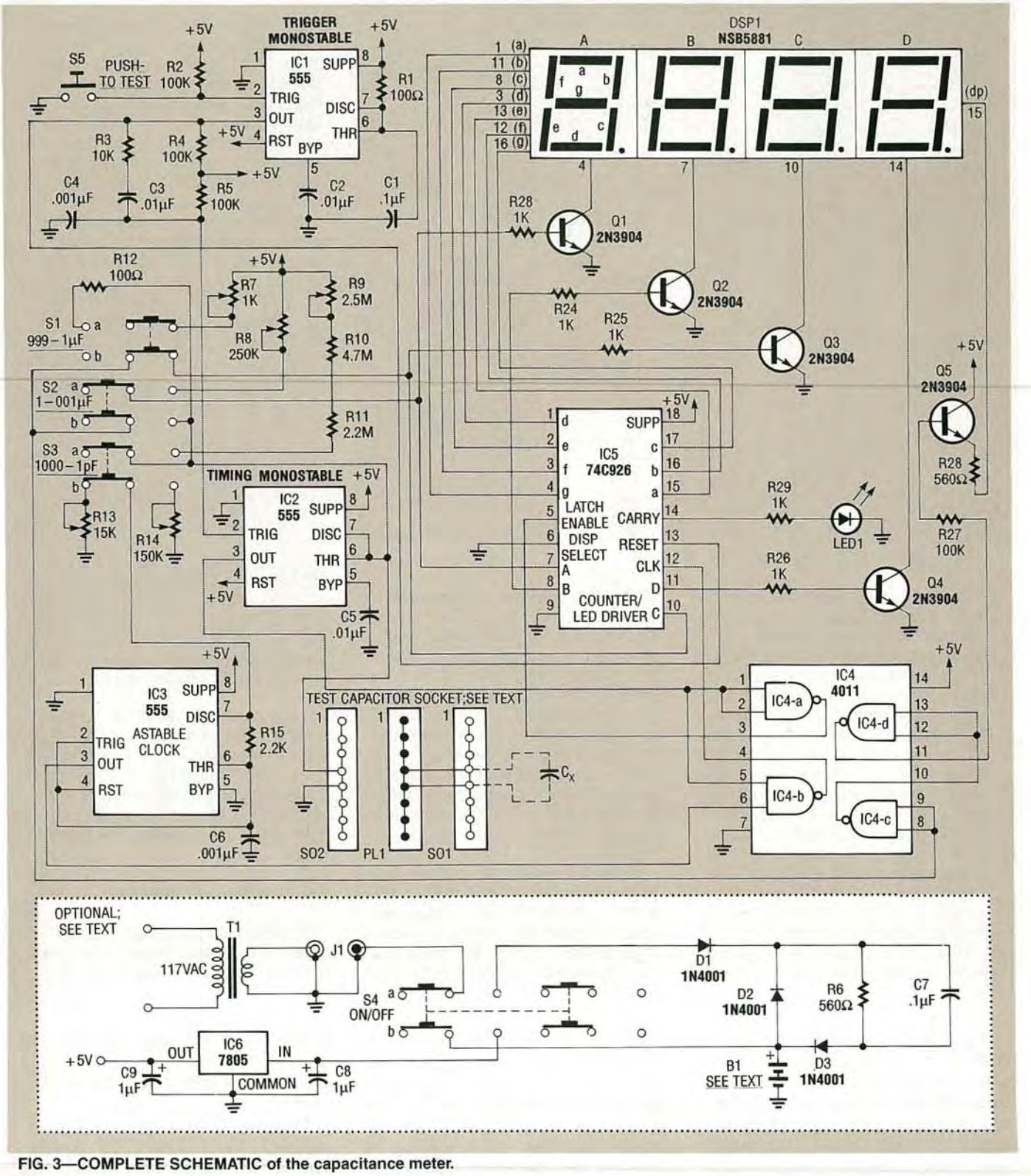

FIG. 3—COMPLETE SCHEMATIC of the capacitance meter.

Circuit theory

To determine the value of an unknown capacitor, C_X, the technique shown in the block diagram of Fig. 1 is used. The unknown capacitor controls the width of the output pulse from the timing monostable. And since the pulse width is proportional to C_X, its value can be determined by measuring the duration of the pulse.

An independent astable multivibrator generates a clock waveform that is NAND-gated with the timing monostable's pulse to yield a measurement pulse (see Fig. 2). The number of astable pulses fitting within the "window" of the measurement pulse is counted and scaled to C_X.

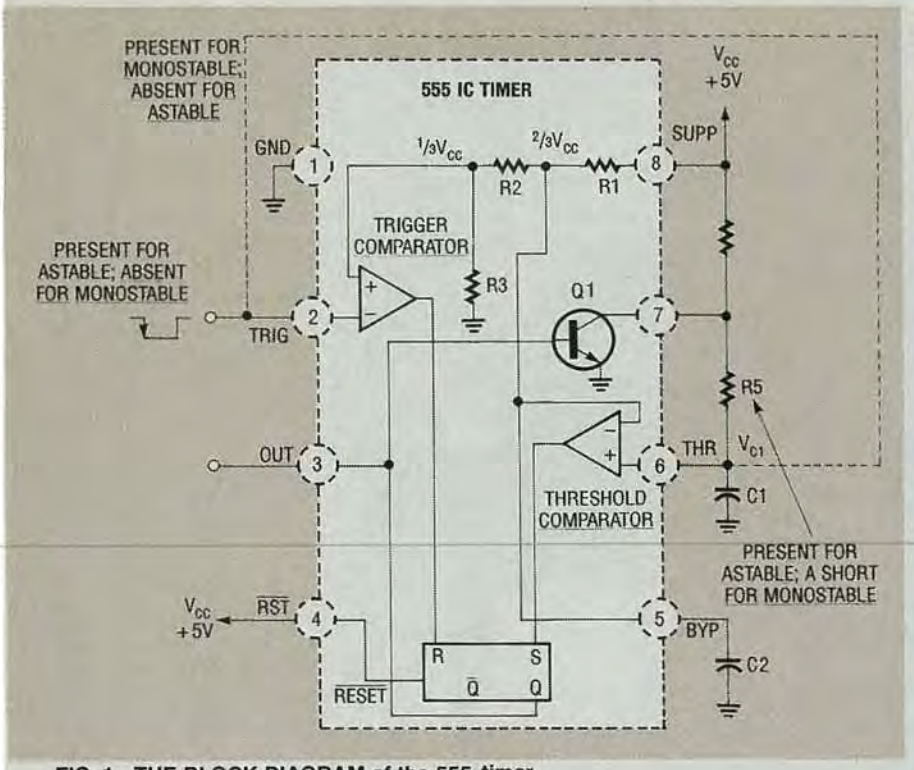

FIG. 1—THE BLOCK DIAGRAM of the 555 timer.

The 555 is the most versatile IC timer ever developed for astable/monostable operating modes, and it needs very few external components to use it. Figure 1 shows the 555's block diagram, with its threshold and trigger comparators, set-reset (S-R) flip-flop, NPN discharging transistor (Q), a noninverting buffer, and an internal voltage divider R1/R2/R3 for comparator reference levels. The flip-flop is "set" if high, and "reset" if low. The comparators sense the variation in C1's voltage in either mode, and charges and discharges C1 between ⅓ and ⅔ of V_{CC}, or about 5 volts. C1's voltage is not the output, but it does govern the 555's operation.

Pins 2, 6, and 7 determine astable/monostable operation. Figure 2 shows the 555 set up for astable mode, using R4, R5, and C1. Figure 3 shows the monostable setup, using R4 and C1, and an external down-going trigger pulse on pin 2. In both modes, pin 4 normally goes to V_{CC}; pin 5 is bypassed by C2 for added stability. In either mode, C1 charges through at least R4 toward V_{CC}, but R5 is present only in the astable mode, for which it varies the duty cycle. Figures 2 and 3 also show the outputs from pin 3 in relation to C1's voltage.

In the astable mode, assume that pin 3 is high, C1 is discharged, and Q is off. Now, C1 charges through R4 and R5 toward V_{CC}. When C1's voltage reaches ⅔ V_{CC}, the threshold comparator sets the flip-flop, turning Q on, discharging C1 through R5 until its voltage reaches ⅓ V_{CC}, driving pin 3 low. The trigger comparator resets the flip-flop, turning Q off, driving pin 3 high. This cycle repeats, yielding a rectangular waveform. If R4 is 0 ohm, charging/discharging is only through R5, giving a symmetric square wave. If R4 is greater than 0 ohm, an asymmetric square wave is generated.

In the monostable mode, an external down-going trigger (needed for each cycle) on pin 2 causes the trigger comparator to reset the flip-flop, turning Q off, charging C1 from the saturation voltage of Q (effectively ground) through R4 to ⅔ V_{CC}. The threshold comparator sets the flip-flop, turning Q on, discharging C1, driving pin 3 low, ending the timing pulse.

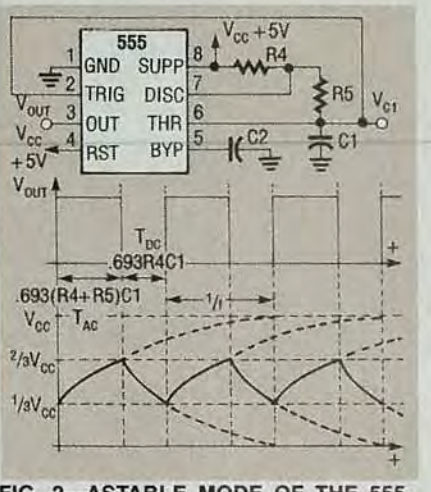

FIG. 2—ASTABLE MODE OF THE 555, showing the relation between the output on pin 3 and C1's voltage on pin 6.

Frequencies and periods

To determine the astable frequency and monostable period, you have to know how C1 charges and discharges. The value of the timing resistors for both the monostable and the astable were selected so that the number of astable pulses is always an exact multiple of 10 times the value of the unknown capacitor. Finally, the trigger monostable is used to start a measurement, latch the count, and reset the meter.

The time constants for the monostables and astable are exact. However, each time an unknown capacitor is tested, variations in battery voltage, temperature, and comparator trigger levels will all contribute to vary the final reading for each trial. That's why you will get slightly different results each time you test the same C_X. For example, when testing a 0.1 μF capacitor, you may get a reading of 0.094 μF the first time and 0.103 μF the second.

The schematic

Looking at Fig. 3, 555 timers are used for the monostables (IC1 and IC2) as well as for the astable (IC3). A 4011 quad NAND gate (IC4) provides gating, inversion, and buffering, and a 74C926 display driver (IC5) is used to drive the 4-digit 7-segment display, DSP1.

Pressing S5 drives pin 3 of IC1 momentarily low, resetting IC5. A delay line (R3–R5 and C3 and C4) increases the rise time of IC1's output pulse, so that the triggering of IC2 is delayed until IC5 is reset. The switch array S1–S3 determines the capacitance range by adjusting the timing parameters of IC2 and IC3. Only one of the three switches in the array can be

charges. Let R_{EFF} be the effective charging/discharging resistance in either mode. In astable mode, R_{EFF} is equal to R4 + R5 when charging, and R_{EFF} is equal to R5 when discharging. The duty cycle in the astable mode must be the ratio of those, or the duty cycle is equal to [(R4 + R5)/R5] × 100%, or equal to [1 + (R4/R5)] × 100%.

In monostable mode, R_{EFF} equals R4 when charging; there is no discharge path. If C1 is discharged and in series with R_{EFF}, with both connected to V_{CC}, C1 charges "exponentially" from ground toward V_{CC}. That basically means that C1's voltage never reaches V_{CC}, but gets very close.

The "time constant" is always: $\tau = R_{EFF} \times C1$, in secsonds. When speaking of a capacitor charging/discharging, one refers to the number of time constants that have elapsed. A capacitor charges to 63.2% of the difference between its initial and target voltages in one τ, and essentially fully charges/discharges to a target voltage within 5τ (99.33%).

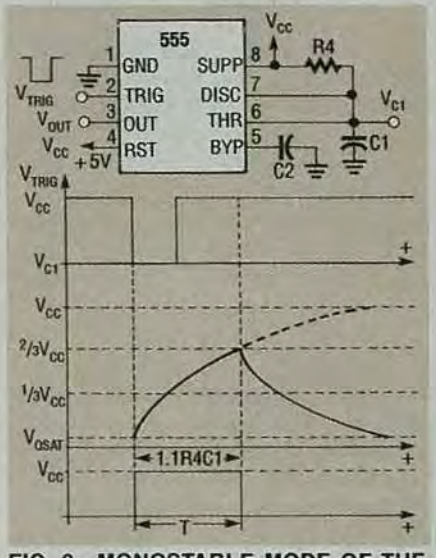

FIG. 3—MONOSTABLE MODE OF THE 555, showing the relation between the output on pin 3 and C1's voltage on pin 6.

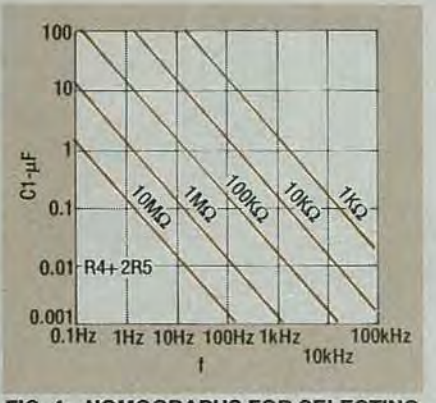

FIG. 4—NOMOGRAPHS FOR SELECTING component values for the 555 timer in the astable mode.

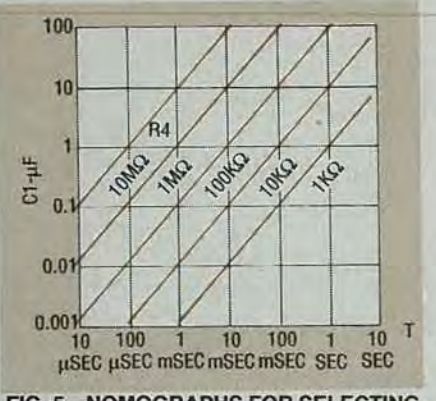

FIG. 5—NOMOGRAPHS FOR SELECTING component values for the 555 timer in the monostable mode.

The voltage divider partitions the charge/discharge cycle so that there are two sets of target voltages; those created by the divider, and those of V_{CC} and ground. The C1 voltage stays between ⅓ and ⅔ of V_{CC} in the astable mode. Since C1 either charges toward V_{CC} or discharges toward ground, the V_{CC}/ground target voltages are never reached in the astable mode, being outside the charging/discharging bounds created by the voltage divider.

The intervals required to reach the voltages due to the voltage divider, both charging and discharging, can be determined exactly. This eliminates the problem that C1 can only charge/discharge arbitrarily close to a target voltage.

In the astable mode, C1 cycles between ⅓ and ⅔ of V_{CC}, always charging/discharging to halfway between an initial and target voltage. When charging, the initial voltage is ⅓ V_{CC} and the target voltage is V_{CC}. When discharging, the initial voltage is ⅔ V_{CC}, and the target voltage is ground.

For C1 to charge/discharge through R_{EFF} from one divider voltage to the other, it always takes:
$T = 0.693 \times \tau = 0.693 \times R_{EFF} \times C1$.
In the astable, the charging interval is:
$T_{AC} = 0.693 \times (R4 + R5) \times C1$.
The discharge interval is:
$T_{AD} = 0.693 \times R5 \times C1$.
The total period is:
$T_A = T_{AC} + T_{AD} = 0.693 \times [R4 + (2 \times R5)] \times C1$
And the frequency is:
$f_A = 1/T_A = 1.44/[R4 + (2 \times R5)]C1$.

In the monostable mode, Q holds C1 at ground. After triggering, C1 charges through R4 to ⅔ V_{CC}. Both the charging cycle and the pulse are now ended by the threshold comparator, as mentioned earlier. For reasons too lengthy to discussin the space we have, pulse duration will be: $T_M = 1.1 \times R4 \times C1$.

Figure 4 is a nomograph of C1 vs. f_A in the astable mode for different values of R4 + (2 × R5). Figure 5 is a nomograph of C1 vs. timing-pulse width T_M in the monostable mode for different values of R4. **R-E**

pressed "in" at any given time, although all three can be "out" at the same time.

Each DPDT switch in the array (S1–S3) has two sets of contacts. To simplify our discussion, we will call the "upper" set of contacts (the set closest to the top of the figure) "a," and the lower set "b" (see Fig. 3). Note that S3 doesn't have to be pushed "in" to serve a function; because of the way in which it is wired, it does affect the circuit in the "out" position.

Switches S1-a, S2-a, and S3-a control the capacitance-measurement range by switching in the appropriate potentiometer—R7, R8, or R9. The potentiometers control the duration of the pulse from IC2, with the ranges as shown in Fig. 3. Switches S1-b and S2-b control which decimal point is selected, and S3-b controls the frequency of the astable 555, IC3. There are two potentiometers used to determine the astable frequencies: R13 and R14. Pressing either S1 or S2 switches R13 into the circuit for both the 999–1-µF and 1–0.001-µF ranges, for an astable frequency of 100 kHz. However, when S3 is pressed, R13 is removed from the circuit, and R14 is switched in for the 1000–1-pF range, for an astable frequency of 10 kHz.

Counter/driver IC5, a 74C926, contains a 4-digit negative-edge-triggered counter, a 4-digit internal output latch, drivers for a 4-digit 7-segment LED display, an internal multiplexer with four outputs, and its own free-running oscillator. A high on pin 13 resets the counter to zero

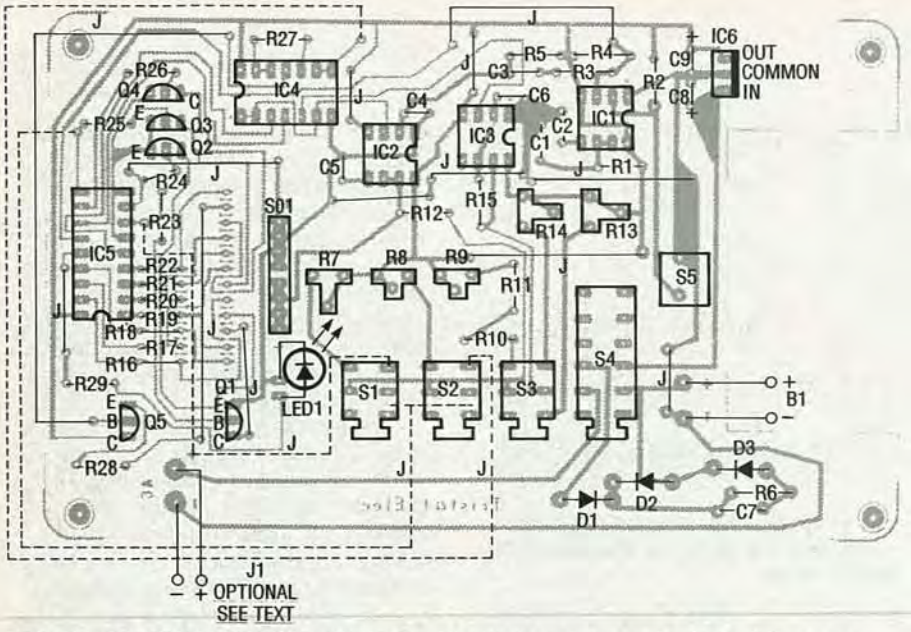

FIG. 4—PARTS PLACEMENT DIAGRAM. The jumpers shown in dashed lines are soldered to the solder lugs on top of the switches.

and drives pin 14 (CARRY OUT) low. A low on pin 5 (LATCH ENABLE) latches the number in the counter using the internal output latches, whereas a high on pin 5 permits a flow-through condition in which the internal latches ignore future counts. A high on pin 6 (DISPLAY SELECT) displays the number in the counter, while a low displays the number in the output latch. In this application, pin 6 is grounded, permanently displaying the contents of the latch, and never the output of the counter.

The pulse from IC2 is positive, and after being NAND'ed (by IC4-b) with the output from IC3, the resulting output in inverted. The down-going pulse from IC4-a enables IC5 to latch the count of the astable pulses within the measurement pulse. Because pin 5 of IC5 goes low during the timing pulse, the new value in the counter is automatically latched each time a count occurs.

The latched count is then converted into the value of the unknown capacitor by shifting the decimal point on DSP1 via transistors Q1–Q5. IC4-c and IC4-d buffer the outputs from the A and C digit drivers of counter/driver IC5, to provide sufficient logic swing for the display. When the counter in IC5 exceeds 9999, pin 14 goes high, lighting the range-overflow indicator, LED1.

Pin 7 of IC5 controls digit A, pin 8 controls B, pin 10 controls C, and pin 11 controls D. Pins 1–4 and 15–17 drive each individual segment of each digit. IC5's internal clock scans the digit-control lines fast enough to avoid display flicker. The decimal point is selected by feeding pin 7 of IC5 (which controls digit A) back to S1-a for the 1–.001 μF range, or pin 10 (which controls digit C) back to S1-b for the 999–1 μF range. The other two decimal points are not used. The display format has no leading-zero blanking or external scaling. Therefore, 100 pF is displayed as 0100, 0.001 μF is displayed as 0.001, and 4.7 μF as 004.7.

Switch S4 supplies power to the 7805 voltage regulator, which provides a steady 5-volts DC to the circuit. If you use a 9-volt battery, you can ignore the optional charger/adapter jack, J1. (Two pads labeled "AC" are provided on the PC board for J1.) A Ni-Cd battery can only be recharged when the meter is on; that's because S4 connects J1 to D1 and the battery to IC6. Charging the Ni-Cd battery pack normally draws about 300 mA, so be sure that whatever you're using can handle that.

PARTS LIST

All resistors are ¼-watt, 5%, unless otherwise indicated.

R1, R8, R12, R16–R22—100 ohms
R2, R4, R5, R27—100,000 ohms
R3—10,000 ohms
R6, R28—560 ohms
R7—1000 ohms, PC-mount potentiometer
R8—250,000 ohms, PC-mount potentiometer
R9—2.5 megohms, PC-mount potentiometer
R10—4.7 megohms
R11—2.2 megohms
R12—7.1 megohms
R13—15,000 ohms, PC-mount potentiometer
R14—150,000 ohms, PC-mount potentiometer
R15—2200 ohms
R23–R26, R29—1000 ohms

Capacitors

C1, C7—0.1 μF, ceramic disc
C2, C3, C5—0.01 μF, ceramic disc
C4, C6—0.001 μF, ceramic disc
C9—1 μF, tantalum electrolytic

Semiconductors

D1–D3—1N4001 rectifier diode
Q1–Q5—2N3904 NPN transistor
IC1–IC3—555 timer IC
IC4—4011 CMOS quad 2-input NAND gate
IC5—74C926 CMOS counter/LED display driver
IC6—7805 5-volt regulator
DSP1—NSB5881 4-digit 7-segment LED display
LED1—red light-emitting diode

Other components

SO1, SO2—8-pin SIP wirewrap socket
PL1—8-pin SIP plug
S1–S3—board-mounted 3-pushbutton DPDT switch array, 3/16-inch lead spacing, with PC-contact pins and solder lugs for wires
S4—board-mounted pushbutton 4P2T switch, 3/16-inch lead spacing, with PC-contact pins and solder lugs for wires
S5—board-mounted momentary pushbutton, 5/16-inch lead spacing
B1—9-volt alkaline battery or optional 7.2-volt rechargeable Ni-Cd (see text)
J1—subminiature jack matching the plug of the charger/adapter (optional, see text)
T1—optional charger/adapter, 117/12-volts AC, 300 mA

Miscellaneous: Pacifitec Model HPL-000 project case, 9-volt battery clip, LED bezel, solder, wire, etc.

NOTE: The switches for the prototype were obtained from Active Surplus Annex, 347 Queen Street West, Toronto, Ont., Canada, (416) 593-0967. A kit of all parts except resistors, capacitors, and PC board is available for $39.95, plus $5.00 shipping and handling. A PC board is available for $12.00. Contact Tristat Electronics, 66A Brockington Crescent, NEPEAN, Ont., Canada K2C 5L1.

Construction

The Parts-Placement diagram is shown in Fig. 4, and a foil pattern is provided in PC Service. Before soldering, it's a good idea to clean the foil side of the board with steel wool to remove oxides; that ensures a smooth solder flow. Use sockets for the IC's and various transistors.

Figure 5 shows how to make the test socket, SO1, and its corresponding plug, PL1. SO1 is made from an 8-pin SIP wirewrap socket, and PL1 from an 8-pin SIP plug; the two are connected by a twisted pair. SO1 is epoxied into its opening in the case, and PL1 fits into SO2.

The display is connected to the PC board using 2 inches of No. 12 ribbon cable. Solder one side to the display and the other side to the PC board. (Be certain that pin 1 of the display goes to pad 1 on the PC board.) Only solder pins 1, 3, 4, 7, 8, and 10–16 of the display—the others are not used.

Solder LED1 approximately ¾ of an inch above the PC board, so that its top is flush with the case. You can use a mounting bezel for LED1.

Figure 6 is a photograph of the prototype meter. Study Figs. 3, 5, and 7 for the relationship of all components to one another, as well as the position of all components. Note that the 7805 is bent flat for case clearance, with its metallic side facing upward.

If you decide to use Ni-Cd batteries, the most convenient way to install the charging jack (J1) is to drill a hole in the meter case near the "AC" pads on the PC board. (Drill slowly to prevent damaging the plastic.) It's up to you to choose the type of jack for J1; it must, however, match the plug of the charger/adapter, and be small enough to fit in the case.

Before installing the IC's or transistors in their sockets, apply power to the board and check for correct voltages. Then, shut off the power, insert the IC's and transistors, and turn the meter on again; the display should now show a random 4-digit number. If not, turn the meter off and check the wiring, looking particularly for a short in the display foils.

Exact calibration

To calibrate the meter, you should use an oscilloscope or frequency counter, and one precision unknown capacitor for each range. Connect the oscilloscope or frequency counter between pin 3 of IC3 and ground. Then

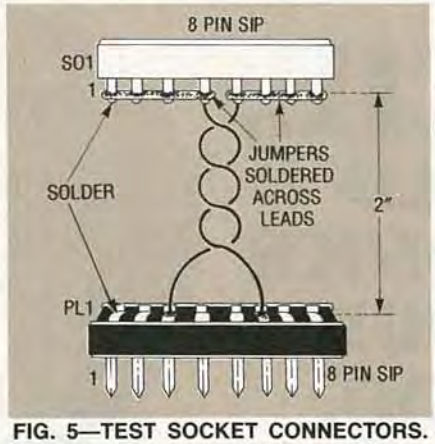

FIG. 5—TEST SOCKET CONNECTORS. This assembly connects the capacitor under test to the PC board's test socket.

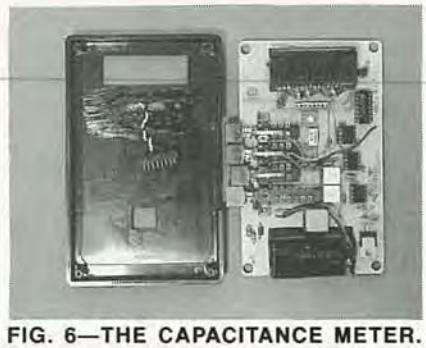

FIG. 6—THE CAPACITANCE METER. Notice how the various parts are oriented.

press either S1 or S2 and adjust R13 for 10 kHz. Now press S3 and adjust R14 for a reading of 100 kHz. If you've got precision capacitors, insert a suitable one for the 999–1 μF range, press S5, and adjust R7 until the display reads the nominal value.

Without precision unknown capacitors, use an iterative (repetitive) approach. Use three or four nonprecision capacitors for each range, of the same nominal value. For the 999–1 μF range, test an unknown capacitor at random, adjusting R7 until C_X's nominal value appears on the display, and then set the capacitor aside. Next, without adjusting R7, test and record the other unknowns for that range, and average the results.

Now, using the first unknown capacitor tested (the one set aside), adjust R7 so that the meter shows your average value, rather than the nominal value. Without adjusting R7, test the other unknowns and average the new values. Now, let the first unknown in the new average have the first average value that you came up with. Repeat until the average value no longer changes much. The accuracy of the meter will increase with the number of unknowns tested per range, and the number of iterations. Repeat the procedures for the other two ranges, adjusting R9 for the 1–0.001-μF range, and R11 for the 1000–1-pF range.

Approximate calibration

Without proper gear, you can get good but not perfect calibration. Use a nominal value of capacitor suitable for each range as an unknown, and set all potentiometers to mid-point. Select a range, and insert a suitable unknown capacitor. Don't vary R7 or R9; adjust R11, R13, or R14 until the nominal value of the capacitor being tested appears on the display. Set the first unknown aside, and repeat the procedure, sampling the other identical nominal value capacitors for this range without varying any of the potentiometers at this point, and average the display values. Using the first nominal-value capacitor tested, readjust R11, R13, or R14 for the first average value. Repeat the procedures for the other ranges.

Using the meter

Once calibrated, plug PL1 into SO2 on the PC board, and put the meter in its case. A polyethylene faceplate was epoxied to the prototype's case, but the front-panel design for your meter is up to you.

The meter's stray capacitance is about 30 pF, and can't be zeroed on the pF range. If you press S5 with no capacitor attached, while in the pF range, the meter should read about 30 pF. The stray capacitance is in parallel with the unknown, so it must be subtracted from any pF-range reading.

When testing a capacitor, watch LED1 to get higher precision on the two lower ranges. For a nominal value of 0.01 μF, the meter might read 0.010467 μF, in which case the pF range would overflow; the number of LED1 flashes gives the overflow digit. On the 1–0.001-μF scale, the nominal 0.01-μF capacitor might read 0.011. On the pF range, LED1 should flash once since the counter passed 9999 once; the display should read 0467. However, LED1 flashes rapidly, and is hard to count.

If LED1 flashes once, that means an overflow digit of one; then, C_X is 10,467 pF or 0.010467 μF. If LED1 flashes twice, the reading would be 20467 pF, etc. Note that holding S5 down doesn't increase accuracy, It just wastes current by repetitively testing a capacitor, and will prevent a reading from being displayed. **R-E**