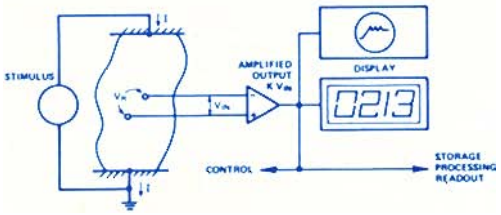
VOLTAGE MEASUREMENTS IN BIOMEDICAL RESEARCH

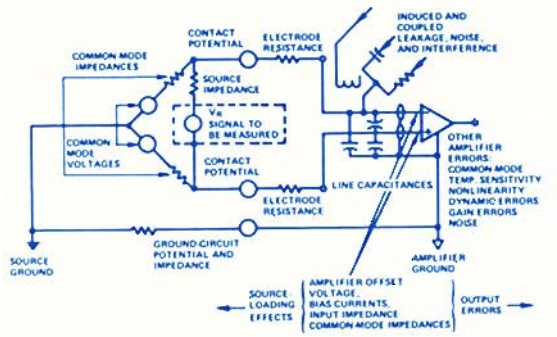
HOW FET-INPUT IC OP AMPS CAN HELP—A BRIEF SUMMARY

by Rich Frantz

The problem is easily stated but wicked to solve: One must measure a (small) voltage occurring between two points in an entity under test safely and with reasonable accuracy and fidelity (Figure 1a). Why it is difficult can be seen in 1b. The sources of trouble are threefold: the entity itself (including the measurement electrodes), the amplifier that acquires and processes the measurement, and their interconnection (and interaction).



a) Typical bioelectric measurement



b) Sources of noise and errors

Figure 1. Ideal measurement and the arrayed opposition

The entity. First of all, the voltage to be measured may be inaccessible to direct measurement; or the act of measuring it may introduce significant errors (such as contact potentials), or it may even change or destroy the entity if too large an energy flow (either in or out) occurs. The first two of these considerations are in the province of the design of the experiment itself; the third can usually be ameliorated by proper electronic design and choice of circuitry. In addition, there will be a number of traditional electrical characteristics of the circuit that affect measurement accuracy, compounded by the differential nature of the measurement (since there aren't too many entities in Nature that are so obliging as to have a terminal at ground potential). These include: source impedance, common-mode impedances, and common-mode voltages and currents (such as line-frequency and radio-frequency pickup).

The Amplifier. Faithful readers of these pages and others, such as the *Analog-Digital Conversion Handbook*[1] (see page 23), have been well-exposed to the foibles of nonideal amplifiers and the comparative merits of isolation amplifiers, differential-instrumentation amplifiers, and op amps in subtractor configurations. Relevant sources of error include the amplifier's offset voltage and bias currents (and their variations with time, temperature, and supply voltage), amplifier voltage- and current-noise, input impedance (the raw amplifier and/or the associated circuitry), common-mode voltage error and impedances, bandwidth limitations (both differential and common-mode). Equally important considerations in these days of shrinking budgets are device costs; fortunately, integrated-circuit productivity tends to be counter-inflationary, and a respectable-performance differential amplifier can be constructed from low-cost IC FET-input op amps, such as the AD503K or the AD514L.*

Interconnection. The problems that arise here include induced noise and interference, ground loops, common-mode and scale-factor errors due to loading, offset errors due to the flow of bias currents through source resistances, attenuation of high-frequency signals due to capacitive loading, and ac common-mode errors due to asymmetrical capacitive loading. In addition to the *errors* caused by contact potentials and their variation, such offset voltages may be considerably larger than the signals that "ride" on them and require continuous long-term nulling or ac coupling to avoid overranging the amplifier. Dangers to the entity under test may be posed by: differences in ground potential, dissipation due to bias current flow through the source resistance, capacitive coupling from the power line, and potentials or currents imposed by component or system failures, or potential differences in the "power-off" mode.

CHOOSING AN APPROACH

Space limitations prohibit completely satisfactory treatment. However, having raised the questions that would lead the designer to consider salient elements of the problem, we can now suggest a few elements of solution that are known to be effective.

Isolation. For extreme "hard cases" where the entity under test involves living tissue, which must be protected in a "fail-safe" manner, and where some performance compromise is possible in terms of noise and bandwidth, an isolation amplifier (model 273, or some newer designs)†, may be considered.

Instrumentation Amplifiers. Depending on the characteristics of the source and the required performance, instrumentation amplifiers are available for use, essentially as "subtractors-with-gain."§ As a rule, they are designed to minimize cost, voltage drift, and/or common-mode error. It is hard to find an amplifier that combines all of these features *and* the high input impedance and low bias current of FET-input amplifiers.

Instrumentation-Amplifier Configurations. Where the high input-impedance and low bias-current of FET's are essential to minimize loading of the source, a proven configuration that can utilize low-cost FET-input op amps is shown in Figure 2.

[1] Still in print and available at $3.95 from Analog Devices, Inc., P.O. Box 796, Norwood, Mass. 02062, U.S.A.

*For information on these amplifiers, request **M2** and **M5**.

†For information on the 273 and other isolation amplifiers, request **M18**.

§For information on the AD520, 602, 603, and 605 instrumentation amplifiers, request **M19**.

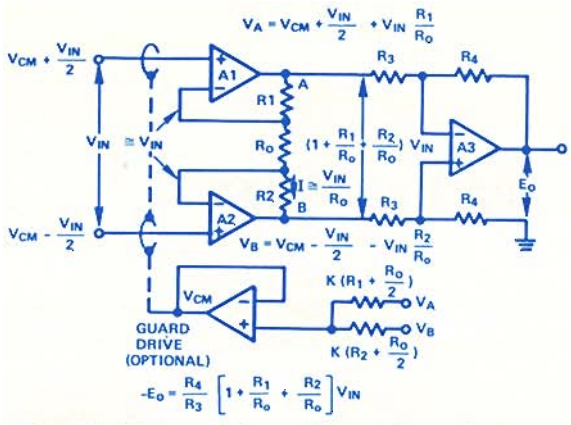


Figure 2. Differential-amplifier configuration

How it works: Since the voltages appearing at the positive inputs of A1 and A2 must be duplicated at the negative inputs, the current through R0 is determined by the difference voltage, V_{IN}, which is magnified by the sum of the resistance ratios, to appear as the difference voltage $V_A - V_B$. Since the common-mode level is the same as the input common-mode level, current to flow through R0; therefore the output common-mode level is the same as the input common-mode level. This relative reduction of the common-mode level eases the task of stage A3 (shown as a simple subtractor-with-gain) to bring the differential output of the first stage "down to earth," i.e., to system ground. The common-mode rejection of the second stage is theoretically infinite, but it is affected by the resistance-ratio match and the amplifier characteristics. However, the common-mode error in the A3 stage is reduced (relative to the input) by the gain of the first stage.

First-stage common-mode errors can be minimized (a) by choosing amplifiers with low error contributions and/or (b) by matching their errors in polarity (and magnitude), and mounting them isothermally, so that the errors become common-mode signals, rather than difference signals. Figure 2 includes a guard-drive circuit that can minimize pickup and capacitive loading on the source. FET-input op amps can minimize amplifier loading on the source and voltage drops in the source impedance due to amplifier bias current. Circuit-board leakage, especially to the supply leads ($15V/10^{11}\Omega$ = 150pA!) should be reduced by the use of guarding and Teflon standoffs. Since bias current of FET input transistors doubles with each 10°C increase of temperature, the amplifiers should be kept cool by the use of heat sinks (such as Wakefield 205 or 209), and decreased supply-voltage. ▶▶▶

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A LOW-NOISE FET-INPUT IC OP AMP

is usually proportional to 1/f, though, more generally, it often fits a $1/f^{\alpha}$ relationship. It is thought to be due to imperfect surface conditions on transistors and integrated circuits, in carbon composition resistors, etc. In bipolar transistors, a correlation has been established between excessively-large amounts of 1/f noise and unreliability. In some transistors, "popcorn" noise exists; it is an erratic jitter between two values of h_{fe}, causing additional base-current noise, consisting of a shift at random intervals between two values of base current. It is unacceptable in a low-noise amplifier.

SPECIFYING AND MEASURING THE AD514

As with modular low-noise amplifiers, such as the model 52 (see page 10), noise in the 1/f region is usually measured in terms of its peak-to-peak value, for a number of reasons: first, peak-to-peak noise is the important variety in many low-frequency applications, second, it permits inspection of a large number of individual noise values in a short period of time, whereas an rms measurement provides a single average number, with little qualitative or quantitative regard for what the actual waveform might be like. Finally, it permits a rough estimate of the general order of magnitude of the rms voltage. Unlike sample testing in the laboratory, the quantities of low-cost IC's that must be tested on-line in a relatively-short time preclude the possibility of using chart recorders for unhurried examination of noise waveforms over lengthy periods in a quiet environment (if the environment is not quiet, the peak that causes an amplifier to "fail" may be an artifact caused by interference). Since most other tests on IC operational amplifiers are performed in milliseconds, it may be evident that, in order to keep the cost at a minimum, the time allowed for noise testing has to be kept to a matter of seconds.

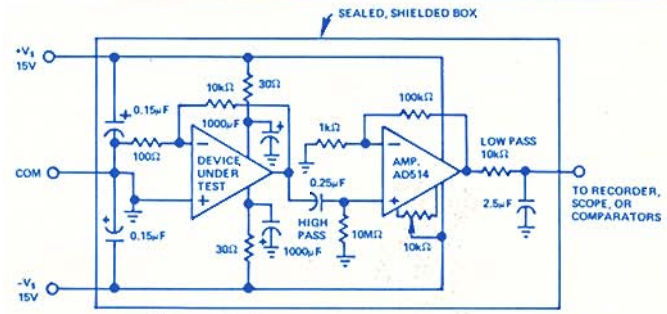

Figure 3. Test circuit for AD514

The amplifier under test is inserted into the circuit of Figure 3, in a closed, shielded box, protected (as well as possible) from both electrical noise and random air currents (they can introduce drift error, which is indistinguishable from low-frequency noise), and allowed to warm up for 30 seconds. The output of the circuit is then observed electrically, using biased comparators and logic. If, in two-out-of-three 10-second intervals, the specified maximum value of peak-to-peak noise has not been exceeded, the device is deemed to have passed the noise test.

An oscilloscope may also be used for observation, but one should use high intensity, careful attention, and an increased number of observations. If the test occurs in an electrically-noisy environment, great care should be taken to avoid picking up interference noise, since there may be no practical way of knowing whether a single excessive spike is an artifact or a true random event.

The test circuit consists of two stages of amplification, one of which is inherently provided by the device under test. The post-amplifier also has a high-pass and a low-pass filter, which together determine the test bandwidth (100:1, or 2 decades in the 1/f region). For frequencies as low as 0.5Hz, this procedure will have sampled more than 10 cycles, and for frequencies down to 0.1Hz, 2 or more cycles. ▶▶▶