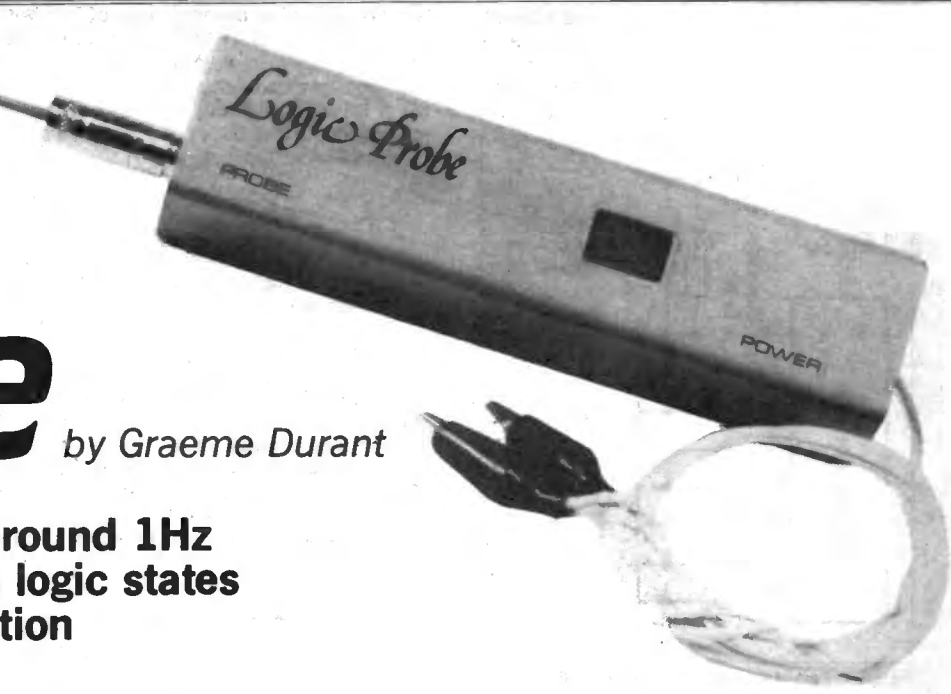
Logic Probe

by Graeme Durant

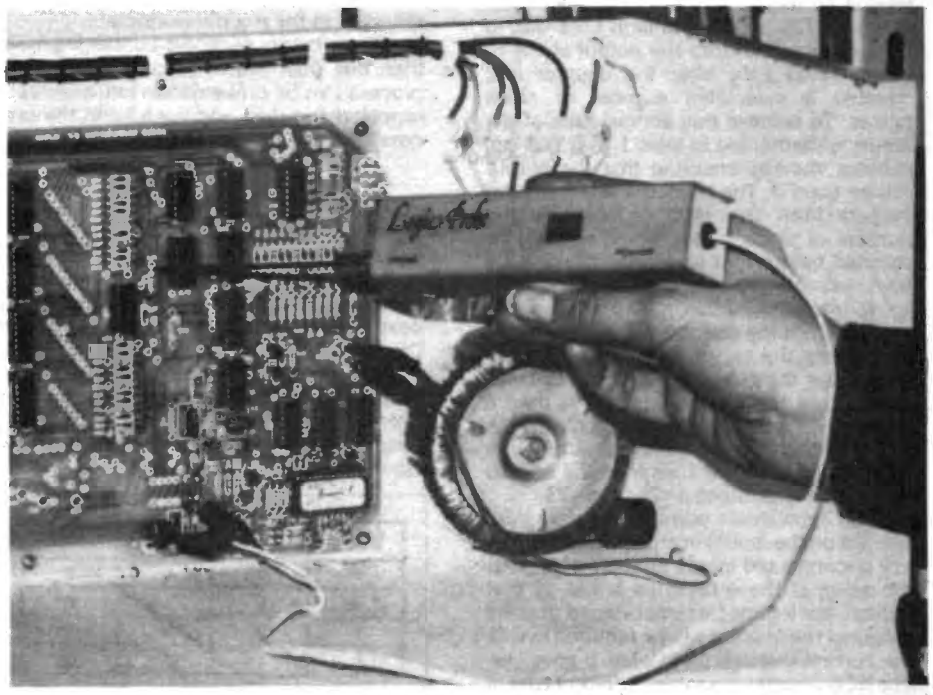


- ★ **Detects pulses from around 1Hz**
- ★ **Instantly recognisable logic states**
- ★ **Low current consumption**
- ★ **Over volts protection**

Over the years, countless designs have appeared in the electronics press for logic probes; ranging from very simple High/Low indicators, to complex pulse stretching probes. The logic probe described here, has a number of features found only on the more complex probes, and as such, lies somewhere between these two extremes. Thus it is perfectly suited to day to day fault diagnosis.

As well as detecting High and Low logic states, open circuit (floating input) and pulsing inputs are displayed. Pulse trains from around 1Hz are detected as a pulsing input, the upper limit is above that attainable in most common C-MOS logic.

The main difference between this logic probe and all others is that the output is shown on a seven segment LED display, as a letter of the alphabet; Hi for High; L for Low; F for Floating; P for Pulsing. In this way, the logic state is instantly recognisable and totally unambiguous, unlike some commercial logic displays. The use of a special high efficiency display means that the total current consumption at a supply voltage of 15v is only 15mA - quite suited to battery operated circuits. In addition, the probe is protected against overvoltage inputs, and reversed supply.



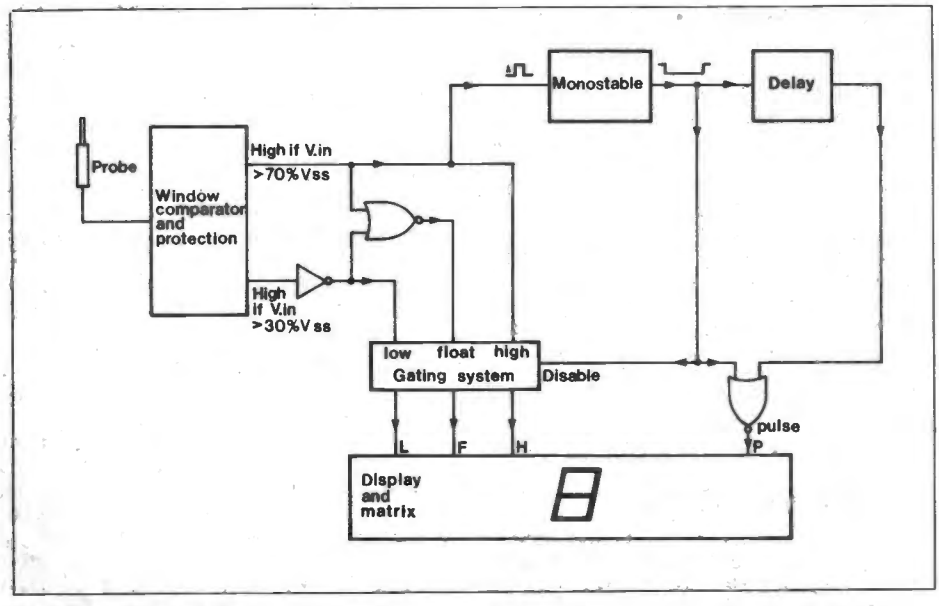


Figure 1. Block diagram.

Block Diagram

The input from the probe goes via a protection network to a window comparator, with switching levels of 70% Vss and 30% Vss; these are the standard CMOS limits. If the upper limit is exceeded, then the probe input is CMOS logic high. Thus, the upper output goes on to the display circuitry for HIGH indication.

If the probe input does not exceed the lower limit, then it is at CMOS logic low. The output of the lower comparator is inverted to give a high level at the display circuitry for LOW indication. If the probe input is between logic levels,

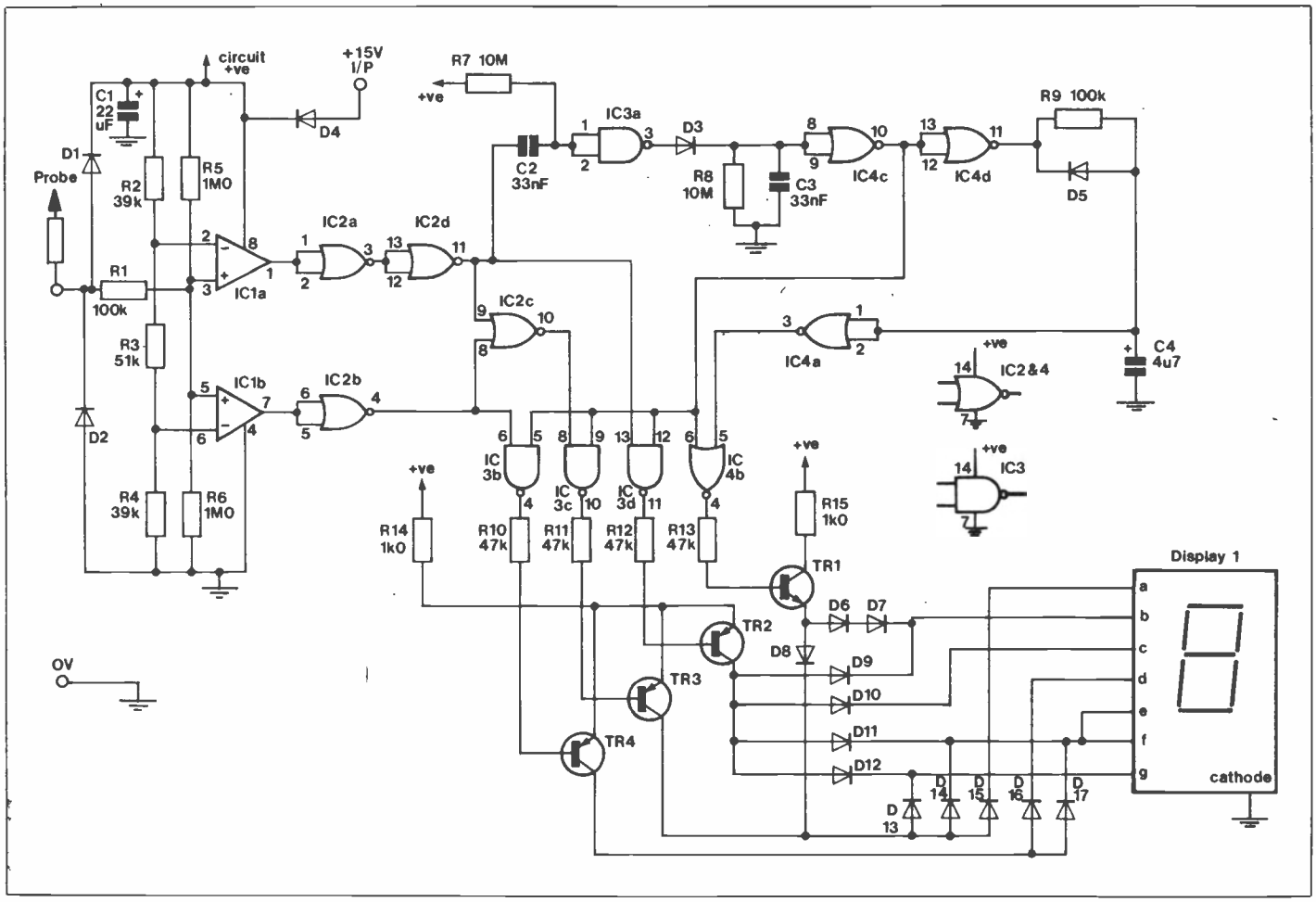
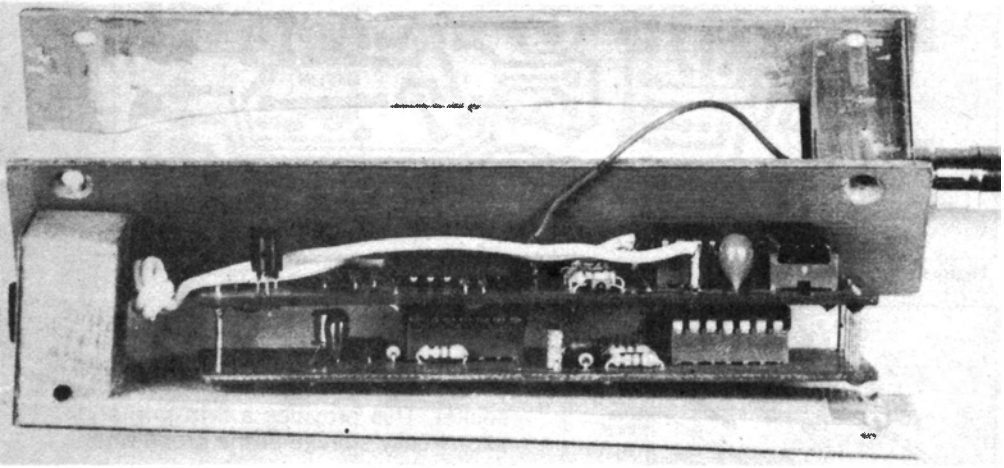


Figure 2. Circuit diagram.



then the upper comparator will be low and the lower comparator high. These two outputs are fed to a NOR gate, which gives a high level to the display circuitry on FLOAT.

The HIGH indication also drives a retriggerable monostable. will produce a continuous low output. If this monostable goes low, the display is disabled via a simple gating system. This is to prevent misleading displays, whilst the circuit decides whether the input is indeed pulsing, or whether a low to high transition has taken place (e.g. the probe has just touched a point at logic high). As soon as a low pulse appears at the monostable output, a delay, slightly

PARTS LIST FOR LOGIC PROBE

Resistors: All 0.4W 1% metal film unless specified

R1,9	100k	2 off	(M100K)
R2,4	39k	2 off	(M39K)
R3	51k		(M51K)
R5,6	1MO	2 off	(M1MO)
R7,8	10M	2 off	(B10M)
R10-13	47k	4 off	(M47K)
R14, 15	1kO	2 off	(M1KO)

Capacitors

C1	22uF 25V Tantalum		(WW73Q)
C2, 3	33nF polycarbonate	2 off	(WW35Q)
C4	4u7F 35V Tantalum		(WW65V)

Semiconductors

IC1	CA3240E		(WQ21X)
IC2, 4	4001BE	2 off	(QX01B)
IC3	4011BE		(QX05F)
TR1	BC107B		(QB31J)
TR2, 3,4	BC557	3 off	(QQ16S)
D1, 2	BAR28	2 off	(QQ13P)
D4	1N4001		(QL73Q)
D3, 5-17	1N 4148	14 off	(QL80B)
Disp.1	Low current disp.		(QY54J)

Miscellaneous

Printed circuit board (top)		(GB30H)
Printed circuit board (bottom)		(GB31J)

Additional parts if required

8pin DIL skt		(BL17T)
14pin DIL skt	3 off	(BL18U)
Screened phono plug		(HH01B)
Threaded phono skt		(YW06G)
Croc. clips		(HF25C)
Zip wire	1 metre	(XR39N)
Filter red		(FR34M)
Veropin 2141	1 pkt	(FL21X)

A complete kit of all parts is available. Order As LK13P (Logic Probe Kit). Price £9.95.

longer than the monostable period is initiated. At the end of this time period, if the output of the monostable is still low, i.e. the input is pulsing, the display shows PULSE. Otherwise, the HIGH/FLOAT/LOW display is enabled again.

The display consists of driver transistors, a diode matrix to produce the desired alphabetic displays, and a seven segment LED display.

Circuit Description

The probe input goes via R1 to a simple window comparator formed around IC1. R2, R3 and R4 determine the changeover voltage levels. The circuit input is protected from overvoltage by D1, D2 and R1; the input is biased at half supply by R5 and R6 so that if the input is open circuit, the display shows FLOAT. The upper window comparator output is buffered by IC2a and IC2d, and goes to the display switching transistor for HIGH indication, via IC3d, which allows the HIGH display to be disabled.

The low and float displays are similarly connected, using IC2b and IC3b for LOW, and IC2c and IC2c and IC3c for FLOAT.

A simple CMOS monostable wired around IC3a and IC4c, and having a period of around 0.5 seconds senses a pulsing input. Its output, which is normally high, disables the HIGH/FLOAT/LOW display, and starts a delay, formed around C4 and R9, which is a little over the monostable period. The output of the RC delay is inverted and fed to IC4b, which senses whether the input is still pulsing. If it is, Q1 is switched on, and PULSE is displayed. Otherwise Q2 to 4 are enabled, A diode matrix and seven segment common cathode display decode the signals, so as to give H, F, L and P displays.

'Construction'

Before soldering in any components, solder in wire links on both PCBs, there are eight in all. Fit in all the resistors and capacitors, taking care with polarity on C1 and C4. If you are using IC sockets these may be fitted along with the diodes — again be careful about polarity. Note also, that D4 is fitted vertically on the PCB. Fit the transistors, and finally, the ICs. It is a good idea to use veropins for all the cable to PCB connections, but it is not vital. This only leaves the display, which requires setting at the correct height to fit inside a suitable case.

The PCBs are mounted one on top of the other in the case, with connections between made by solid wire links - cropped component leads are ideal. Solder eleven lengths of wire, about 20mm long, to the underside end connections of the top board, passing the wire through the holes until level with the topside of the PCB. See Figure 5.

Slide on the lower board, until there is a gap of a millimetre or so between the top board and the tallest components on the bottom PCB. Solder the wires to the bottom board and crop as normal.

The circuit now may be fitted into the case, insulated from the case bottom by masking tape and held firmly in position by sticking a strip of thin foam rubber in the lid, with a cutout for the display. A small square of red display filter film may be stuck behind the cutout for the display for easier viewing.

The power cable, a piece of Zip wire terminated in crocodile clips must pass through the case via grommet. The probe, made from a sharpened steel rod or knitting needle, is soldered into a Phono plug, and connected to the circuit by a case mounted Phono socket. This provides a firm grip and allows easy storage of the probe when not in use.

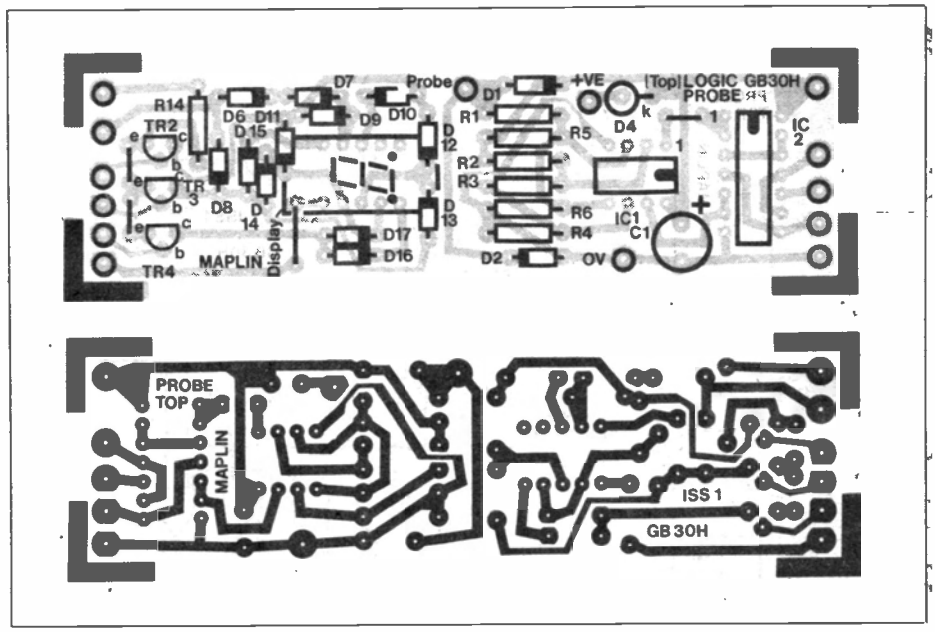


Figure 3. PCB layout.

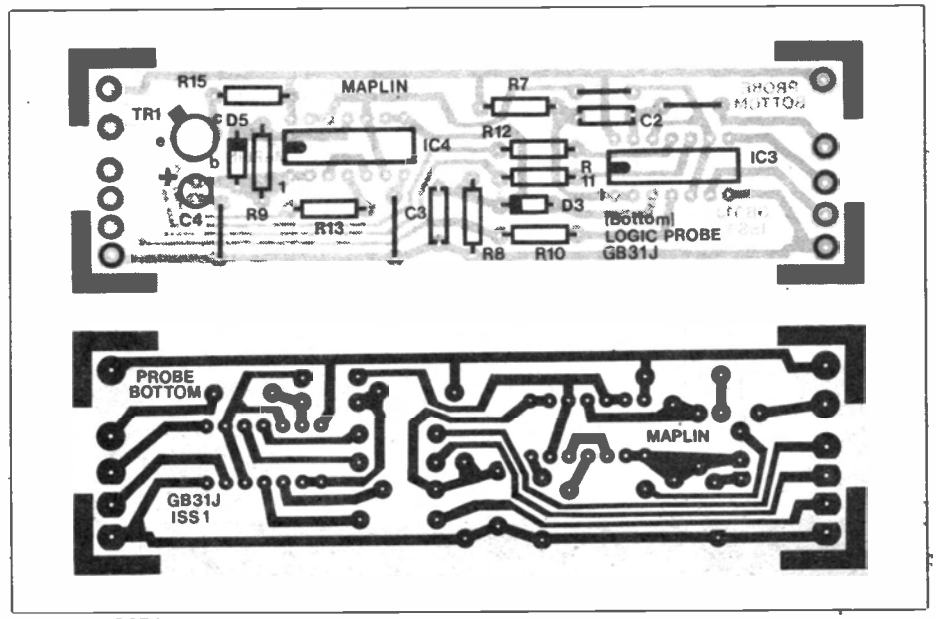


Figure 4. PCB layout.

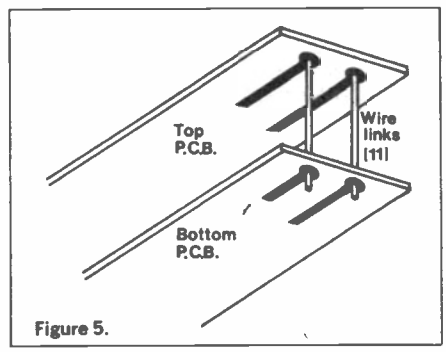


Figure 5.

Testing and Use

Power the circuit up with a typical CMOS supply voltage. After around half a second, the display should show a letter F. If not, disconnect quickly, and recheck the circuit. If all is well, touch the probe to positive - a letter H should be light after a brief delay. Tap the probe on and off positive a few times a second - a letter P should be displayed after a delay. Then, touch the probe to Ov - a letter L should light immediately. If all this happens, the probe is working perfectly.

The probe is designed for use with CMOS logic circuitry, and may be used to trace faults on any such logic. All that remains now is to find a suitable circuit to test!