Bill Vergona
3504 Taylor Avenue
North Las Vegas NV 89030

You Still Haven't Built a Logic Probe? — try this one

Many people who get involved in home computer systems or any other form of digital electronics at one time or another run into hardware problems. If you want to fix them yourself, you need some way to look at what's going on inside the logic.

Usually, if you want to see logic levels, you might use a simple logic probe or a high-impedence FET (Field-Effect Transistor) volt ohmmeter (VOM). If you want to see a timing relationship, you need a triggered sweep oscilloscope to see the actual timing relationship of two different pulses or signals.

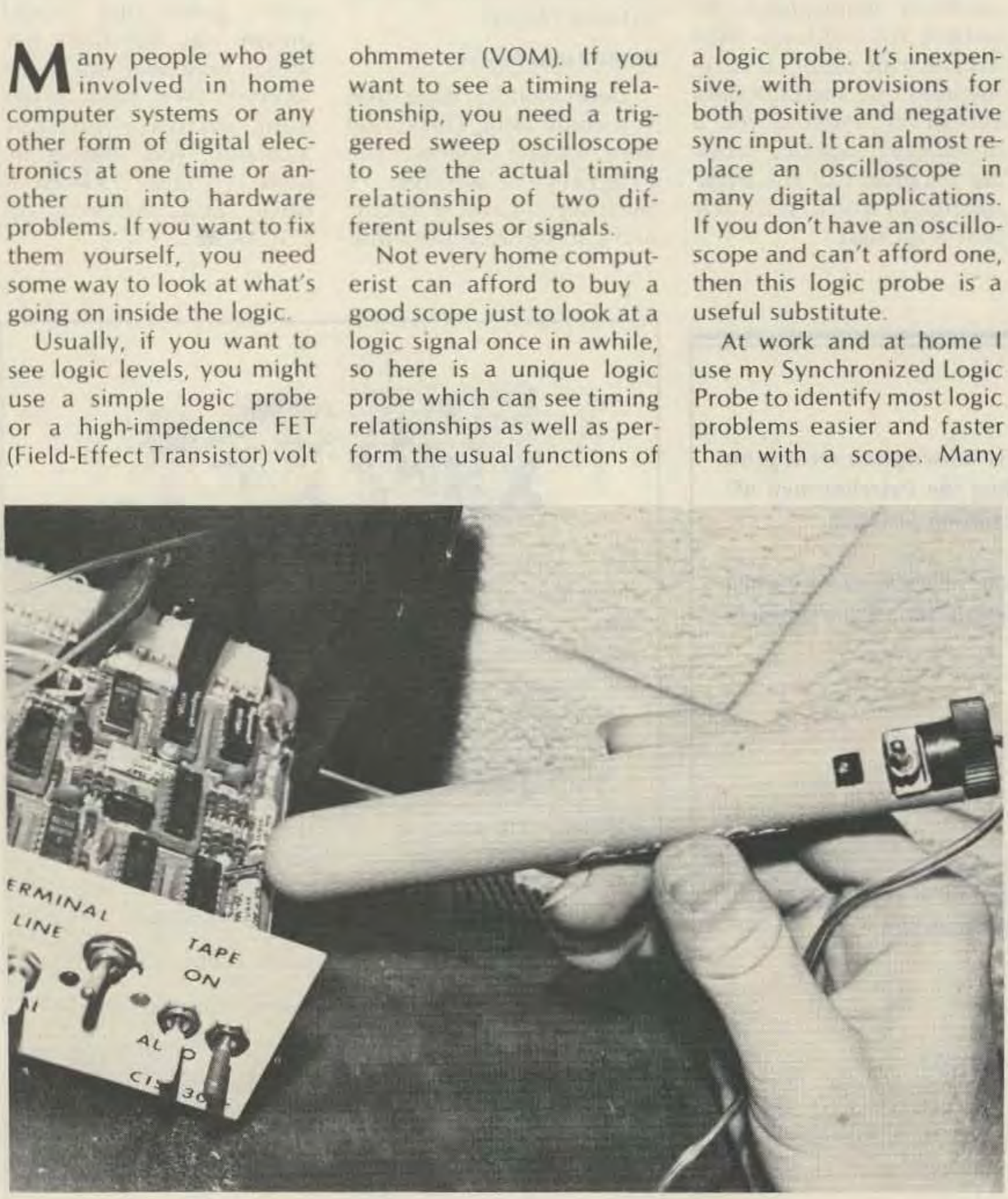
Not every home computerist can afford to buy a good scope just to look at a logic signal once in awhile, so here is a unique logic probe which can see timing relationships as well as perform the usual functions of a logic probe. It's inexpensive, with provisions for both positive and negative sync input. It can almost replace an oscilloscope in many digital applications. If you don't have an oscilloscope and can't afford one, then this logic probe is a useful substitute.

At work and at home I use my Synchronized Logic Probe to identify most logic problems easier and faster than with a scope. Many times it's too much trouble to pull out the scope, so I use this probe instead. My probe also has features missing in an oscilloscope. Did you ever try to see an 18-ns pulse on a scope when it only happens about once every 5 or 10 seconds? With a scope, such a pulse is invisible, but using a probe which stretches the pulse enables it to be seen.

This logic probe will display a P for approximately 0.75 seconds every time a pulse occurs. It also displays standard logic levels like L for a low (false), H for a high (true), and an F for a float (open). Not only that, you can synchronize it to one signal and see if another signal happens at the leading or trailing edge of the sync input. One of the nicest points about this logic probe is that you can build it for about seven dollars.

How does this work? See the schematic, Fig. 1, and the timing diagram, Fig. 2. Under all conditions, segments E and F are always enabled via the +5-volt power bus forming the left-hand vertical bar of P, L, H, or F. The first condition discussed will be the static or no-signal condition.

At this time, the probe tip



The completed Synchronized Logic Probe in action. Custom case is a cigar tube.

is connected to neither a ground nor a true value. Pin 1 of IC1A is floating (true in TTL) and pin 2 is connected to a true (Vcc) through S1 and J1 (Sync input), giving a false output of IC1A. Pin 13 of IC1D is at ground potential through R6, and pin 12 of IC1D is also true through S1 and J1, so the output of pin 11 is true. The false output of IC1A is applied to both inputs of IC1B, making its output true.

This true is applied to one input, pin 9, of IC1C. The other input, pin 10, also is true from the output of IC1D, so now IC1C has an output which is false. This false is applied to input pin 12 of IC2D. The other input is tied to the $\overline{Q}$ output of the one-shot, IC4, which is statically true. The output of IC2D is logic true, which causes segment A of the display to be lit. To complete an F, we need to light segment G and make sure segments B, C, and D are off.

Pin 9 of IC2C is true from the output of IC1D and pin 10 of IC2C is true from the one-shot, making its output false and thus keeping segment B off. Pin 3 of inverter IC3B is true from IC1, making its output false, which, when applied to IC2B, makes its output true.

This output is inverted again through IC3C and makes segment C false, thus keeping its segment off. Pin 1 of IC2A is false from IC1A, making its output true and lighting segment G; this output is also inverted by IC3D, keeping segment D off. Thus, segments A, E, F, and G are lit while B, C, and D are off, giving a display of F (float).

Now that we have seen the float condition and the basic operation, I am going to explain the logic true or high condition. When a logic true is present at the probe tip, it is applied to pin 1 of IC1A, making its output false. This false output is

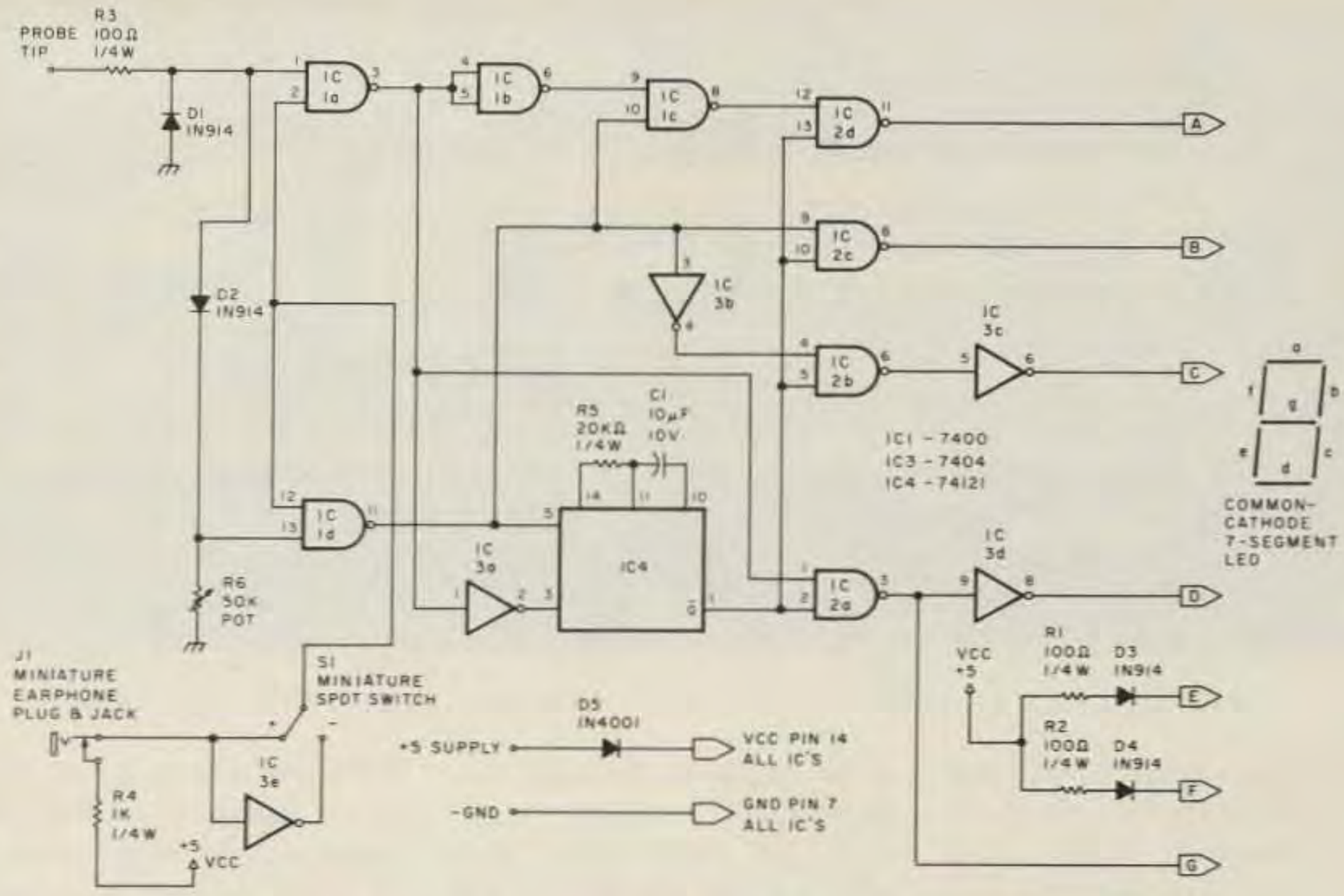


Fig. 1. Schematic diagram of the Synchronized Logic Probe.

applied to both inputs of IC1B, making its output true, which is then applied to pin 9 of IC1C.

The probe tip input is also applied to pin 13 of IC1D, making its output false and this being the other input to IC1C, thus makes its output true. This true which is applied to one input of IC2D along with a true on the other input from the $\overline{Q}$ output of the one-shot makes the output of IC2D false, which turns segment A off. Pin 9 of IC2C is false from IC1D, making its output true and lighting segment B. Pin 4 of IC2B is true from the inverted output of IC1D, making the output of IC2B false, which is inverted by IC3E, lighting segment C. Pin 1 of IC2A is false from the output of IC1A making the output of IC2A true, which is used to light segment G and is also inverted by IC3D which keeps segment D off. Now we have segments B, C, and G lit, while segments A and D are off. Remember that segments E and F are always on and thus the display of H for a static true.

As for the low condition, all segment outputs are opposite except for segment

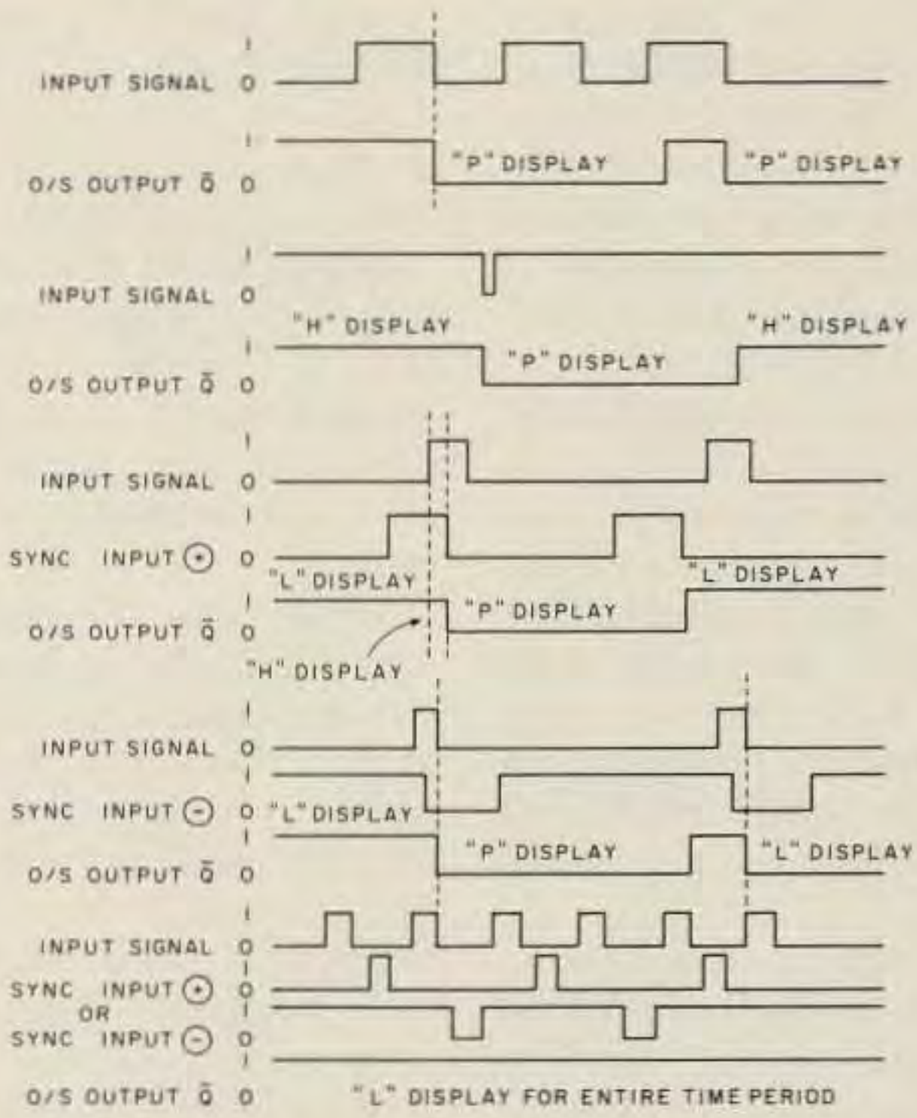
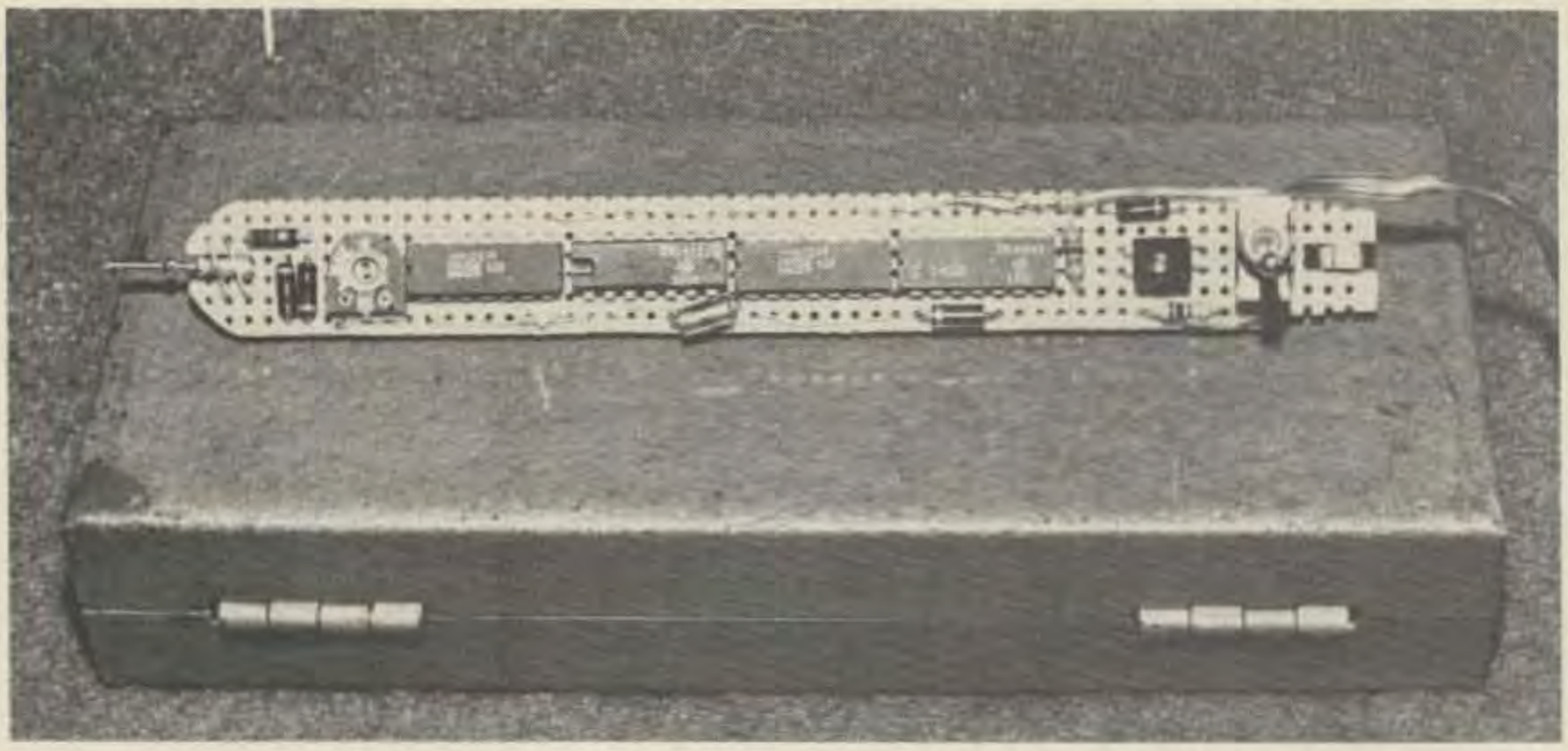


Fig. 2. Timing diagram for logic probe.

A, which remains off. Pin 1 of IC1A goes false, making its output true. This is inverted by IC1B, so a false is applied to pin 9 of IC1C along with a true from the output of IC1D. This makes the output of IC1C true. This is then applied to pin 12 of IC2D, along with a true from the $\overline{Q}$ output of IC4, which makes the IC2D output false. This keeps segment A off.

A note about the low condition: When you first apply the probe tip to a logic false signal, the changing state of IC1A through IC3A triggers the one-shot, making the $\overline{Q}$ output false. This, in turn, enables segments A, B, and G regardless of the other inputs and also disables segments C and D, thus displaying a P for approximately .75 seconds before going to an L display. This can be viewed as a self-checking way to see if



Components are mounted on 0.1" perfboard shaped to fit inside cigar tube.

the pulse circuit is working. Whenever there is a high-to-low transition at the input of IC1A, the one-shot will be triggered and a P will be displayed until a constant state is reached. This covers the generation of the H, L, P, and F display conditions. Note that the length of the P display can be changed by varying R5 and/or C1.

This brings us to the operation of the sync input. Under normal conditions (not using sync), switch S1 is kept in the positive (+) position, thus applying a logic true to one input of IC1A and IC1D. When the sync-pulse input is used, the logic true is disconnected from the switch input and replaced by the sync-input signal.

First the positive sync input will be discussed. When using the positive sync input, this means that we are looking for a signal at the probe tip which is either occurring at the leading edge (low-to-high transition) of the sync pulse or during the true state of the sync pulse. When the sync pulse is true, it is applied through the switch and enables the inputs to both IC1A and IC1D. If the signal you are looking for at the probe tip becomes true at the same time or during the time of the sync pulse, a P will be displayed, indicating that the logic true was present. This is accomplished by the changing states of IC1A and IC1D which trigger the one-shot, IC4. If the signal you are looking for was not true during the sync pulse time, an L will be displayed and remain.

When using the negative sync input, this means that you are looking for a signal at the trailing edge of a sync pulse or during the time that the sync is false. The first thing to do is to move the switch (S1) to the negative position. When the sync pulse goes low at its trailing edge, it is applied to pin 11 of IC3E, making its output true and thus enabling IC1A and IC1D. If the input signal goes true during that time, the pulse circuit is triggered and a P is displayed, indicating that the pulse was there at that time. When you are not using a sync input, switch S1 must be kept in a positive position or the normal probe functions will not work correctly. Also, when the sync input is used and the probe tip is floating, a P will display if the sync input is active.

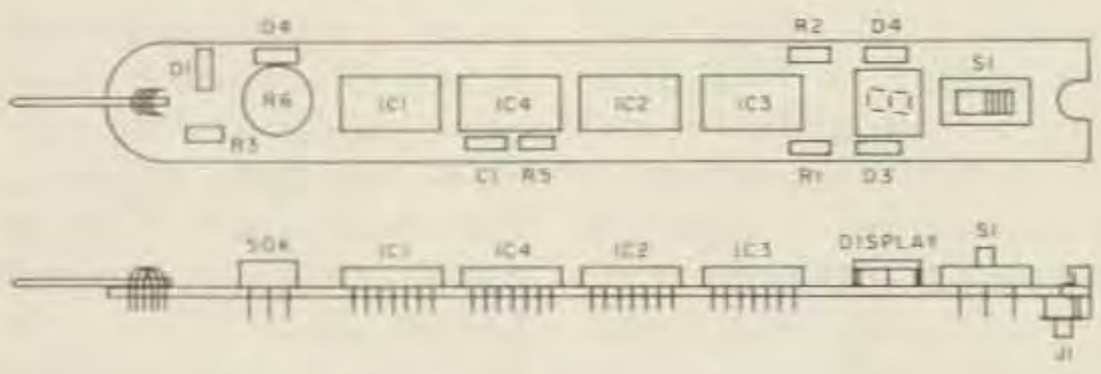


Fig. 3. Synchronized Logic Probe component mounting.

Construction

Fig. 3 and the photos show the complete circuit of the Synchronized Logic Probe, but there are a few things that might prove to be helpful. The prototype of this probe was built using 0.1" perfboard which was cut and shaped to fit inside a cigar tube prior to mounting any of the components. Wire buses were used for the +5-volt and ground connections for the chips and other components. As shown in Fig. 3, you should mount the display, switch, and sync jack on the end of the board first, and make any necessary cutouts on the tube housing and board. Make sure that switch S1 is easily accessible and sticks up through an opening in the tube.

There is only one adjustment on the probe—the 50k variable resistor used to establish the F state. When you get the probe assembled, connect it to your power supply and note that there is a legible display (L, H, or F). You should adjust the potentiometer until an F is displayed with no connection to the probe tip. Once this is obtained, you will notice that there is a range of adjustment before the display changes from an F to an L or H. This adjusts the sensitivity of the probe tip to a logic high or low.

Upon completion, touch the probe tip to the +5-volt side and then to the ground side of the power supply that you are using. The probe should display an H when touched to the +5 volts. A P should be displayed for approximately .75 seconds when first touched to ground, before going to an L display. If a P is not displayed when the probe tip is first touched to ground, the pulse circuit is not functioning correctly. As long as the other displays are correct, then the problem should be in the one-shot (IC4). Check the external capacitor and resistor connections to the chip. If the other displays do not work correctly, then you will have to troubleshoot the entire circuit.

A neat trick for troubleshooting can be used if you have a display with a decimal point: Connect a piece of wire approximately 10 inches long through a 100-Ohm resistor to the decimal point and use it for a simple probe. If you touch the wire to a logic high, the decimal point will light, and if it is a low the decimal point will stay off. The 100-Ohm resistor in series with the wire is to prevent burning up the decimal point.

I used this basic logic probe when troubleshooting the more sophisticated, Synchronized Logic Probe. This, along with the circuit operation and schematics provided, should give you everything you need to build and troubleshoot the Synchronized Logic Probe. Good luck!■