Use this Adapter to add storage facilities to your CRO

Digital Storage CRO Adapter

While many hobbyists and electronics technicians have access to an oscilloscope, very few are fortunate enough to have access to a storage oscilloscope. These expensive instruments can be a real boon for examining transient behaviour such as "glitches" in digital circuitry. Our Digital Storage CRO Adapter provides this facility at a fraction of the price of a conventional storage oscilloscope using low cost components.

by JOHN CLARKE

Unwanted transients in digital waveforms often go unnoticed when using conventional oscilloscopes but they can cause serious disruptions in the operation of circuitry and make fault finding difficult.

Storage of the waveform is a necessity in these cases and a relatively inexpensive method of achieving the store is preferable to the costly storage oscilloscope. Conventional storage oscilloscopes consist of either a special screen phosphor or charged mesh, which keeps the trace visible for long periods of time.

An alternative method of storing a waveform is to use a digital memory. Here the waveform is stored by sampling the waveform and placing in each memory location the discrete voltage level existing at that point in time. After the waveform is stored, the memory can be continuously cycled through its addresses to display the stored waveform.

Several advantages are to be had from digital storage over conventional storage methods. Firstly, the stored waveform can be displayed indefinitely, giving the observer unlimited time to observe the waveform. Secondly, the trace can be expanded with either the oscilloscope or Digital Storage CRO Adapter timebase to observe critical areas in the waveform, without having to store the waveform again.

Since we can adjust the timebase after recording the waveform, some form of recorded timebase marker would be helpful for us to measure the frequency of the recorded waveform. This is done in the form of a tracer or marker pulse which is recorded during the recording of the waveform. This tracer is mixed with the stored waveform on playback to give a visible and unambiguous timebase marker. So however we set the timebases after recording, the tracer will remain in a time relationship with the recorded waveform.

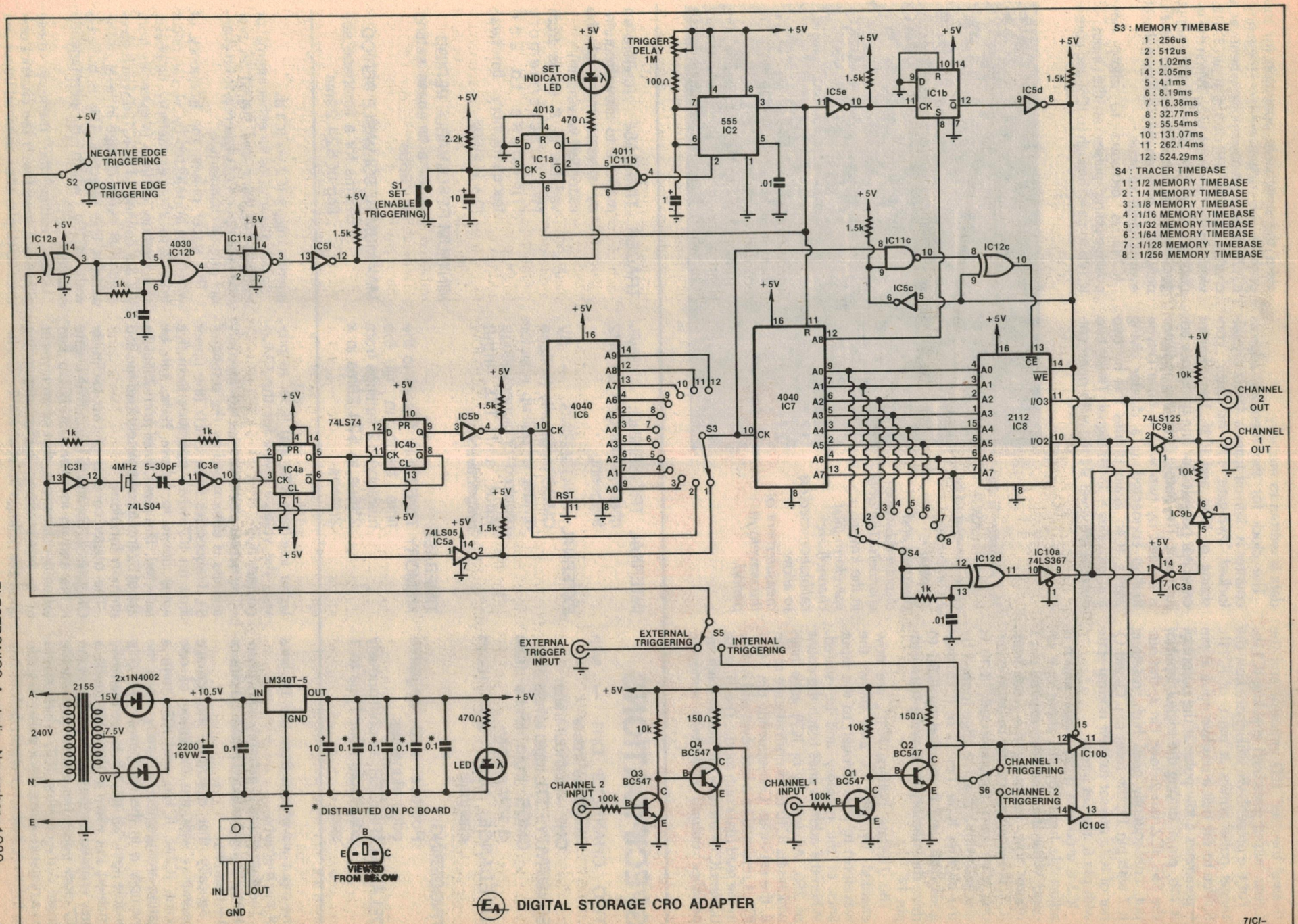
Turning now to the circuit diagram: Heart of the circuit is the 2112 memory (IC8) which features four input/output (I/O) lines and eight address lines. The eight address lines allow for 256 bytes of the four bit memory. In other words we can store and retrieve four channels each of up to 256 level changes.

Driving the memory address lines is the 12-stage binary counter IC7. This is normally operating in a continuous count mode such that the address lines are incrementing from 0 (eight zeros) to 256 (eight ones). When 256 is reached, the address count begins again at zero. In effect, we are continuously and sequentially addressing each memory location. If data is in memory then this will be retrieved as a repeating waveform.

To be able to store a digital waveform, the memory must be placed into the "write" mode, the address lines must be reset to zero and some means of preventing "overwriting" after the memory is full (256 addresses) is required. Ancillary to these requirements is that the storage of the waveform takes place only when a trigger signal is initiated.

To see how each of these functions are performed let us examine what happens when a waveform is stored. Initially the memory is in the output mode, supplying data and the counter is cycling through the addresses. Upon depression of the "set" switch, (S1) pin 3, the clock input of IC1a, a D-type flip-flop, is brought low. Releasing the switch allows the 10uF capacitor also connected to pin 3, to charge. This positive edge clocks IC1a. The Q-output now goes low ac-

FACING PAGE: the circuit diagram for the Digital Storage CRO Adapter.



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tivating the "set" LED indicator and the Q-bar output goes high enabling IC11b.

For the present, we will ignore how the trigger pulse arrives at pin 6 of IC11b. Suffice to say that a positive pulse at pin 6 generates a low pulse at the output of IC11b, pin 4, driving the trigger input of the 555, IC2, pin 2, low. Pin 3, the output, consequently goes high, resetting IC7 with pin 11, the reset pin. Q and Q-bar of IC1a are set to their normal state with pin 6, the set input.

IC2 is used as a delay trigger which is adjustable from 10us to about one second. When the time delay expires, pin 3 returns low, removing the reset from IC7, allowing the counter to begin counting from zero. Simultaneously IC1b is clocked with a positive edge formed by the inverter IC5e. Pin 12 of IC1b then goes high, and is inverted by IC5d to drive the memory to its write state with pin 14.

The Tri-state buffers, IC10, are now enabled by pin 15 and allow the waveform to pass through to the input lines of the memory and be stored. When the address lines reach the count of 256, A8 (pin 12 of IC7) goes high which sets IC1b to its normal state at pin 8, the set input. Consequently pin 14 of IC8 is returned to a low level and is now in the read (data out) mode. The Tri-state buffers IC10 are now in Tri-state (high impedance output) effectively removing data is written to memory.

The clock for the memory address counter is derived from a 4MHz crystal-locked, two-gate TTL oscillator, consisting of IC3e and IC3f. The trimmer capacitor provides for fine frequency adjustment. The output from this oscillator is divided by two with IC4a, a D-type flipflop connected as a divider giving 2MHz. IC4b again divides this by two and provides a 1MHz signal. These two outputs are level shifted with open collector inverters IC5a and IC5b, to provide the voltage levels for the CMOS counter IC6.

The actual clock rate for the memory address is determined by the setting of S3. Frequencies from 2MHz (the upper limit for IC7 when operating from five volts) down to below 1kHz, can be selected. This gives times from 256us to about 524ms to completely load the 256 memory locations.

The trigger consists of two exclusive-OR gates IC12a and IC12b, a NAND-gate IC11a and an inverter IC5f. IC12a performs two functions, that of an inverter or a non-inverting buffer depending upon the voltage level at pin 1. S2 provides the switchable operation for this positive or negative-edge triggering. IC12b gives a positive pulse whenever a change in waveform occurs at pin 5. This works in the following way. When the inputs on IC12b are different the output goes high and is low otherwise. The RC network on pin 6 enables a 10us pulse at every change of state.

IC11a is provided to allow only positive-going pulses at the input of IC12b to pass through to IC5f and consequently trigger IC2 via IC11b.

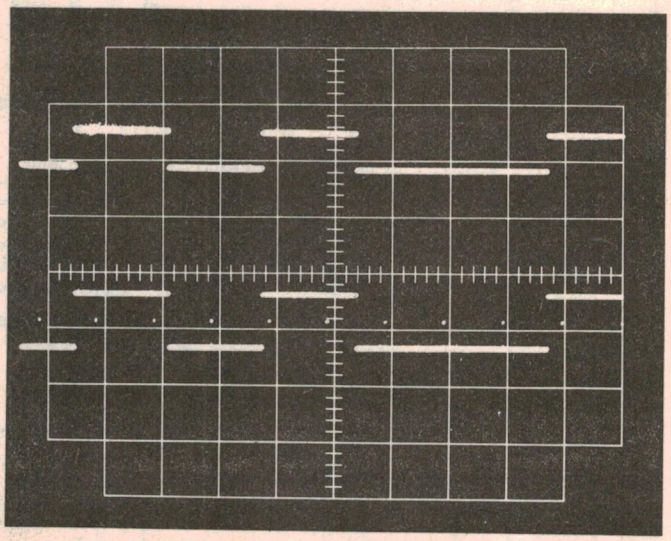
Switch S5 provides for either internal or external triggering and switch S6 provides the option of triggering from channel one or channel two.

The tracer pulses, the frequency of which can be selected by S4, can occur from 2 to 256 per memory timebase. The memory address frequencies from IC7 are connected to IC12d which gives a pulse at every change in level of the address line selected. This is buffered with IC10a which is permanently enabled.

Upon reading the memory, these pulses are mixed with the channel one trace to display the combined tracer and the input waveforms from the 1/0 lines of the memory.

The data stored in memory is now constantly being produced at the 1/0 pins of the memory.

Basically that describes the storage operation with the exception of one point. IC11c, IC12c, and IC5c form a gating arrangement whereby when the memory is in the read mode the chip enable (pin 13) of IC8 is permanently enabled, but when in the write mode is only enabled on the positive cycle of the IC7 clock pulse. This is done to allow the ripple carry counter, IC7, which clocks on a negative going clock pulse, to settle its memory address outputs before any



The Adapter in use – here an ASCII code generated by a computer terminal is captured and displayed by both channels. The dots in the lower waveform (first channel) are calibration markers to allow measurement of the waveform period.

SPECIFICATIONS

TWO CHANNELS: CH1 — with timebase tracer
CH2 — without tracer

SENSITIVITY: TTL logic levels and CMOS logic levels from 3-15V supply

IMPEDANCE: 100k ohm (both channels)

TRIGGERING:
Positive and negative edge triggering:

DELAYED TRIGGER: — continuously adjustable from 10us to 1 sec

INTERNAL TRIGGERING: — switchable from CH1 or CH2 triggering

EXTERNAL TRIGGERING: — 5V CMOS input only (voltage divider or pull-up resistor required for higher voltage input and TTL input respectively)

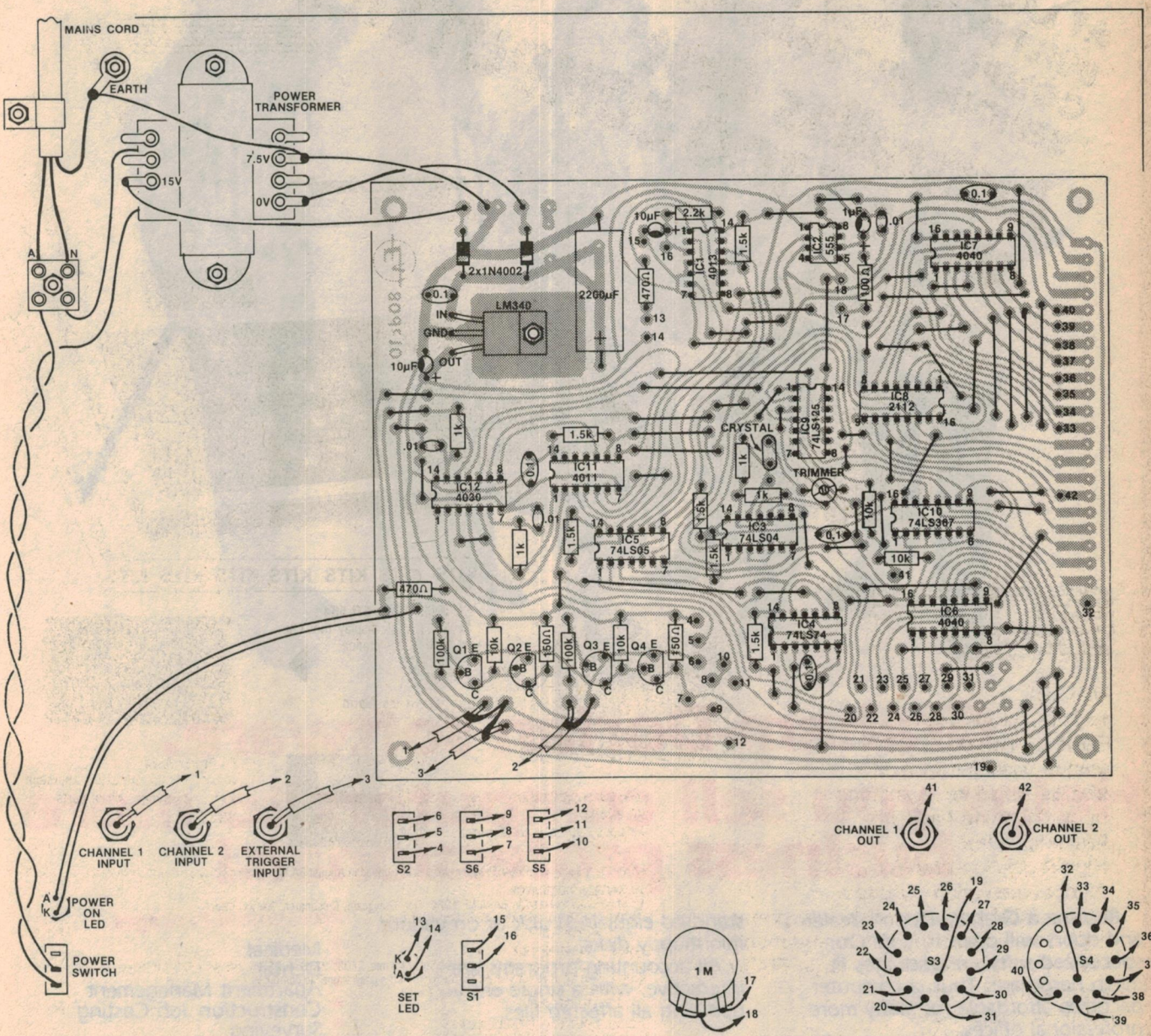
TIMEBASE:

MEMORY TIMEBASE: (refers to the time taken to fill the memory) 12 settings from 256us to 524.29ms in x 2 steps

TRACER TIMEBASE: (calibrated markers to allow frequency measurement of the recorded waveform) variable in 8 steps from two traces/memory timebase to 256 traces/memory timebase in x 2 steps

MINIMUM RESOLVABLE PERIOD: 1us for a timebase setting of 256us

MAXIMUM RESOLVABLE PERIOD: 524ms for a timebase setting of 524.29ms



Follow this wiring diagram in conjunction with the circuit on p55. The PC board is shown from the component side.

stored waveform. This is done with two Tri-state buffers 1C9a and IC9b, and inverter IC3a. IC9a and IC9b have their Tri-state controls complementary to one another, such that one is in Tri-state while the other is not. At the event of a tracer pulse, IC9a goes into Tri-state and IC9b pin 6 gives a negative pulse. This is voltage divided to give a 2.5 volt trace. At the completion of the tracer pulse, IC9b goes to Tri-state and IC9a gives the stored signal output.

Both input channels have transistor buffers to allow for various input voltage levels, such as 15V CMOS or TTL levels.

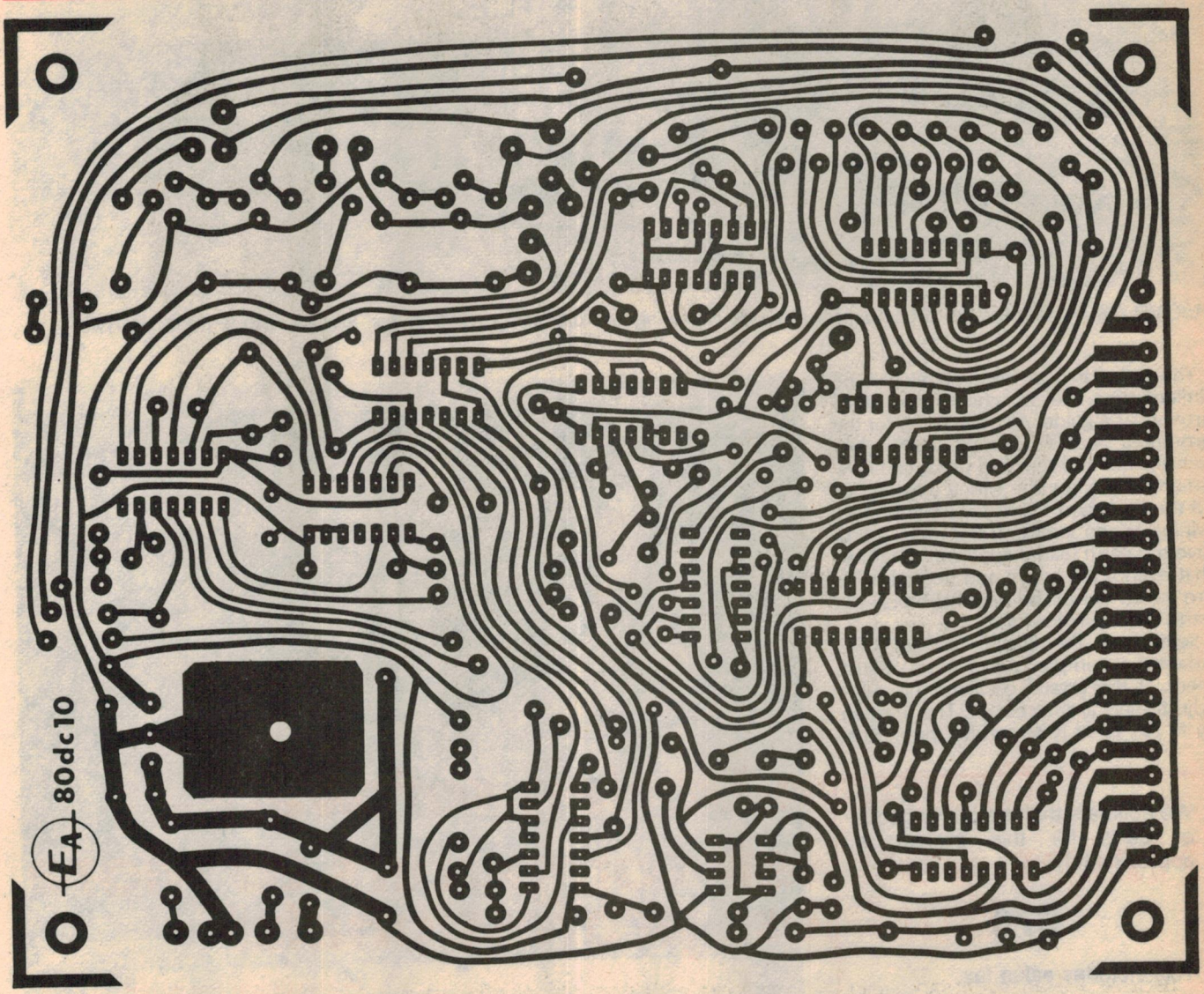
The power supply consists of a centre tapped transformer connected in a full-wave configuration. The rectified output is filtered with a 2200uF capacitor and regulated with a 5V three-terminal regulator. Power on is indicated by a LED. Four 0.1uF capacitors are spread throughout the printed circuit board power supply rails to aid decoupling.

We built our Digital Storage CRO Adapter on a PC board measuring 141 x 174mm, coded 80dc10, and housed it in a Horwood instrument case measuring 305 x 76 x 228mm (W x H x D).

Start construction by placing the links on the PC board and soldering them in place. Use the overlay diagram to help you in the construction. There are over 50 links on the PC board.

Next the diodes and resistors can be soldered into place, followed by the ICs. The CMOS ICs, the 4040, 4011, 4030 and 4013 should have their power supply pins soldered first with the barrel of the soldering iron connected to the negative rail. Note that the 2112 is oriented differently to the other ICs on the PC board.

Finally the capacitors, transistors and crystal can be soldered in place. The three terminal regulator is intended to be bolted flat to the board with a brass nut and bolt so that the small amount of heat generated by the regulator is dissipated by the copper beneath the board. The leads will need to be splayed and bent to fit into the holes reserved for the regulator.



Here is an actual size reproduction of the PC artwork.

PARTS LIST

1 Scotchcal panel
1 Instrument case measuring 305 x 76 x 228mm (W x H x D)
1 printed circuit board measuring 141 x 174mm, coded 80dc10
5 panel mount BNC sockets
3 knobs
1 15 volt 1A centre tapped-transformer, A&R 2155 or equivalent
1 single pole, 12-way rotary switch
1 single pole, 8-way rotary switch
1 single pole normally open pushbutton switch
4 SPDT switches
1 4MHz crystal (miniature type)
1 mains cord and plug
1 grommet to suit mains cord
1 cable clamp
4 rubber feet

SEMICONDUCTORS
1 555 timer
1 LM340T-5, A7805, 5V 1A, 3-terminal regulator
2 LEDs with bezels
2 1N4002 100PIV rectifier diodes
4 BC547 NPN transistors

RAM
1 2112 256 x 4 static RAM, 450ns access time

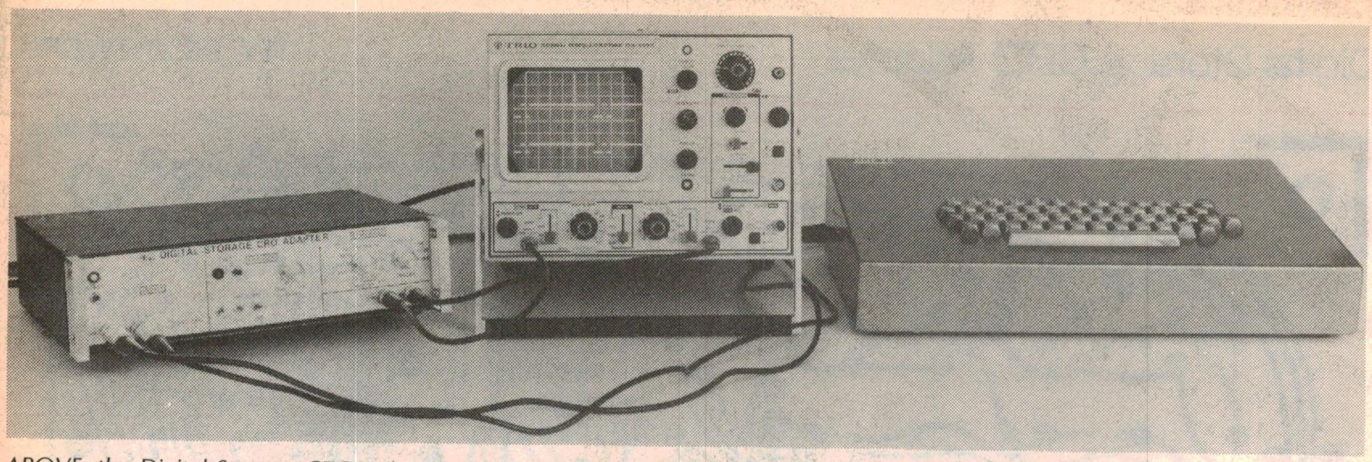
CMOS
1 4011 quad two-input NAND gate
1 4013 dual D flipflop
1 4030, 4070 quad EXCLUSIVE-OR gate
2 4040 12-stage ripple carry binary counters

Low Power Schottky TTL
1 74LS04 hex inverter
1 74LS05 hex inverter with open-collector outputs
1 74LS74 dual-D flipflop
1 74LS125 Tri-state quad buffer
1 74LS367 Tri-state hex buffer

CAPACITORS
1 2200uF/16VW pigtail electrolytic
2 10uF/6VW electrolytic
1 1uF/6VW electrolytic
5 0.1uF metallised polyester
3 0.01uF metallised polyester
1 5-30pF ceramic trimmer

RESISTORS (¼W, 5%)
2 x 100k, 4 x 10k, 1 x 2.2k, 6 x 1.5k, 4 x 1k, 2 x 470 ohms, 2 x 150 ohms, 1 x 100 ohms, 1 x 1M (linear) potentiometer.

NOTE: Ratings are those used on the prototype. Components with higher ratings may generally be used providing they are physically compatible.



ABOVE: the Digital Storage CRO Adapter at work, capturing and displaying ASCII codes. BELOW: inside the prototype.

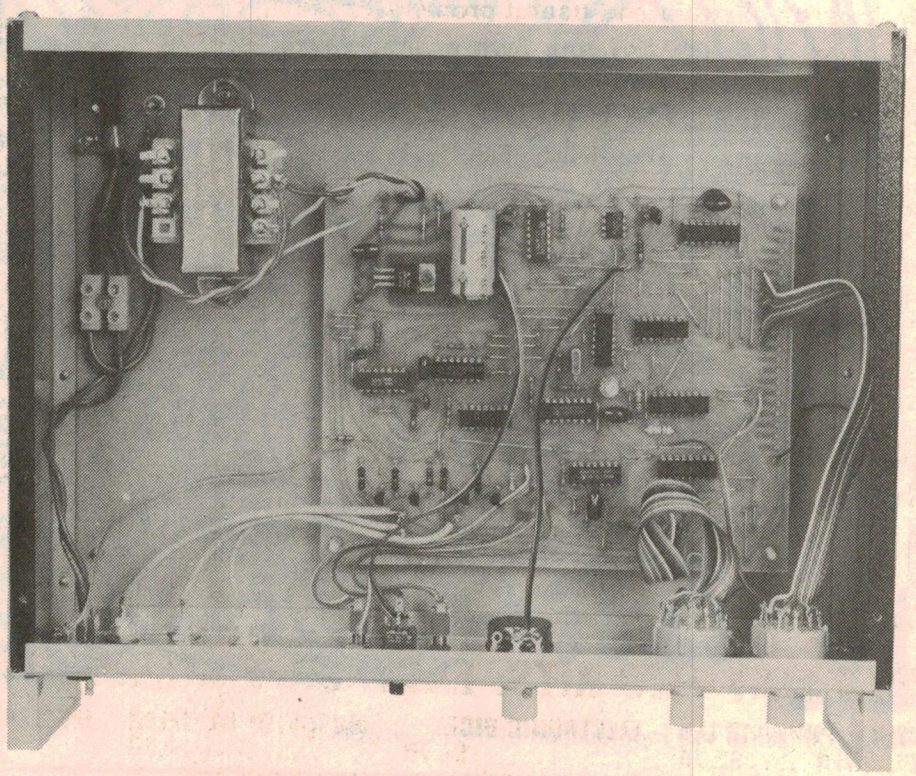
The holes in the front panel can be drilled using the Scotchcal front panel artwork as a guide. Also the holes for the grommet, cable clamp, earth lug, transformer and terminal block can now be drilled. Follow the wiring diagram for all the PC board to external component wiring. When wiring in the mains cord, give the earth lead a generous length so that even if the active and neutral wires are pulled out of the terminal block, the earth wire remains intact.

Setting up the Digital Storage CRO Adapter is simple. Apart from adjustment of the crystal oscillator no other adjustments are necessary. The frequency at pin 10 of IC3e can be trimmed to 4MHz with the use of a frequency meter. This adjustment is not critical, however, and even without adjustment, will give a more accurate timebase than that on an average oscilloscope.

We estimate that the current cost of parts for this project is approximately

$78

This includes sales tax.



Although there are many controls, operation of the Digital Storage CRO Adapter is not difficult. Most of the controls are self explanatory. Firstly any signals to be stored are fed to the channel one and channel two inputs. The inputs to the CRO then come from the channel one and channel two outputs of the Adapter.

Triggering can be selected to be either from channel one, channel two or from an external source, in which case the external trigger input will need to be connected as well. Note that this input can be a 0-5V signal only. A voltage divider will be necessary if other logic levels are used. Positive and negative edge triggering can be selected. The time delay between the triggering and beginning of storage can be set with the Delay control, for delays from 10us to about one second.

There are two timebase controls, the tracer and memory timebase. The graduations on the memory timebase refer to the time taken to completely load the 256 memory locations. For example on the maximum timebase of 256us, the memory will take 256us to load the data. Consequently we can load data which has level changes not exceeding 256us/256 = 1us. Alternatively on the slowest timebase of 524.29ms, we can load data at the rate not exceeding 524.29ms/256 = 2.05ms.

From the above discussion it is evident that we can record level changes from 1us (or 500kHz) down to the lowest resolvable frequency of 1/524.29ms, that is 2Hz for a full cycle of storage or 1Hz for a half cycle of storage.

The tracer timebase is adjustable from two traces per memory timebase to 256 per memory timebase. For example with a 256us memory timebase and tracer timebase setting of 1/2, the time between each tracer is 256 x 1/2 = 128us. Alternatively on the same memory setting but on the 1/256 tracer timebase, the time between each tracer is 256us x 1/256 = 1us.

The Set switch enables the circuitry to be ready for storage of the waveform immediately there is a trigger signal. This can be immediately or if a rarely occurring pulse is to be stored, can be minutes or even hours away before the storage takes place.

Some readers may be wondering why the PC board has facilities for more external connections than are actually used. In a future issue we hope to produce an extra PC board incorporating an analog-to-digital converter and digital-to-analog converter plus extra memory and triggering circuitry so that an analog signal can be stored.