Add-on oscilloscope waveform store — 1

Digital unit for audio waveform storage and display using a dual-channel oscilloscope

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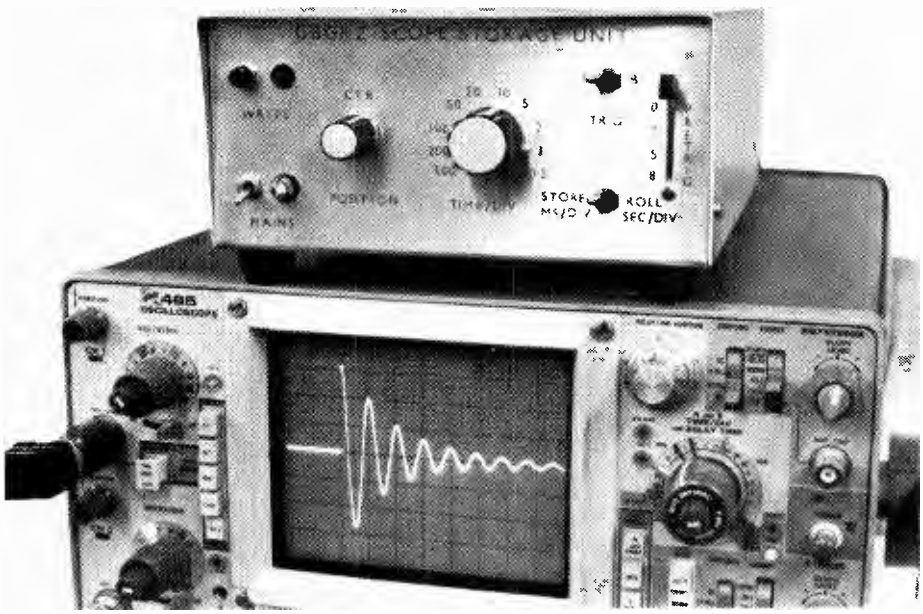
The instrument described here employs digital storage techniques to allow an ordinary dual-channel oscilloscope to function as a storage type. The input signal to the oscilloscope is extracted, converted to digital form, stored, converted back to the analogue form and displayed on the oscilloscope screen. A useful feature is that the waveform before the trigger pulse can be displayed. Circuitry is included to remove the "steps" in the waveform which would ordinarily be the result of a sampling process. Interfacing with the oscilloscope is not dealt with in detail, since requirements vary with facilities existing already.



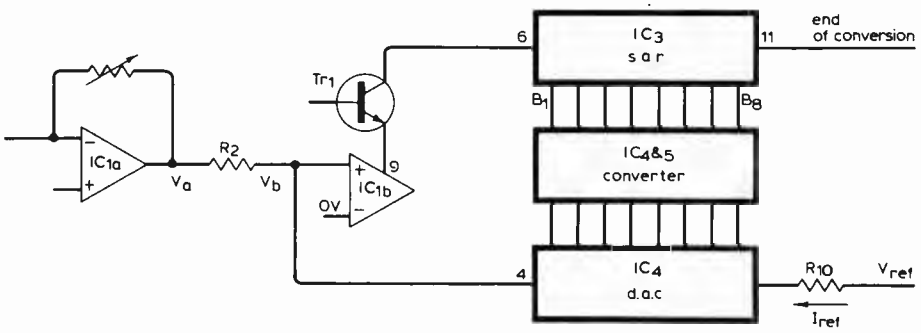
The storage unit in use, displaying a test waveform.

THIS IS a mains-powered instrument designed to give a storage facility to a non-storage oscilloscope. The instrument consists of an analogue-to-digital converter, 8000 bits (1000 × 8) of memory, a digital-to-analogue converter and a step eliminator, which converts the normal step output of the d.a.c. to straight lines. This greatly improves the presentation of stored waveforms with few samples. There is also some control circuitry to control the read/write, sync. and blank functions. A crystal oscillator is used for simplicity and stability, and its frequency is divided down in a 1, 2, 5 sequence to give 10 time/division ranges. There is also a roll mode of operation which gives an extra nine time/division ranges below that of the normal storage mode. A useful pretrigger function enables the unit to store the waveform leading up to and away from the trigger point – a mode which is not possible with normal c.r.t. storage. An advantage of this system of storage is that the waveform may be expanded and analysed after being stored.

Since the unit may be used to store digital waveforms with fast transitions a tracking a-d converter was rejected because of its slow full-scale slew rate. The successive-approximation type used will reach any level in a maximum time of 2% of a division, assuming the input changes state during the first of the two samples. On the other hand, the slew time of the tracking type of converter depends on the input levels, and has a maximum time of 2^n clock pulses. Reduction of this time can be accomplished by increasing the clock frequency when the difference between input and digital output is greater than a specified amount. The frequency can then be reduced when the difference between the levels has been reduced. There is the disadvantage, in this mode of operation, that more complex circuitry is needed to detect the levels at which the higher speed clock is gated in and out.

Random-access memory i.cs were rejected as storage elements in favour of shift registers, because the register's sequential operation suited the circuit operation. One disadvantage of r.a.ms is the need for address lines, which results in more components and greater complication in p.c.b. layout. Another is the increased complexity of the circuitry, especially regarding roll and pretrigger functions.

Fig. 1. Block diagram of the input circuit and d-a converter.



Analogue-to-digital converter

Analogue input waveforms are converted to 8-bit binary form to provide 256 discrete levels on conversion back to analogue form for display. The converter, shown in Fig. 2, is in action continuously, whether the instrument is reading or writing. It uses three integrated circuits to perform its major functions: a MC14559 c.m.o.s. successive-approximation register (not the locmos version, which has a higher propagation delay); a MC1408-L8 bipolar, 8-bit digital-to-analogue converter; and MC1407 bipolar a-d control circuit, which is a wideband amplifier and comparator. Transistor Tr_1 shifts vol-

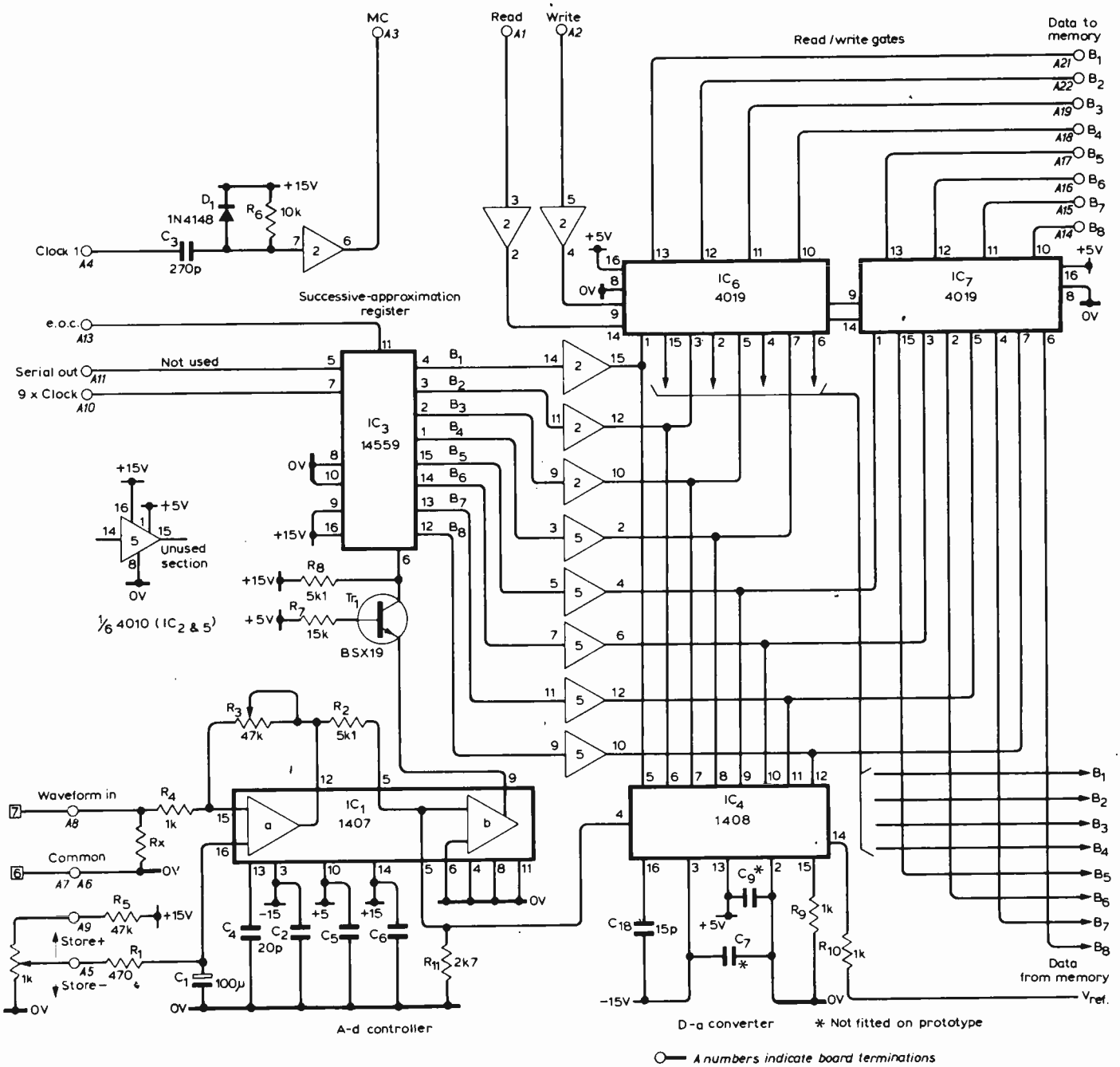
tage levels from the bipolar 5V of the MC1407 (IC_1) to c.m.o.s. 15V for IC_3 and, similarly, the eight buffers in $IC_{2,5}$ shift levels back to 5V for the bipolar MC1408-L8 – IC_4.

Operation. In essence, the converter is an analogue-digital-analogue feedback loop. The block diagram of Fig. 1 shows the input amplifier, IC_{1a}, whose output is taken to a voltage comparator, IC_{1b}. Via the level shifter, Tr_1, the comparator controls the successive-approximation register, IC_3, which is clocked. The digital outputs of the s.a.r. are buffered and applied to the digital-to-analogue converter, IC_4, whose output is then taken back to the comparator. The loop circulates until the two comparator inputs are zero.

Assume that, in Fig. 2, the s.a.r. is reset, with B1 to B8 low: IC_4, the d-a converter in the a-d loop, is drawing no current via its output pin 4. Also assume some positive output, V_a, from IC_1, pin 12. The comparator sees a positive voltage, V_b, on its non-inverting input, IC_1, pin 5; its output, pin 9, is high. Transistor Tr_1, the 5V-15V level shifter, is off and its collector is high. This high voltage is fed into the s.a.r. D input, IC_3, pin 6 which, on receipt of the first clock input, enables B1, the most significant bit, which appears on IC_3, pin 4, to be set. When the m.s.b. goes high, it is converted down to the 5V level and is fed into IC_4, pin 5. IC_4 now draws $I_{ref}/2$, and V_b, the voltage at the comparator input is now $V_a - I_{ref}/2 \times R_2$. If this voltage is positive, the comparator output will be high; if negative, the output will be low.

If it is high, the next clock pulse sets IC_3, pin 3, which is bit 2, high. This causes IC_4 to draw $I_{ref}/2 + I_{ref}/4$, hence the current corresponding to each bit is half that for the previous one. Now, $V_b = V_a - (I_{ref}/2 + I_{ref}/4 \times R_2)$ and is again compared as before. This time, if V_b is negative, the comparator output is low and the next clock pulse simultaneously resets B2 and sets B3. The output of IC_3 draws $I_{ref}/2 + I_{ref}/8 \times R_2$ and again the IR product is subtracted from V_a and the result compared. This sequence is continued for all eight bits, each being generated, added to the previous bit, compared and reset or remaining set to keep $V_b = 0$. At the end of the sequence, IC_3, pin 11, which is "end of conversion" (e.o.c.), goes high and is used to

Fig. 2. Circuit of the a-d converter. The gates in $IC_{6,7}$ are controlled by the read/write circuitry and connect the digitised input to the memory or the output of the memory to its input for re-circulation.



generate a pulse, which sets a flip-flop and strobes the data into memory by means of a write pulse and $IC_{6,7}$. The complete sequence is nine clock cycles long, the e.o.c. being half a cycle wide.

Memory

Sixteen NE2528, dual 250-bit, c.m.o.s. shift registers are used for the memory, operated from +5V and −8V (no 0V). The data is clocked through by a modified end of conversion (e.o.c.) pulse generated by the a-d converter.

Since the memory is, in effect, eight large shift registers, as seen in Fig. 3, all that is required for operation is a clock and some read/write gating. Two 4019 and-or gates, seen in Fig. 2, are used for this gating, controlled by the read and write inputs. The latter enables the gates from the a.d.c. to the memory input, whilst the latter inhibits the gates from the memory output to input. When the unit is in a 'write' condition, the first bistable in the memory acts as a latch, eliminating the need for separate latches.

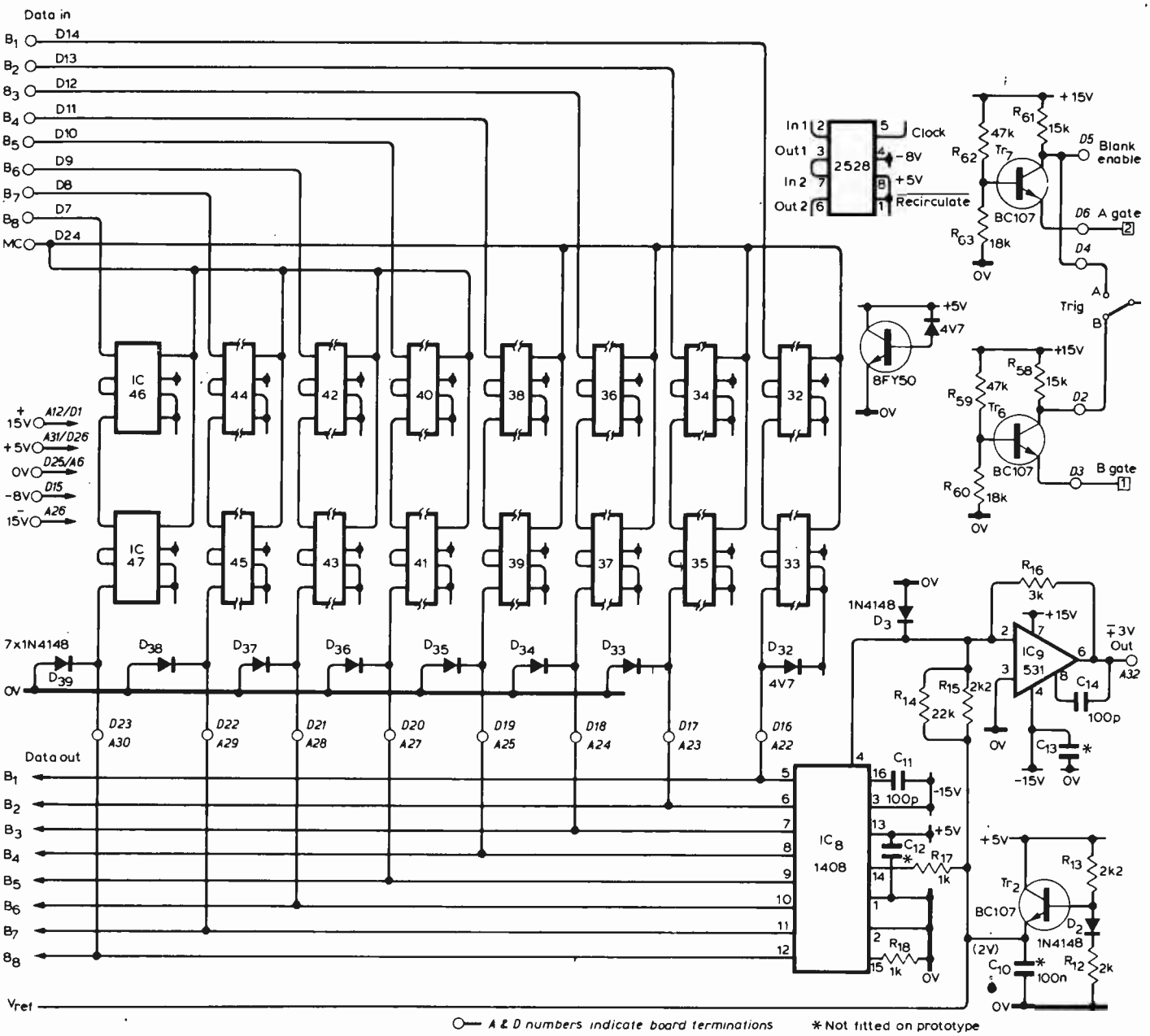
The NE2528 shift registers require a high clock pulse width of not less than 200ns and a low pulse width of not greater than 100μs; if the clock pulse is low for longer than 100μs data is lost, but it may stay high indefinitely. For this reason, R_6 and C_3 in Fig. 2 are required to form a pulse generating circuit, whose function is to limit with width of the clock pulse to approximately 3μs when on low clock rates. Omission of these components results in the stored waveform deteriorating as the memory i.cs warm up.

Fig. 3. Circuit of the memory and d-a converter. IC_9 provides the output for the step eliminator of Fig. 5.

Outputs $B_{2\text{-}8}$ are clamped by 1N4148 diodes to prevent them forcibly switching on the d.a.c. inputs. Output B_1 is clamped by a 7.4V zener diode from +5V because it was found that if this input went 0.7V negative, the output appeared to have "crossover distortion." Several d.a.c. chips were tested and all showed this distortion. No mention of this phenomenon was found in the specifications of the d.a.c. chip.

D-a converter

A second MC1408-L8 i.c., IC_8, is used for the d-a conversion as shown in Fig. 3. Since the device has a constant current-output it is followed by a current-to-voltage converter, IC_9. The inputs to the d.a.c. are taken from the outputs of the memory. A positive current corresponding to B_1 is fed into the output of the d.a.c. via R_{14} and R_{15}, causing the output of IC_9 to become



bipolar. If B_1 were presented to $IC_{8/9}$, pin 4 would draw $I_{ref}/2 = V_{ref}/R_{17} \times \frac{1}{2} = 2V/1k \times \frac{1}{2} = 1mA$. R_{14} and R_{15} in parallel equal approximately 2kΩ. R_{14}, the "select-on-test" resistor, is chosen so that with B_1 only the final output from the unit is 0V; i.e., it is an offset adjustment. R_{14} and R_{15} are connected to V_{ref} and, assuming their combined value is 2kΩ, supply the 1mA to IC_8, pin 4. As IC_9 input is a virtual earth, $IR_{16} = 0$ and therefore the output will be 0V. The voltage output from the circuit ranges from:

$-IR_{14}R_{15}R_{16} = -V_{ref}R_{16}/R_{14}R_{15} = -3V$

to

$-I_{d.a.c.(max)} + IR_{14}R_{15}R_{16} = 2.97$

or about ±3V.

The characteristics of the d.a.c. are such that the m.s.b. current switch is the fastest to operate and the least signficant bit is the slowest, with the intermediate bit-switching times increasing with decreasing significance. the transition B_1 off – B_{2-8} on, to B_{2-8} off – B_1 on, results in some period of time when B_1 has switched on but B_{2-8} (or any combination) have not switched off. During this short period of time all eight bits appear to be on and the output of the d.a.c. tries to draw maximum current, resulting in a negative-going spike. Diode D_3, a 1N4148 or similar, is included in the circuit to "fill in" this spike. If this diode is omitted IC_9 output would try to follow the spike and a positive glitch would appear at the output.

The reference voltage generator is basically a potential divider buffered by an emitter follower Tr_2. The 1N4148 diode is included for thermal stabilisation.

Clock

A 1.8 MHz crystal oscillator, seen in Fig. 4, is used to generate the maximum clock frequency required, which is nine times the maximum sample rate. This is divided down under control of the time/division switch, S_{5a}, to give a nine times clock output for each of the normal store mode ranges. As the output is fed only to the s.a.r. the whole circuit is operated from a +15V supply. MC14510 decade counters are used for the first two stages, IC_{20-21}, and a CD 4029 binary/decade counter, IC_{22}, for the third.

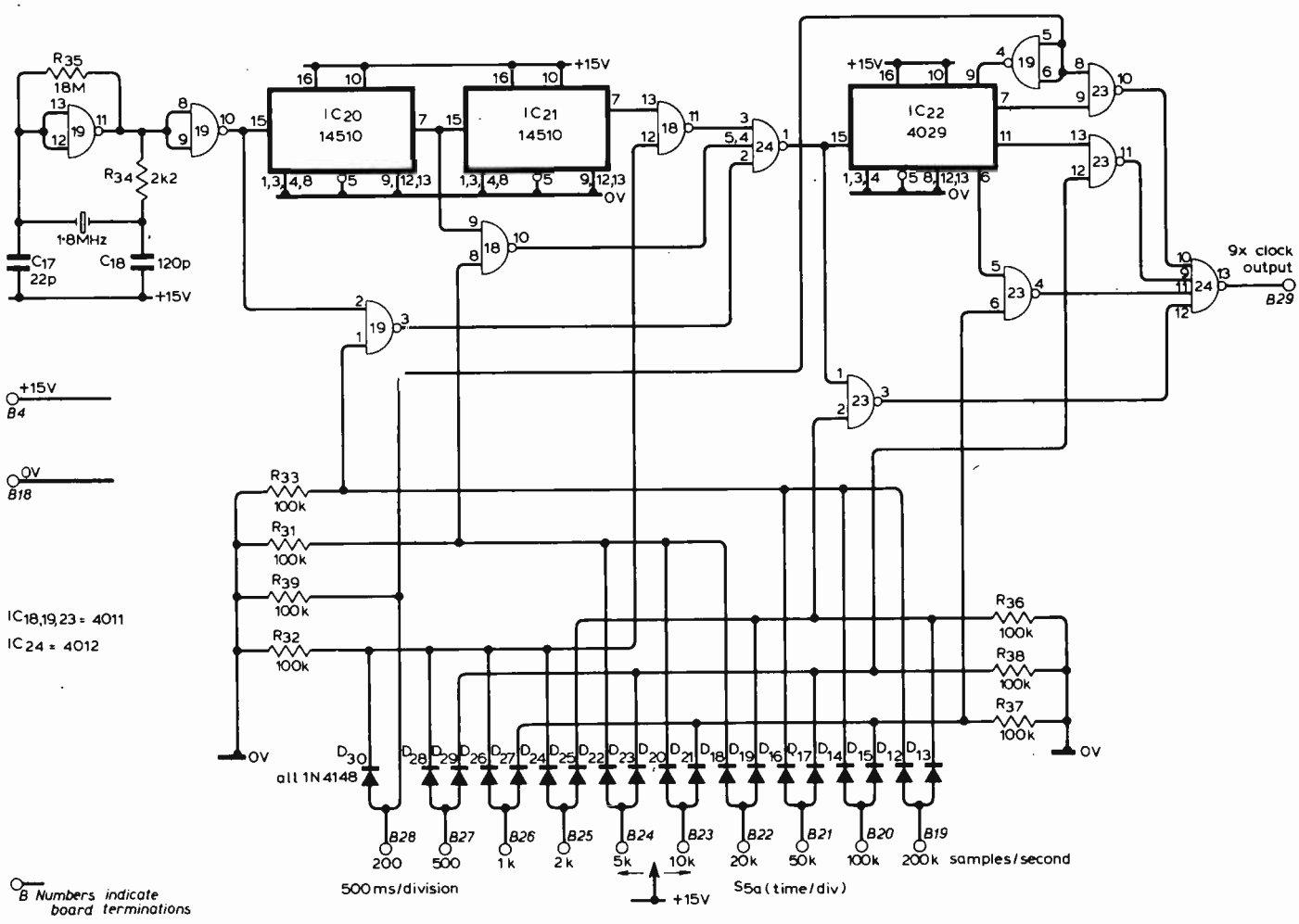
The output from the crystal oscillator is divided down by gating it into, or around, counters as required. Gates are operated in pairs and are enabled from the time/div. switch by diode logic. Ranges above 0.5s/div. use decade counters in the first two stages and a binary counter in the last. Binary outputs 1 and 2 are used to give divisions of 2 and 4 respectively. The 0.5s/div. range is derived in a similar manner, except that the third counter is operated in the decade mode and the output is taken from the terminal count. If starting of the oscillator is unreliable the 18 megohm resistor in the circuit may be reduced to 10 megohms. This resistor sets the bias level at the input of the nand gate.

Fig. 4. Crystal oscillator and dividers, with gating for selection of final clock frequency.

Step eliminator

The function of this circuit, shown in Fig.5, is to convert the normal step output of the d-a converter to something more presentable. It consists of a differential amplifier, followed by a sample-and-hold circuit and an integrator. The output is taken from the integrator, IC_{29}, via an inverting buffer, IC_{28}. The integrator time constants are selected by the time/div. switch.

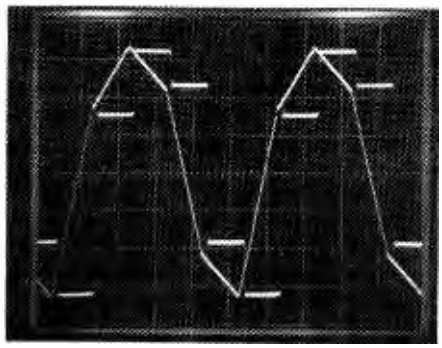
Assuming the input and output of the circuit are at 0V, the differential amplifier IC_{25} will also be at 0V and, when the 4016 analogue gate IC_{26} is strobed, the storage capacitor C_{28} will also be at 0V. When the strobe pulse is removed, the 4016 gate is disabled and has an impedance of several megohms. The voltage stored by C_{28} is buffered by IC_{27}, a LM301 voltage follower, and fed to the input of the integrator, which will remain at 0V by virtue of the virtual earth configuration.



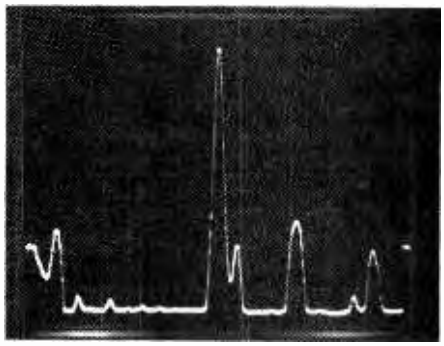
If an input step of 2V is now received, the output from IC_{25} will go to −2V, since it has unity gain. After approximately 2.5μs, which is the time allowed for settling, IC_{26} is strobed by a 0.5μs pulse, the storage capacitor being charged to −2V, and is fed via IC_{27} to the integrator, which is made to perform a positive-going ramp at a rate determined by the −2V and the timing components $R_{50\text{-}52}$ and $C_{31\text{-}40}$. Since the storage capacitor imposes a heavy load whilst charging, a reservoir capacitor, C_{24}, is connected from the output of IC_{25} to 0V to supply the current during the strobe time.

The integrator output voltage is shown simply in Fig. 6. Input current I_{in} = fed-back current $-I_F = V_{in}/R$. $V_c = Q_c/C$ and $Q_c = I_F t$, therefore $V_c = -I_F t/C$. But $I_F = V_{in}/R$, so $V_c = -V_c = -V_{in} t/CR$. CR is chosen to equal the same period t, so that $V_0 = -V_{in}$ by the end of the sample period, and therefore the integrator output = +2V.

If the second sample is also +2V, the output of IC_{25} will be (+2) − (+2) = 0V, i.e. there will be no difference between the two inputs. After the next strobe, 0V will be presented to the integrator input and, since $I_{in} = 0$, I_F must also be zero, and the output will remain at +2V. A third sample of −1V will make IC_{25} output (=2) − (−1) = +3V. This, when fed to the integrator, will cause it to fall linearly by 3V from +2V, resulting in a



The action of the step eliminator, using a waveform with a fewer number of steps than normally seen to illustrate the effect. The result of inaccuracy in the choice of integrator capacitors can be seen. Frequency in was 40kHz at 200 kHz sampling rate. Oscilloscope sweep 20μs/div., storage unit speed 2ms/div.



Pre-trigger of 5 divisions (graticule very faint). Large pulse is trigger.

Typical trace at 100 samples per cycle of the input.

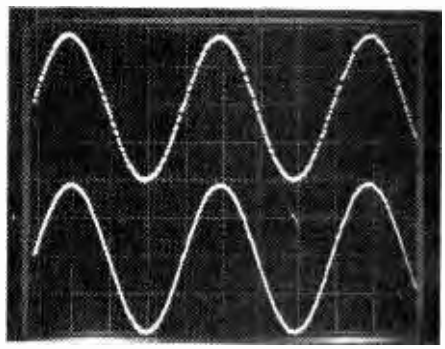
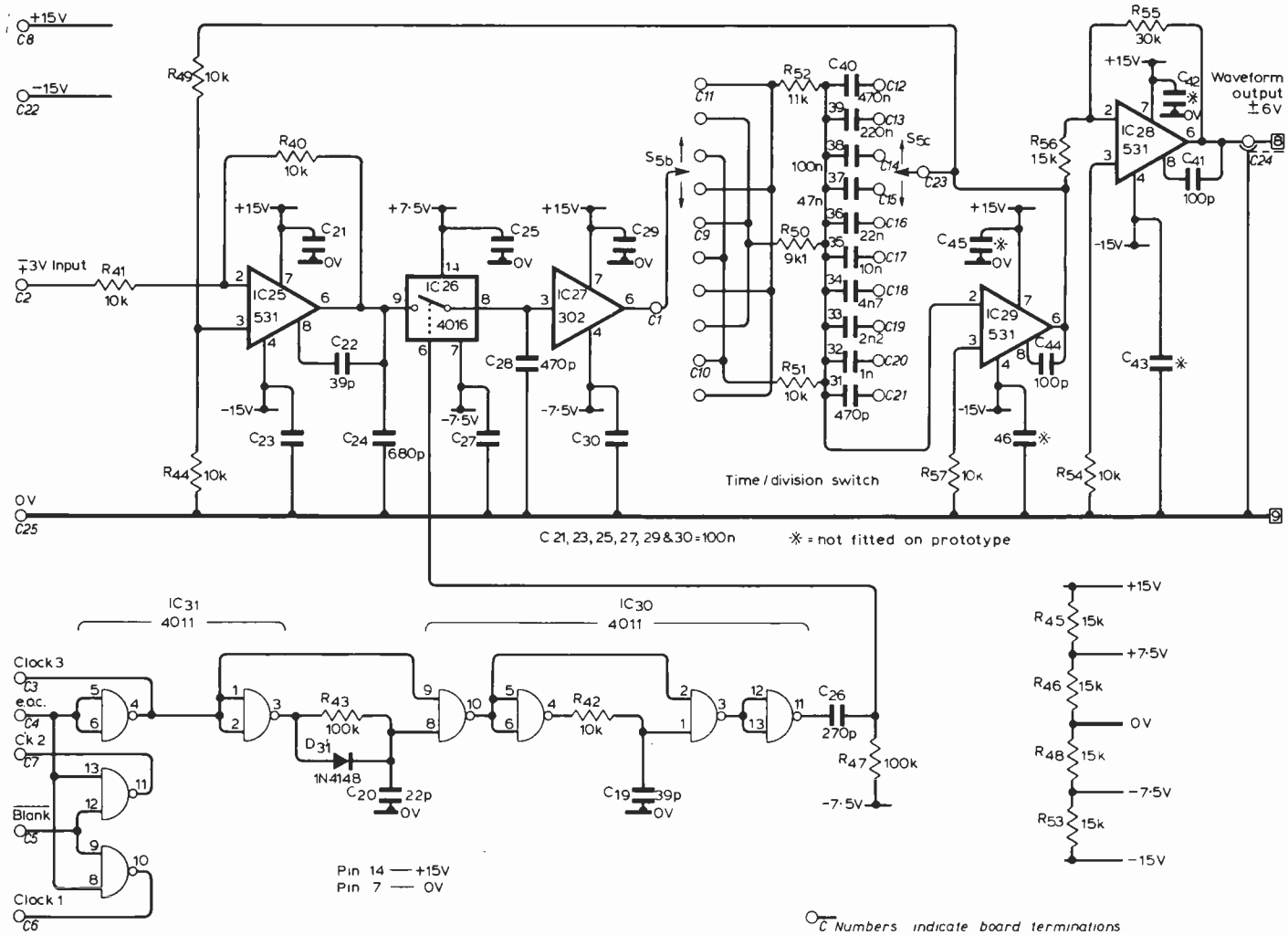


Fig. 5. Step eliminator and output amplifier. The faster ranges of the integrator should have close-tolerance capacitors to achieve the correct slopes.



voltage of −1V by the next strobe pulse. Photograph 1 shows the resulting effect, the slight errors in levels being due to the timing components not being selected for the correct time constants.

The input to the analogue gate is limited to slightly less than the supply voltage to the device. For the bipolar inputs required by the integrator, IC_{26} is operated from a ±7.5V supply. Thus, for safety, the input is limited to ±6V. This, in turn, limits the d.a.c. and integrator outputs to ±3V since, if both were at opposite extremes, the resulting output from IC_{25} would be ±6V.

Strobe pulse generation. The circuit, $IC_{30\text{-}31}$, consists of a positive transition detector, following an inverter, which gives a positive transition approximately 2.5μs after the negative-going edge of the e.o.c. pulse. This delay

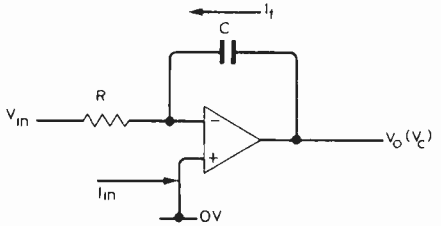


Fig. 6. Derivation of the integrator output voltage.

is required to allow for the data to emerge from the memory, the d.a.c. to settle and to allow the output of IC_{25} to charge C_{24} after the step input. The first positive transition detector is followed by a second one which gives a low going 0.5μs pulse after the positive going edge of the previous stage. Level shifting of the 0 to +15V pulse to −7.5V to +7.5V to be compatible with the gate IC_{26} is by capacitive coupling in C_{26} with a pull down to −7.5V by means of R_{47}. For use with oscilloscopes with 8 divisions horizontally the 1.8MHz crystal, which gives 1,000 samples in 10 divisions at 0.5ms/div., may be replaced with one of 2.25MHz or 1.125MHz. The former gives 1,000 samples in 8 div. at 0.5ms/div. and the latter 1,000 samples in 8 div. at 1ms/div. The higher of the two may be too high for the a-d converter to operate reliably, and the lower reduces the unit time/div. ranges to 9. The time constants of the step eliminator will need to be reduced from 5 to 4μs, 10 to 8μs and 20 to 16μs and their decades (330 + 69, 680 + 120pF, 1500 + 100pF used with 10kΩ).

Printed circuit boards

A set of four double sided p.c.bs is available, at £14.00, including postage and packing, from M. R. Sagin at 23 Keyes Road, London N.W.2.