GERARD ROBIDOUX AND
ROBERT DMITROCA*

LOGIC ANALYZER

Troubleshooting digital circuits is a cinch with this 16-channel, 50-MHz logic analyzer.

A LOGIC ANALYZER IS AN INVALUABLE tool for debugging complex digital circuits. Not only can it sample and store the state of a large number of digital signals, it can perform complex analysis on the signals to determine their timing and state relationships. The acquired data can be displayed on either a waveform screen or a state screen. With four different pull-down menus available, all the controls are right at your fingertips!

The essence of all digital logic circuits is the simultaneous operation of many signal paths. As an example, consider a typical desktop personal computer, such as the IBM PC. In order for the microprocessor to write to a single byte of memory, it must assert 20 address lines, 8 data lines, and over a half-dozen control lines. In total, over 34 signal paths must operate correctly and simultaneously for the computer to function properly.

When a digital circuit fails, it becomes very difficult to debug. Traditional diagnostic tools, such as the oscilloscope, can usually monitor 4 channels at the most. Other tools, such as logic probes, can only display the current state of a signal, and cannot be used to analyze how the signal varies with time.

Those problems led to the development of the logic analyzer. At its most primitive level, the logic analyzer may be considered to be an oscilloscope with a large number of channels, except that only the high-low state of a signal may be seen, rather than a continuous analog waveform. Commercial logic analyzers typically have 16 to 300 channels.

Until now, most logic analyzers have cost well over $1000, which has severely limited their use. Currently, most low-cost logic analyzers consist of cards which plug into personal computers. Those devices require a personal computer to operate and, therefore, are not very portable and tie up the resources of the computer.

Recent advances in CMOS and bipolar technologies, however, make it possible to build a practical, low cost, self-contained logic analyzer. We will show you how you can build a portable, 16 channel, 50-MHz logic analyzer, all for under $700!

Theory

Figure 1 shows a block diagram of the logic analyzer. Connection to the circuit under test is made through an acquisition "pod," or connector array, which contains a set of wires terminated with test clips. The clips are used to attach to the various points in the circuit being tested.

All of the lines contained in the acquisition pod are inputs; the logic analyzer never sends a signal to the device it is connected to. The pod also contains clock and ground inputs as well as data-input lines. More sophisticated units may also contain inputs that qualify the clock, inhibit triggering until certain conditions are met, and so on.

Signals coming in from the acquisition lines enter voltage comparators, which are used to periodically sample the input sig-

*Gerard Robidoux and Robert Dmitroca are partners in Convention Systems, a software consulting company specializing in the design of low-cost test instrumentation.

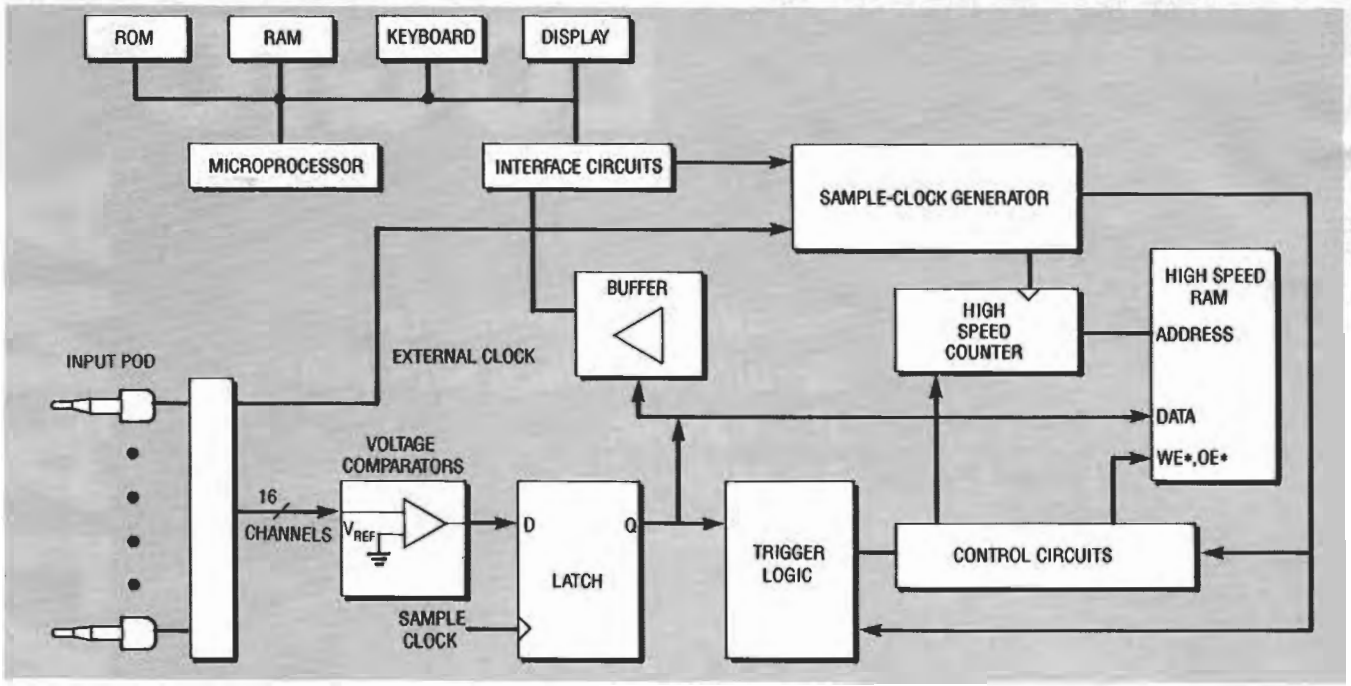

FIG. 1—A BLOCK DIAGRAM OF THE LOGIC ANALYZER. Signals from the acquisition lines enter the voltage comparators and are sampled by the input latches; they then flow into the high-speed RAM and the trigger logic. The final stage is the user interface.

nals and determine their logic level. All logic families have a defined high and low level. For example, the TTL logic family defines a low as a voltage between 0 and 0.8 volts, and a high between 2.4 and 5.0 volts. Some logic analyzers have a variable voltage-threshold, which allows you to define the high and low voltage levels depending on your particular application.

The logic analyzer that we present here recognizes only TTL and 5-volt CMOS levels. Since the vast majority of digital logic is designed with those two families, that's not a serious limitation, and it also eliminates the need for expensive high-speed voltage comparators.

After voltage comparison, the signals entering the logic analyzer are sampled by the input latches. Digital storage scopes (DSO's) use the same sampling technique. The sampling rate is determined by an internal timebase, or from an external clock input. The sampling rate is usually adjustable in a 1-2-5 sequence from a very high frequency to a very low frequency (a few hundred MHz to less than 100 Hz).

With a very fast clock, you can see the operation of the circuit in great detail for a very short period of time. With a slow clock you can see the operation of a circuit for a longer time, but with less accuracy. If you were debugging a high speed digital circuit, such as a microprocessor, you would use a very fast clock. A slower clock would be used to troubleshoot a very slow circuit, such as a 1200-baud serial interface.

The external CLOCK input is used when you want the sampling rate to be controlled by an external circuit. A good example of that is when you attach a logic analyzer to the data and address lines of a microprocessor to trace program execution. The logic analyzer's external CLOCK line is connected to a memory strobe line, such as $\overline{AS}$* (68000 family) or $\overline{ALE}$* (8088 family). The logic analyzer would then capture the status of the processor at each bus cycle.

After being captured by the input latches, the input signal data flows to two places; the high speed RAM and the trigger logic. Let's take a close look at the trigger logic first.

In most digital designs, we're interested in the operation of the circuit at a very specific point. The action of the trigger logic allows us to obtain only that range of data in which we are interested. For each of the signals being monitored, we can specify a trigger pattern of high, low, or "don't care" (either high or low). When the logic analyzer is enabled, it will continuously sample the input data lines until the trigger pattern is recognized. At that point, sampling will either stop, or continue for a preset number of samples. That feature lets us see the state of the signals occurring before, or, perhaps, both after the trigger point.

The high speed static RAM stores the values of the input channels being monitored. That RAM is often known as the acquisition data buffer, since it provides a storage space for the data being acquired from the input data lines.

Notice that a logic analyzer, unlike an oscilloscope, is not a "real-time" device. An oscilloscope can immediately and continuously shows the voltage at the probe. The logic analyzer, on the other hand, stores the signal data until a trigger pattern is recognized. The

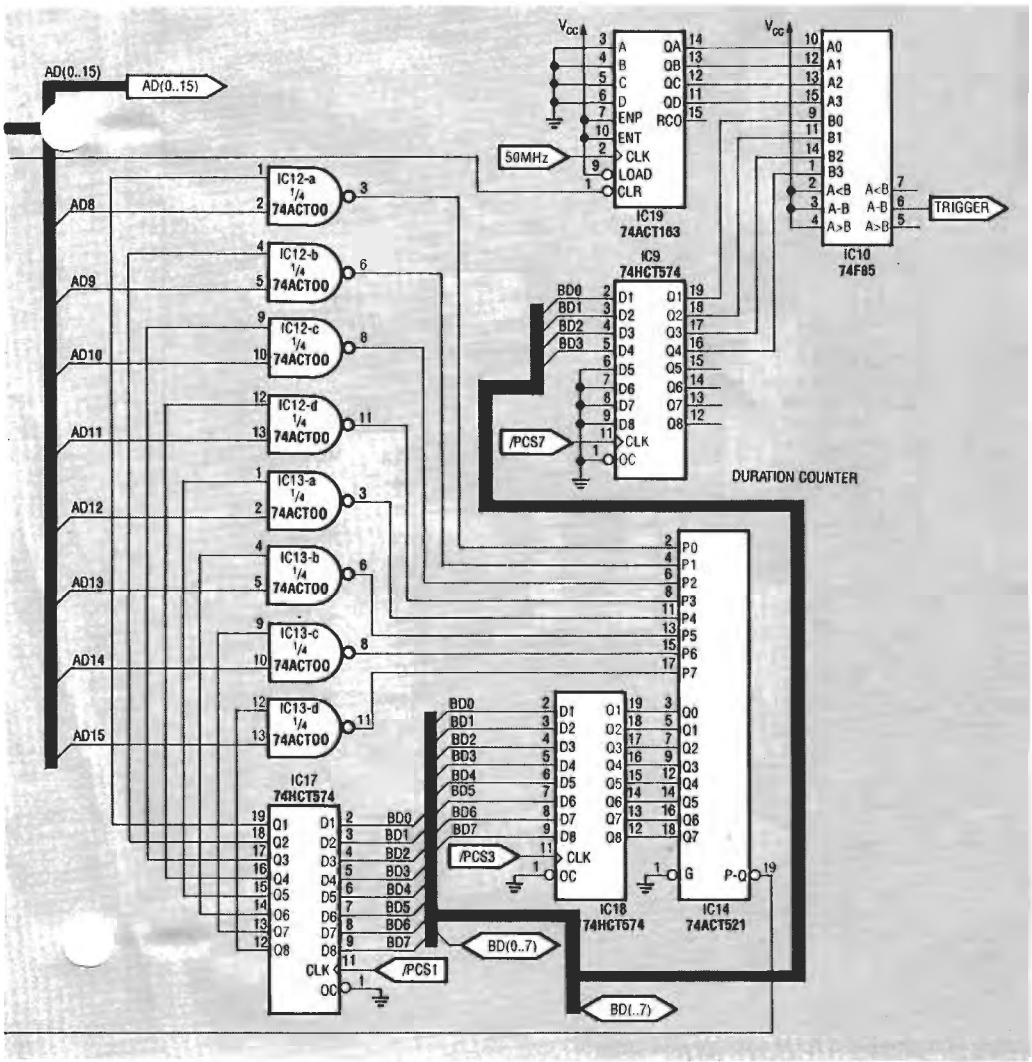

FIG. 2—INPUT BUFFERS AND TRIGGER LOGIC. The input pod contains 16 data-channel inputs, an external clock input and a ground connection. The input data enters resistor arrays RA1 and RA2, and into latches IC1 and IC11. The acquired data is routed into the trigger logic and to the high-speed RAM.

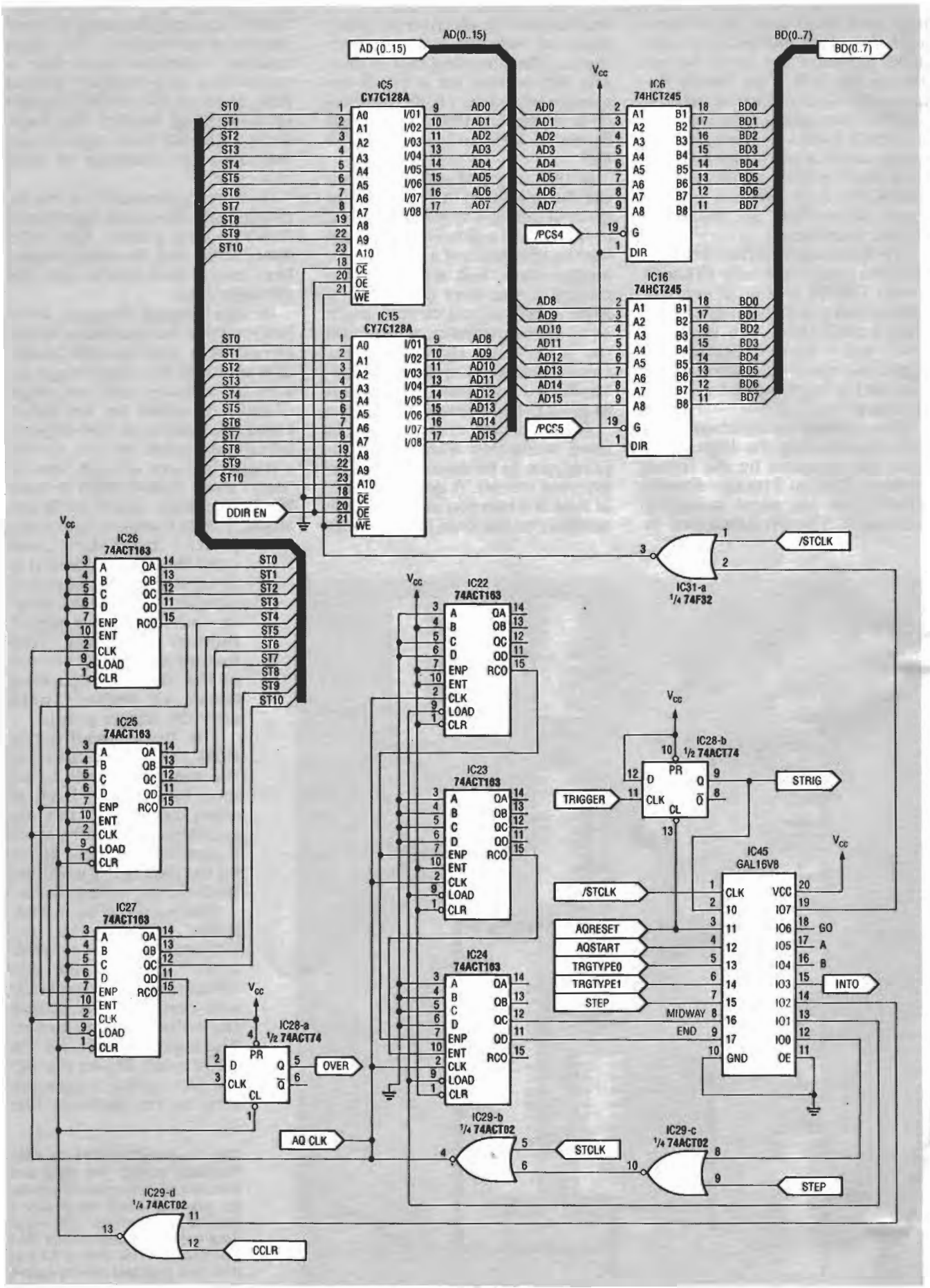

FIG. 3—THE ACQUISITION SECTION, consisting of high-speed RAM storage and control logic, is the heart of the logic analyzer.

signal data is shown only after that has occurred.

The last section of the logic analyzer is the user interface, which consists of a keyboard and display that are built right into the unit.

Circuit description

Now that we've looked at the block diagram of the logic analyzer, we'll turn our attention to how the unit operates. The schematic in Fig. 2 shows the input pod and trigger logic. The input pod connector, J1, contains 16 data-channel inputs, the external clock input and the ground lead connection. It also carries other signals that can be used by external pods.

The data to be sampled goes into J1, through resistor arrays RA1 and RA2, and into latches IC1 and IC11. The level of each channel is latched using the AQ—CLK signal (the sampling clock). Pull-up resistors RA1 and RA2 drive the inputs of the latches high if nothing is connected to the input. The acquired data (AD[0..15]) is routed to the trigger logic and to the high speed RAM storage (Fig. 3).

The trigger condition of the input data may be set to high, low, or "don't care." The "don't care" circuits for the first eight inputs are formed from IC2, IC3, and IC7, and the last eight inputs from IC12, IC13, and IC17. If an input is set to a "don't care" condition, the input of the corresponding NAND gate is set low. That forces the output to be high regardless of the input from the data latch. If the NAND input is set low, the data is simply inverted.

The outputs from the NAND gates are presented to the eight-bit comparators, IC4 and IC14. The output of those IC's (pin 19) goes low whenever the P and Q inputs match.

Masking of IC8 and IC18 latches is performed by the following technique. If the trigger bit to either IC is low, a high is written to the latch. Similarly, if the trigger bit is high, a low is written. For "don't care" conditions, a high value must be written, since we have forced the P input to high (by disabling the NAND gate). The upper and lower trigger outputs of IC29-a forms an active-high trigger output.

PARTS LIST

All resistors are ¼-watt, 5%, unless otherwise indicated.

R1–R8–10,000 ohms
R9—470 ohms
R10—0 ohms, or jumper wire
RA1, RA2—1 megohm, 10-pin bussed SIP resistor array

Capacitors
C1–C11, C13–C20, C23, C25, C27–C38, C40–C49, C58–C60—0.1 µF, ceramic axial
C12, C24—3.3 µF, 10-volt tantalum
C21, C22—10 pF, ceramic disc
C26—100 µF, 25-volt tantalum
C39—50 pF, ceramic disc
C50–C57—22 µF, electrolytic

Semiconductors
IC1, IC11—74ACT574 8-bit latch
IC2, IC3, IC12, IC13—74ACT00 quad 2-input NAND gate
IC4, IC14—74ACT521 8-bit comparator
IC5, IC15—CY7C128A 2K×8 15-ns static RAM (SRAM)
IC6, IC16—74HCT245 octal transceivers
IC7–IC9, IC17, IC18, IC39—74HCT574 8-bit latch
IC10—74F85 4-bit comparator
IC19, IC22–IC27—74ACT163 4-bit counter
IC20—74HCT138 3-to-8 demultiplexer
IC21—TL7705A voltage supervisor and reset control
IC28—74ACT74 dual D-type flip-flop
IC29—74ACT02 quad 2-input NOR gate
IC30—V25 high-integration microprocessor
IC31—74F32 quad 2-input OR gate
IC32—74ACT86 quad 2-input XOR gate
IC33—74F160 4-bit counter
IC34—74ACT153 dual 4-to-1 mulitplexer
IC35–IC37—74LS390 dual bi-quinary counter
IC38—74ACT151 8-to-1 mutiplexer
IC40—Dallas Semiconductor DS1213C "Smart Socket" and 32K×8 100-ns SRAM or Dallas Semiconductor DS1235 integrated battery backed RAM
IC41, IC42—MAX232 RS-232 tranceiver and charge pump
IC43—7805 5-volt regulator
IC44—GAL16V8-15LP PLD
IC45—GAL16V8-10LP PLD
IC46—128K×8 250-ns EPROM
LCD panel—Sharp part no. LM24014W

Other components
XTAL1—16-MHz HC-49 crystal
XTAL2—20-MHz 14-pin DIP package oscillator
XTAL3—50-MHz 14-pin DIP package oscillator
Case—Pactec CM69-120
Key switches (12)—75120-002/0000
AC adapter—9 VDC at 1 amp secondary output

Connectors
J1—Right-angle DB37 connector
P2–P4—3-pin socket strip
J3—Right-angle DB9 connector
J4—20-pin socket strip (2×10)
P1—7-pin socket strip (1×7)
J2—Power connector (2.3-mm barrel)
Keyboard—7×1 row-header
Acquisition clip—DB37 connector with 18 wires and micro-clips.
P1—2×10 row-header connector for LCD panel

Sockets
20-pin machined sockets for IC1 and IC11
32-pin socket for IC46
14-pin machined socket for IC32
84-pin PLCC socket for IC30

Hardware
4 ⅜-inch standoffs with 4-40 internal thread
4 ⅝-inch standoffs with 4-40 internal thread
18 4-40 screws with pan head, ¼-inch length
2 4-40 nuts
1 TO-3 heatsink and heatsink grease

The minimum trigger-duration circuit is made from IC9, IC19, and IC10. That circuit ensures that the trigger is present for a minimum amount of time before the trigger pattern is actually recognized, which prevents glitches from causing a false triggering to occur.

The desired trigger-duration count is contained in the latch of IC9. Whenever the trigger pattern occurs, 4-bit counter IC19 is enabled. That counter runs at 50 MHz (20 ns per count). When the desired duration count and the counter value match, the TRIGGER output (pin 6 of IC10) will go high, indicating that a valid trigger pattern has been recognized. If the trigger disappears before the desired duration count has been reached, the counter is cleared. It will start over when the trigger becomes valid again.

The circuit shown in Fig. 3 contains the heart of the logic analyzer: the high speed RAM storage and the control logic. Data for the lower eight channels is stored in IC5, while IC15 stores the data for the upper eight channels. Both IC5 and IC15 are 2K×8 15-ns SRAMS.

An 11-bit binary counter is formed from IC25, IC26 and IC27. That counter drives the address inputs of the RAM IC's. The

address is incremented by 1 for each cycle of the AQ—CLOCK (acquisition clock) signal.

The TRIG function lets you specify the position of the trigger position within the acquisition data buffer. When PRE is selected, the trigger is set at the start of the buffer. When the trigger condition is met, data is sampled until the entire acquisition buffer is filled. In the MID trigger mode, the trigger point is set at the middle of the data buffer. The first half of the buffer may or may not contain data that was sampled before the trigger point. In the POST trigger mode, storage of data will stop immediately after the trigger condition is recognized.

An 11-bit binary counter is formed from IC22, IC23, and IC24. That counter holds the current position within the acquisition data buffer. The position counter is reset whenever the trigger condition is recognized, after which it is incremented by 1 for each cycle of the AQ—CLOCK signal.

The acquisition section control is formed by IC45, IC29, and portions of IC28 and IC31. The TRIGGER output from IC10 to a constant high level (STRIG) is converted by IC28-*b*. A finite state machine, IC45, coordinates the signals coming in from the microprocessor, trigger logic, and position counters, and generates the appropriate outputs to control the acquisition cycle.

TRGTYPE0 and TRGTYPE1 are used to inform the state machine where the trigger should be positioned in the acquisition buffer (for example, they set the PRE, MID, or POST modes). AQSTART tells the logic analyzer to begin looking for the trigger condition, and to start storing data into the acquisition buffer. The MIDWAY and END signals from the position counters tell the state machine how much buffer has been filled since the trigger.

When a trigger has been recognized and the acquisition buffer filled up, the state machine will assert the INTO line, informing the microprocessor that acquisition data is now available.

The STEP, CCLR, and DDIR—EN

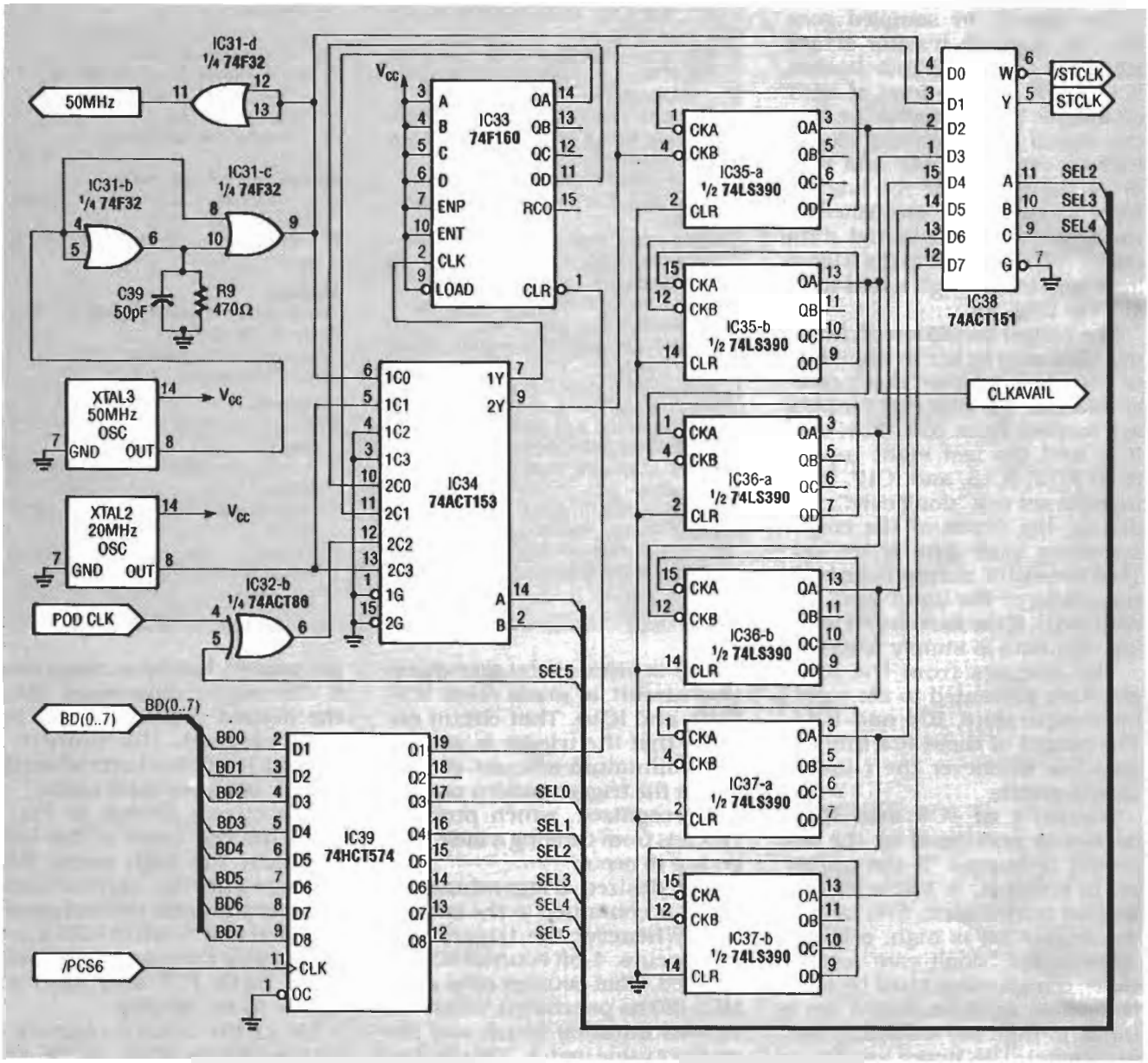

FIG. 4—CLOCK GENERATOR AND TIMING LOGIC. The logic analyzer can generate 22 internal frequencies, ranging from 50 MHz to 5 Hz.

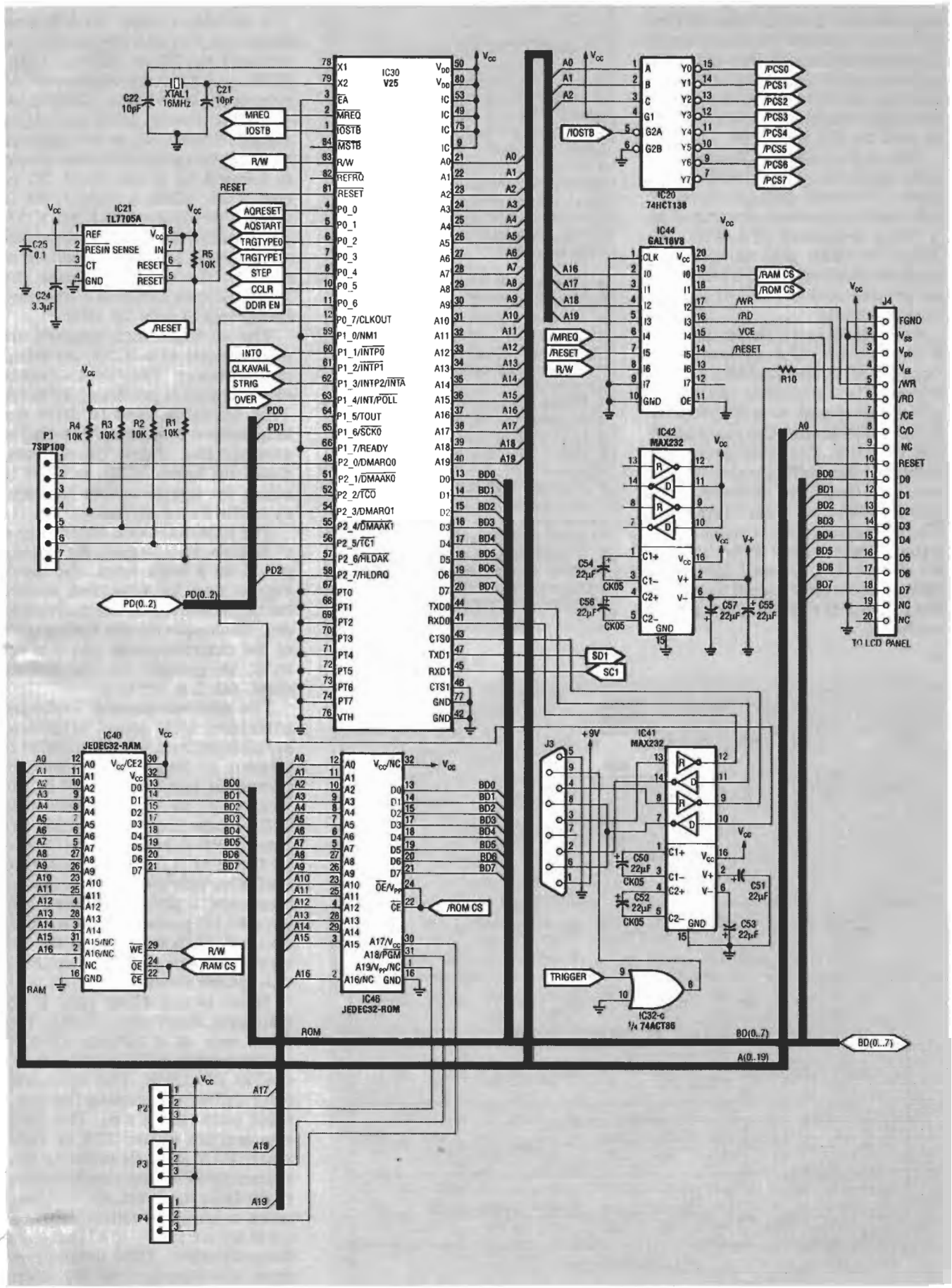

FIG. 5—THE PROCESSOR SECTION contains the microprocessor, keyboard interface, LCD panel interface, serial interface, RAM, and ROM.

signals are used by the microprocessor to copy the contents of the acquisition buffer into the microprocessor's own RAM for further manipulation. Data from the high speed acquisition RAM is read by IC6 and IC16.

Figure 4 shows the clock generator and timing logic for the analyzer. The unit can generate 22 internal frequencies arranged in a 5-2-1 sequence (50 MHz, 20 MHz, 10 MHz, and so on). The highest frequency is 50 MHz (20-ns period) and the lowest is 5 Hz (0.2-s period).

Self-contained TTL oscillators, XTAL2 and XTAL3, generate the base 50-MHz and 20-MHz square waves. The duty cycle of the 50-MHz waveform is adjusted by IC31-b, IC31*c* and the associated R-C network. The timing requirements of the high speed RAM IC's require that the write-enable pulse width be at least 13 ns long. The 50-MHz oscillator produces a square wave with a 50% duty cycle (10 ns low, 10 ns high). The circuit is therefore used to adjust the duty cycle to 35% (13 ns low, 7 ns high).

ORDERING INFORMATION

Note: The following items are available from Convention Systems, 1214-315 Southampton Dr. SW, Calgary AB, Canada T2W 2T6, (403) 253-4427. Send check or money order. Shipping is by ground delivery. Contact Convention Systems for additional charges if overnight delivery is desired. All items are postpaid, except as noted.

- **Etched, drilled and plated main and keyboard PC boards—$99.00.**
- **Preprogrammed EPROM, GAL16V8-15LP, and GAL16V8-10LP (IC44–IC46)—$99.00**
- **Milled-out case with plastic overlay—$79.00.**
- **Probe assembly—$99.00**
- **AC adapter—$15.00**
- **LCD panel—$150.00**
- **IC30 V25 microprocessor—$29.00**
- **Manual—$32.00**
- **Complete kit, including probe assembly and AC adapter—$695.00 plus $20.00 S & H.**
- **A complete assembled unit, including probe assembly and AC adapter—$695.00 plus $20.00 shipping and handling.**

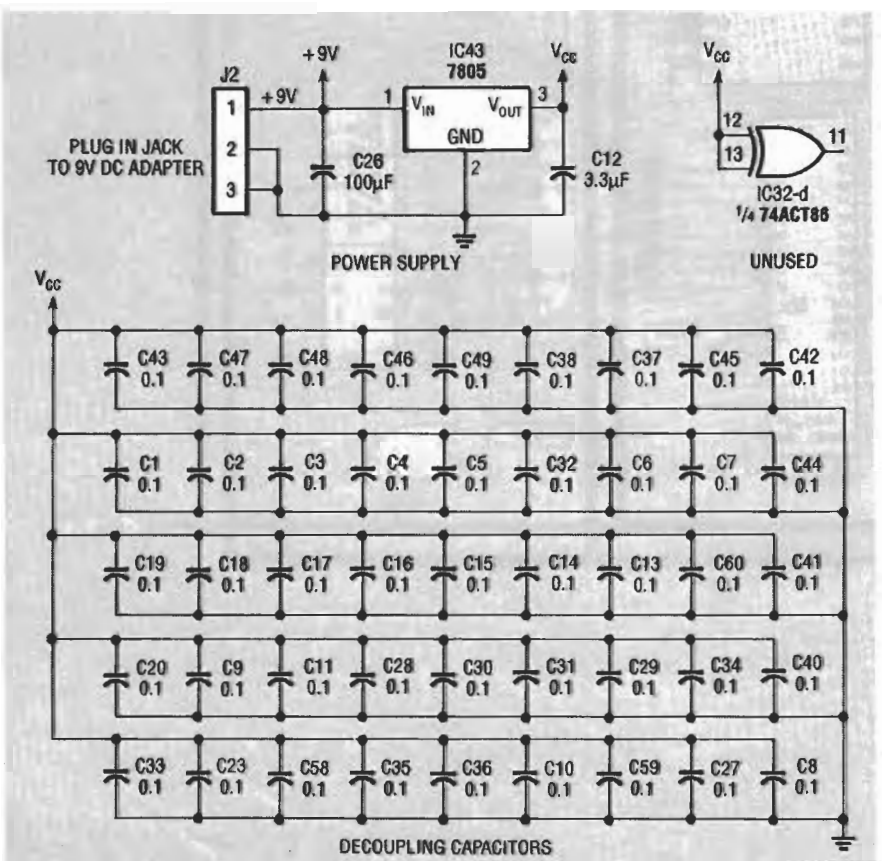

FIG. 6—POWER CIRCUIT AND DECOUPLING CAPACITORS. Each IC is decoupled by a 0.1 µF capacitor.

A divider chain, which produces the 22 clock frequencies, is formed by IC33, IC34, IC35, IC36, and IC37. Multiplexer IC34 selects the 50-MHz or 20-MHz oscillators, the 25-MHz or 5-MHz signals from IC33, or the external K line. A bi-quinary divider chain is formed by IC33, IC35, IC36, and IC37. IC33, a 74ACT160, is similar in function to IC35-IC37, which are 74LS390 dual-decade counters. It is used at the beginning of the chain because the 74LS390 can handle a maximum frequency of only 20 MHz.

The various clock sources are multiplexed into IC38, an 8-to-1 multiplexer. The STCLK (state clock) signal is produced by IC38. That signal is used to drive the acquisition state machine and to sample the input data lines. Eight-bit latch, IC39, is used to select the source and/or frequency of the STCLK signal.

The external clock enters pin 4 of IC32-b, an XOR gate. By setting pin 5 to a high level, the clock signal can be inverted before being presented to the multiplexers. To sample on the rising edge of the external clock, pin 5 is set to 0. To sample on the falling edge, pin 5 is set to 1.

The microprocessor, keyboard interface, LCD panel interface, serial interface, RAM and ROM is shown in Fig. 5. The microprocessor used is the V25 (IC30) from NEC electronics, which is 100% code compatible with the Intel 8088 microprocessor (used in the IBM XT class of computers). The V25 includes two serial channels, a DMA controller, and parallel I/O ports. Using this part allowed us to implement the entire microprocessor section using only seven IC's!

There is one ROM site, IC46, and one RAM site, IC40. The ROM site is a 32-pin JEDEC socket which will accept 1-, 2-, or 4-Mbit EPROMS. The logic analyzer software currently fits in a 1 Mbit part (128K × 8). The RAM site accepts either 32K or 128K static RAM IC's. In order to permanently store the configuration of the logic analyzer, the RAM site uses a Dallas semiconductor component called a SmartSocket. That device consists of a standard socket, along with a 3-volt lithium battery, and

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LOGIC ANALYZER

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a controller chip. Coupled with a standard low-power SRAM, the SmartSocket provides all of the benefits of standard non-volatile memory. The logic analyzer currently uses a 32K × 8-RAM.

The TTL levels of the V25 are converted to RS-232 levels by IC41, a Maxim MAX232 RS-232 transceiver. The part requires only a +5-volt supply and has integral charge-pumps to create the necessary −10-volt and +10 volt RS-232 levels.

The negative contrast-voltage for the LCD panel is generated by IC42, also a MAX232 chip. The V25 address and control lines are decoded by IC44 and IC20 to produce device selects for the memory, LCD, and control registers. A programmable logic device (PLD) from Lattice Semiconductor, IC44, (a GAL16V8) produces the control signals required by the LCD panel. It also generates the RAM and ROM chip selects. The chip selects for the registers which control the logic analyzer section are produced by IC20.

The LCD is a 240 × 64 pixel graphics display with built in RAM, controller, and microprocessor interface. That display allows the logic analyzer to run a true windowed graphics interface under the control of the V25.

The TL7705 is a reset and power-supply monitor circuit. It produces a glitch-free reset signal on power up. It will also reset if the drops below 4.75 volts.

Each IC on the circuit board is de-coupled using a 0.1 μF capacitor. That is shown in the large capacitor array in Fig. 6. The power supply uses a standard three-terminal voltage regulator, IC43. Because the logic analyzer draws approximately 600 mA, a TO-3 type case and heat sink are used.

The analyzer is powered from a plug-in wall transformer which supplies an unregulated 9 volts DC. Note that the logic analyzer can also run off batteries. Six D-cell alkaline batteries will run the analyzer for over eight hours.

Next month when we continue, we'll show you how to build the logic analyzer, and how to use it to troubleshoot circuits. **R-E**

LOGIC ANALYZER

GERARD ROBIDOUX AND
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Troubleshooting digital circuits is a cinch with this 16-channel, 50-MHz logic analyzer.

LAST MONTH WE INTRODUCED THE 16-channel, 50-MHz logic analyzer. We discussed all the capabilities of this digital-test instrument, and the theory behind its operation. This month we'll show you how to build it.

Construction

The logic analyzer consists of two PC boards, a case, and an overlay. Due to the extremely high-speed logic used in this design, it is critical that PCB's be used. Wire-wrap and point-to-point construction techniques will not work!

A photo of the inside of an assembled unit is shown in Fig. 7. The main logic board has four circuit layers: two signal layers, one power, and one ground plane. The PC board can only be fabricated by a fairly sophisticated board vendor. Because of that, foil patterns have not been provided in this article. A finished board and all the required parts, however, are available from the source mentioned in the Parts List. Figure 8 shows an internal photo of the unit with the LCD panel removed.

Figure 9 shows the parts-placement diagram. Make sure you observe the correct component orientation and capacitor polarities when soldering the components. Assemble the keyboard first, because it is the simplest circuit. Note how the keys are placed on the component side of the circuit board, as shown in Fig. 9. The keyboard connector, P1, must be placed on the solder side, in the position that is shown.

When soldering the keys, S1–S12, pay particular attention to their alignment. They must be straight with respect to the edge of the board and to each other, otherwise the cutouts in the case will not fit over them.

When you've finished soldering in the components, all flux *must* be removed from the circuit boards. We recommend that solder with a water-soluble flux be used, rather than the standard rosin core. Rosin-core flux must be removed with a freon based solvent, which is quite expensive. Water-soluble flux, however, can be cleaned off with warm tap water and a small brush (a toothbrush is remarkably effective). Kester solder with type 331 flux is a good one to use.

Assembling the main circuit board is also straightforward. Install all mechanical components as shown in Fig. 10. Most of the components on the main board are CMOS, therefore they're quite sensitive to static electricity. Make sure you follow adequate precautions when handling those IC's. When assembling the main board, it is critical that you use a properly grounded three-wire soldering iron, and that your workbench is covered with an anti-static mat to avoid damage to the CMOS IC's.

Solder in all of the IC's and sockets first. Notice that IC1, IC2, IC30, IC32, IC40, IC44, IC45, and IC46 are socketed. The socket for IC30 has pin 1 facing to the left. The socket for IC40 is a Dallas Semiconductor Smart Socket. It does not use all of the

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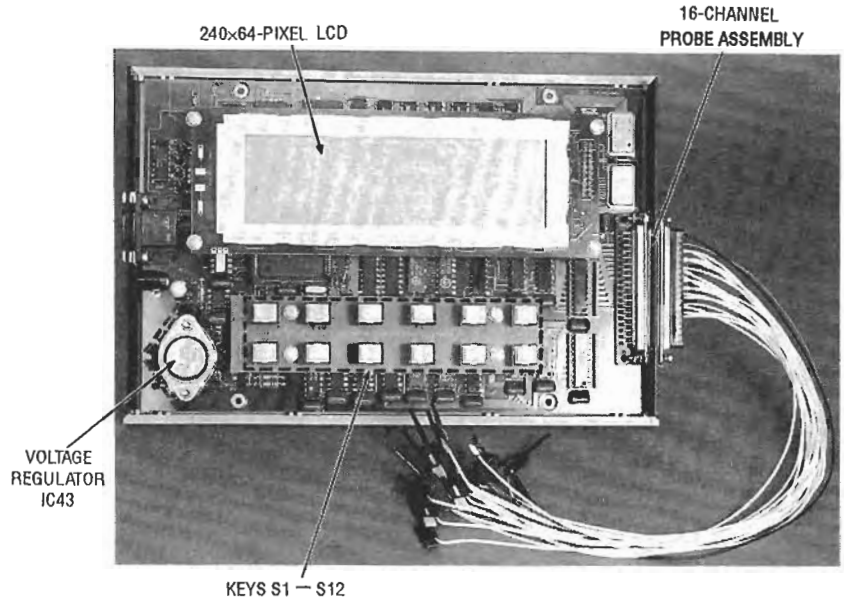


FIG. 7—INTERNAL PHOTO OF the logic analyzer. The main PC board has four layers: two signal layers, one power, and one ground plane. Wire wrap and point-to-point soldering techniques cannot be used because of extremely high-speed logic.

holes provided for IC40. Align that part in the lower part of the socket.

The capacitors and resistors should then be added, followed by connectors J1–J4, P1, and the header blocks P2–P4. Attach the heatsink to the voltage regulator, IC43, using a thin layer of conductive heat-sink cream. Secure that assembly to the board using ½-inch 4-40 screws, washers, and nuts.

The circuit board must be jumpered to work properly with the size of SRAM and ROM being used. To accomplish that place shorting blocks between P2 (pins 1-2), P3 (pins 2-3), and P4 (pins 2-3).

That completes the assembly of the main logic board. After cleaning the board of flux, carefully inspect it for good solder connections and make sure there are no solder bridges present. Touch up any cold or questionable solder joints.

Carefully inspect the alignment of all of the components. Insert the V25 microprocessor (IC30) into its socket. Make sure that pin 1 is aligned correctly. It's very difficult to remove a PLCC device from the socket once it's been inserted. Insert components IC1, IC11, IC44, IC45, and IC46. IC44 and IC45 are programmable logic devices (PLD's).

Acquisition connector

The acquisition clip assembly consists of a DB-37 connector shell containing eighteen wires terminating in small micro-clips. It is supplied in a pre-assembled format.

There are three separate parts to each micro-clip assembly; the wire, the body, and the plunger. Each part can have a different color. The color coding is used to separate the function of the input lines; all data input channels have a white wire, the clock wire is green, the ground wire is black.

The plunger and body are used to distinguish the input channel numbers. Channel 0 has a black plunger and a black body, channel 1 has a brown plunger and a black body, channel 2 has a red plunger and a black body, and so on. Table 1 lists the cap, plunger, and wire color coding of the probe assembly.

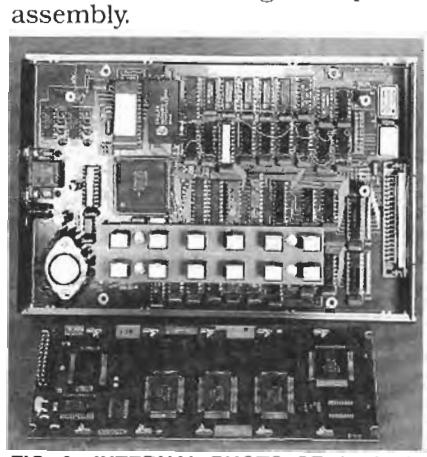


FIG. 8—INTERNAL PHOTO OF the logic analyzer with the LCD panel removed.

Final assembly

We're now ready for final assembly. To connect the LCD panel to the main logic board, connector P4 must be soldered onto the display. Connect P4 to the bottom side of the LCD panel (away from the LCD panel itself).

To complete the mechanical assembly, attach four ⅝-inch and four ⅜-inch standoffs to the circuit board as shown in Fig. 10. The shorter standoffs are used for the keyboard. Align the keyboard connector and attach it to the main circuit board. Do the same for the LCD panel.

Checkout

At this point we're ready to test the logic analyzer. Measure the resistance between pin 20 and pin 10 of IC1 (the power pins). The resistance should be above 20 ohms. If it's below that value, there's a short somewhere on the board. Do not power the unit up until you find it!

Plug the AC adapter into the wall outlet then plug it into J2. The LCD panel should display a brief title-page before running the software. (You can become familiar with the software running on the logic analyzer by reviewing the introductory sections in the manual provided with the kit or with the ROM). If you don't see the title page, then there's a problem with the microprocessor section (IC30, IC40, IC42, IC44, and IC46). The LCD contrast voltage at R10 should be around −10 volts. The voltage at IC1 pin 20 (+5-volt power supply) should be between 4.75 and 5.1 volts.

We will now test the internal clock generator circuits. For that test, you'll need a 100-MHz counter. Connect the counter to pin 5 of IC38. Go to the SYSTEM screen and select an internal clock. Then select each clock speed in turn. For each clock speed, make sure the counter shows the same speed on the display (for example, if a 10-MHz clock has been selected, the counter should show 10 MHz).

You can check the external clock signal input by selecting the external clock function. Using a function generator, place a TTL-level signal of a known frequency into the CLK pod. The counter should show the function generator's frequency.

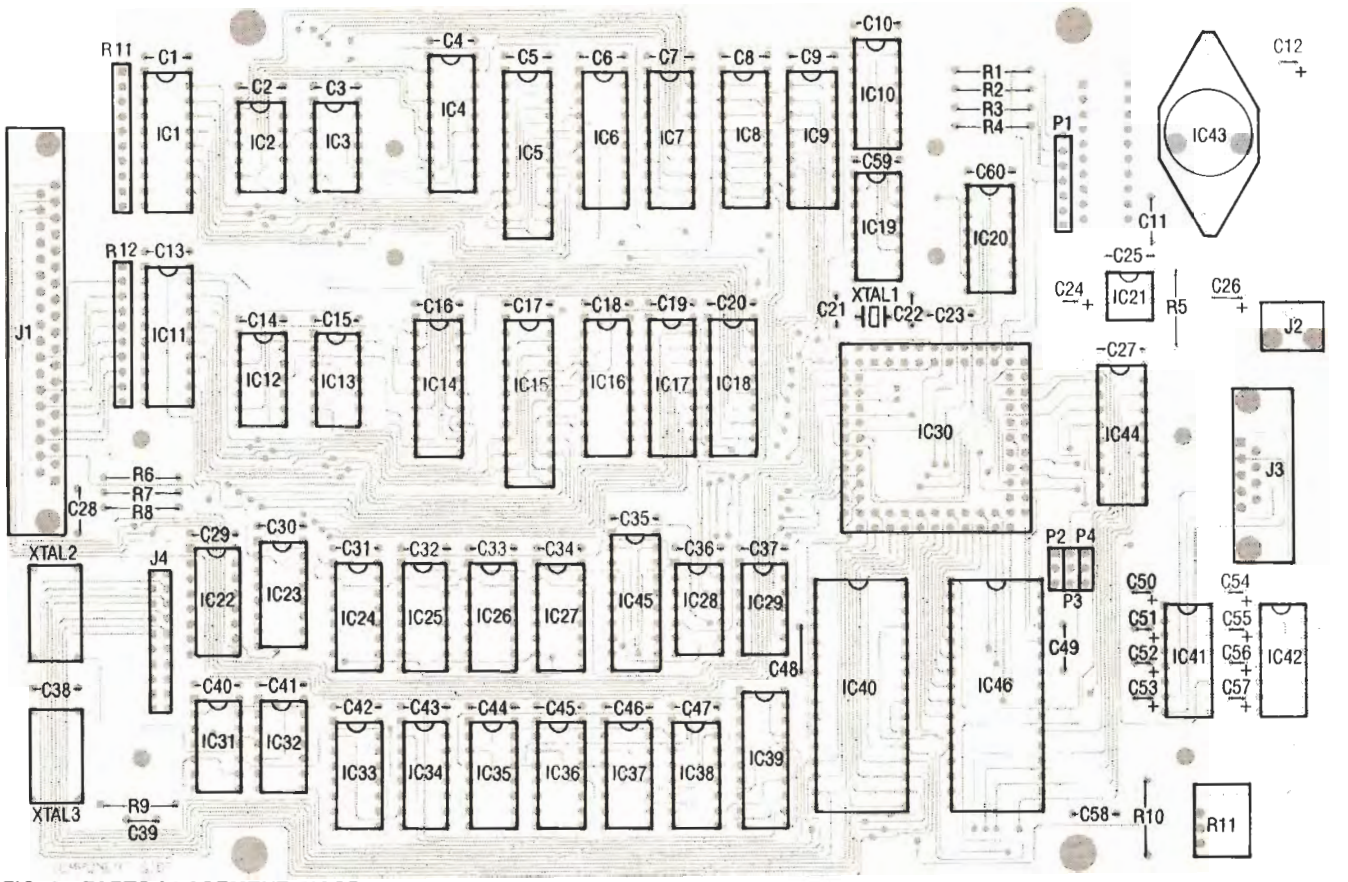


FIG. 9—PARTS-PLACEMENT DIAGRAM.

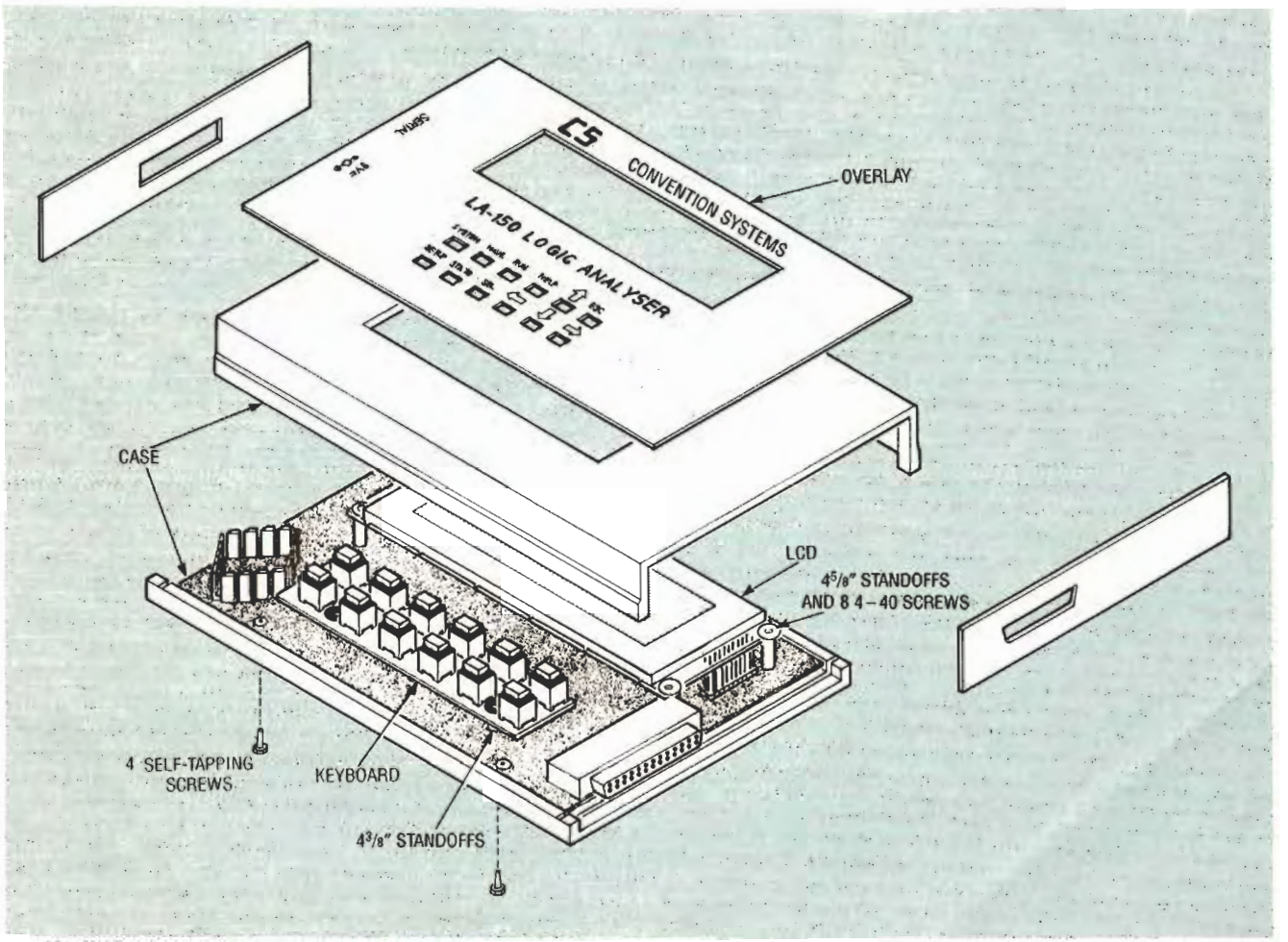
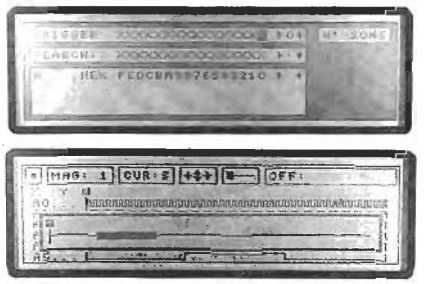


FIG. 10—THE ASSEMBLY DRAWING SHOWS how the case is secured together.



THE SETUP SCREEN is shown in the top display. The bottom screen shows a large block indicating the size and position of data and its location relative to the entire acquisition data.

Go to the SEARCH field on the setup screen. Select it using the SEL key, and change it to the INPUT item. Make sure the acquisition clip assembly is connected to the logic analyzer. Briefly touch each input channel clip to the ground clip. That grounds the channel. Verify the display shows a low symbol, when the clip is touching the ground clip, and a high symbol, when the clip is not touching. That verification tests the input buffers, acquisition RAM, and microprocessor interface.

All we have left to test is the trigger logic. First set the trigger word to all "1's" (for example, TRIGGER = "1111111111111111"). Press the RUN key. Two messages should flash briefly on the screen, and the logic analyzer should return to you immediately. Now set the trigger to "111111111111110" (trigger when channel 1 is low and all others are high). Press RUN. The "WAITING FOR TRIGGER CONDITION" message should remain on the screen until the channel 0 clip is touched to the ground clip. Repeat that procedure for all sixteen channels. All of the circuits have now been tested.

Now it's time to put the circuit boards into a case, which comes in four pieces; the top, bottom, and side panels. The top and bottom halves of the case contain grooves on the front and back. It's important that the boards be placed with the keyboard closest to the side with the raised groove of the bottom piece. The main circuit board will fit tightly over four plastic standoffs which have been molded into the bottom of the case. It may be necessary to press firmly on the circuit board to force the holes over the standoffs. The two side pieces can then be slipped over the connectors on the appropriate ends. After that's been done, the top piece is slipped over the keyboard and attached to the bottom piece using four self-tapping screws.

At this point, make sure the keyboard and display are straight with respect to the edges of their cutouts. The overlay must now be applied to the top piece. The wax paper sheet on the back of the overlay must be removed to reveal the pressure-sensitive backing.

A word of caution regarding the glue used: once it's been pressed down on the case the overlay, it cannot be moved without destroying the overlay and the case. This glue has no respect for mistakes! Peel the entire wax paper sheet off. Use great care in positioning the overlay over the keys of the keyboard. Make certain that the overlay is true to the edge of the case. Gently press the overlay down. At this point it's still possible to move the overlay, but once pressure is applied, however, the overlay cannot be moved. Working from the center of the overlay out, smooth the overlay down, being careful not to catch air bubbles.

PARTS LIST

All resistors are ¼-watt, 5%, unless otherwise indicated.
R1–R8–10,000 ohms
R9—470 ohms
R10—0 ohms, or jumper wire
RA1, RA2—1 megohm, 10-pin bussed SIP resistor array

Capacitors
C1–C11, C13–C20, C23, C25, C27–C38, C40–C49, C58–C60—0.1 µF, ceramic axial
C12, C24—3.3 µF, 10-volt tantalum
C21, C22—10 pF, ceramic disc
C26—100 µF, 25-volt tantalum
C39—50 pF, ceramic disc
C50–C57—22 µF, electrolytic

Semiconductors
IC1, IC11—74ACT574 8-bit latch
IC2, IC3, IC12, IC13—74ACT00 quad 2-input NAND gate
IC4, IC14—74ACT521 8-bit comparator
IC5, IC15—CY7C128A 2K × 8 15-ns static RAM (SRAM)
IC6, IC16—74HCT245 octal transceivers
IC7–IC9, IC17, IC18, IC39—74HCT574 8-bit latch
IC10—74F85 4-bit comparator
IC19, IC22–IC27—74ACT163 4-bit counter
IC20—74HCT138 3-to-8 demultiplexer
IC21—TL7705A voltage supervisor and reset control
IC28—74ACT74 dual D-type flip-flop
IC29—74ACT02 quad 2-input NOR gate
IC30—V25 high-integration microprocessor
IC31—74F32 quad 2-input OR gate
IC32—74ACT86 quad 2-input XOR gate
IC33—74F160 4-bit counter
IC34—74ACT153 dual 4-to-1 mulitplexer
IC35–IC37—74LS390 dual bi-quinary counter
IC38—74ACT151 8-to-1 mutiplexer
IC40—Dallas Semiconductor DS1213C "Smart Socket" and 32K × 8 100-ns SRAM or Dallas Semiconductor DS1235 integrated battery backed RAM
IC41, IC42—MAX232 RS-232 tranceiver and charge pump
IC43—7805 5-volt regulator
IC44—GAL16V8-15LP PLD
IC45—GAL16V8-10LP PLD
IC46—128K × 8 250-ns EPROM
LCD panel—Sharp part no. LM24014W

Other components
XTAL1—16-MHz HC-49 crystal
XTAL2—20-MHz 14-pin DIP package oscillator
XTAL3—50-MHz 14-pin DIP package oscillator
Case—Pactec CM69-120
Key switches (12)—75120-002/0000
AC adapter—9 VDC at 1 amp secondary output

Connectors
J1—Right-angle DB37 connector
P2–P4—3-pin socket strip
J3—Right-angle DB9 connector
J4—20-pin socket strip (2 × 10)
P1—7-pin socket strip (1 × 7)
J2—Power connector (2.3-mm barrel)
Keyboard—7 × 1 row-header
Acquisition clip—DB37 connector with 18 wires and micro-clips.
P1—2 × 10 row-header connector for LCD panel

Sockets
20-pin machined sockets for IC1 and IC11
32-pin socket for IC46
14-pin machined socket for IC32
84-pin PLCC socket for IC30

Hardware
4 ⅜-inch standoffs with 4-40 internal thread
4 ⅝-inch standoffs with 4-40 internal thread
18 4-40 screws with pan head, ¼-inch length
2 4-40 nuts
1 TO-3 heatsink and heatsink grease

Five-chip circuit transforms scope into logic analyzer

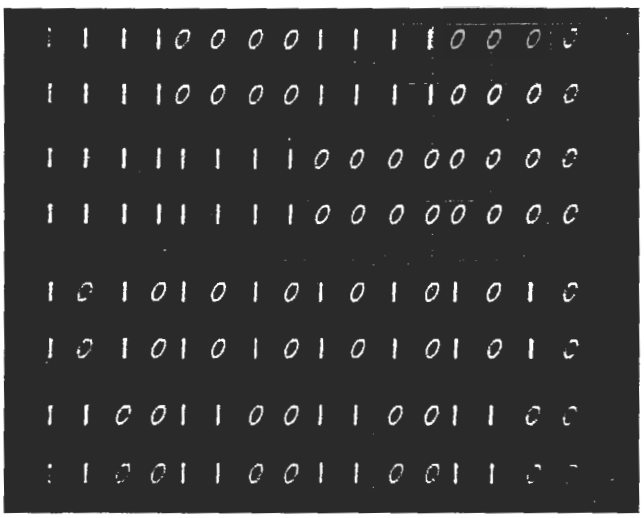
by P. Martinez, A. Roy, and J. Barquillas
Department of Electronics, University of Zarogoza, Spain

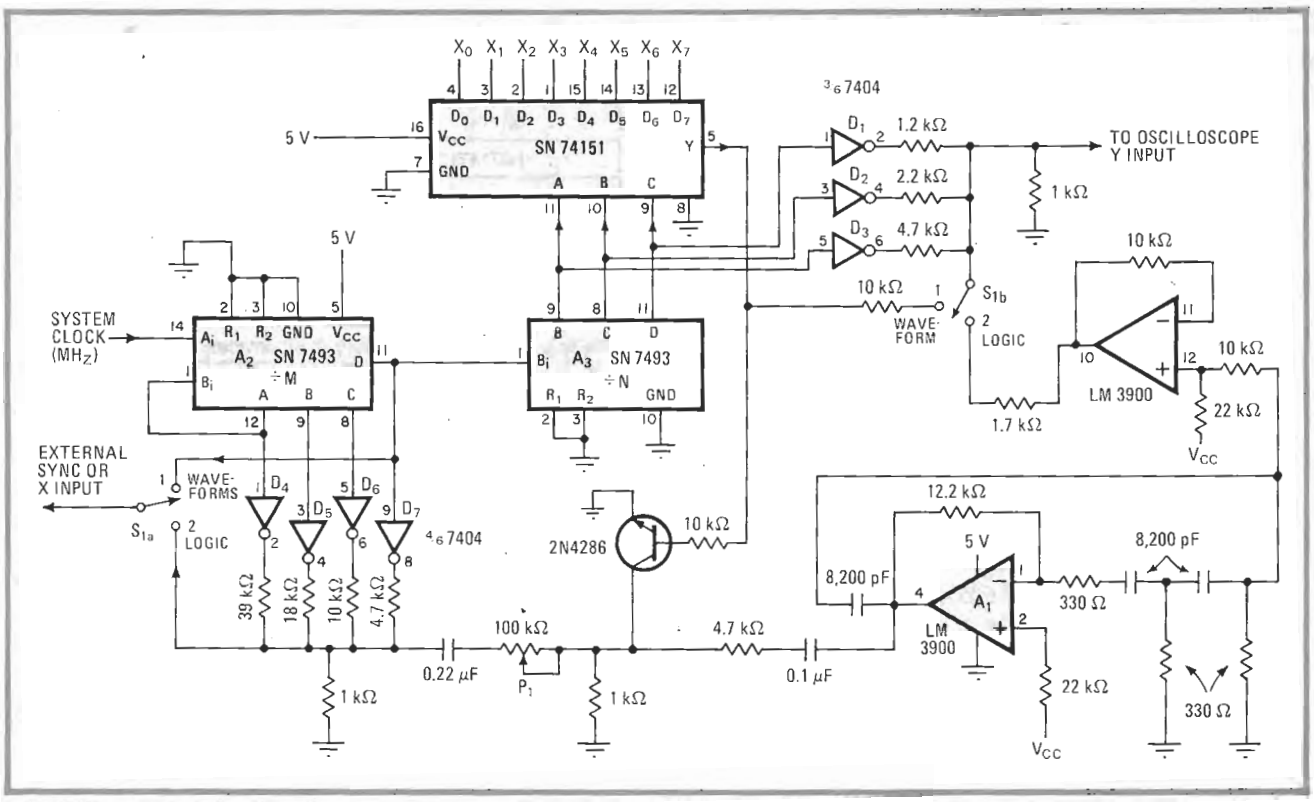
Adapting a general-purpose oscilloscope to use as a logic analyzer, this inexpensive five-chip circuit will permit the numerical display of 1s and 0s for as many as eight digital wavetrains simultaneously. The design is vastly simplified through the use of a rudimentary adder circuit and two primitive digital-to-analog converters, which combine a derivative of the multiplexed signals to be displayed with the numeral-forming circuitry.

In general operation, logic variables X_0–X_7 are introduced into the inputs of the 74151 eight-line multiplexer, as shown. Meanwhile, the LM3900 generator, A_1, produces a sine wave in the vicinity of 150 kilohertz; and the 7493 divide-by-M counter, A_2, which in conjunction with the 7404 inverters and weighted-resistor network forms a d-a converter, is advanced by the system clock. The divide-by-M circuit drives a second counter, A_3, which advances the multiplexer at a rate equal to 1/M that of the stepping frequency of A_2.

If the mode switch, S_1, is placed in position 1, X_0–X_7 are applied directly to the scope's Y input. A_2 drives the sync input with a logic 1. Thus the scope may be utilized to display eight digital waveforms.

The unit is placed in the analyzer mode when the switch is brought to position 2. When the numeral is to be displayed for a given X_i, the sine-wave output of A_1





Adaptation. Inexpensive five-chip circuit adapts scope for duties as logic analyzer. Circuit generates sine wave at Y channel and 90°-displaced sine wave at X channel to produce skewed 0 numerals for any digitally multiplexed X_i input. Unweighted sawtooth is generated at X channel for display of 1s. Mode switch S_1 selects either eight digital waveforms or logic states of the input waveforms as in the photo.

appears at the scope's Y input along with weighted voltage of d-a converter D_1–D_3, which ultimately determines the vertical position of the trace on the screen. At the X input, A_2's weighted output delivered by converter D_4–D_7 adds a component of voltage to A_1's output that effectively displaces its sine-wave signal by 90°. Thus a small numeral 0, slightly skewed, appears on the screen as a result of the Lissajous addition.

If, on the other hand, a 1 is to be displayed, the Y output of the 74151 moves high and brings point A to ground. Consequently, the X input is driven by a waveform, generated only by D_4–D_7, that is an approximate sawtooth. Under these conditions, the trace can rise only vertically, being bound in the horizontal direction at any instant.

In either case, because A_2 steps forward at M times the speed of A_3, the trace will sweep across the entire screen to monitor the variable under observation before the multiplexer is advanced to its X_{i+1} port. Note that the sweep is not continuous, but proceeds from left to right in discrete steps, as a result of A_2's stepped output.

The process is then repeated for the next variable. Because the speed of the system clock is high and the persistence of the scope's phosphor is high, the 1s and 0s appear to be scanned simultaneously. The display format generated is illustrated in the photo. □

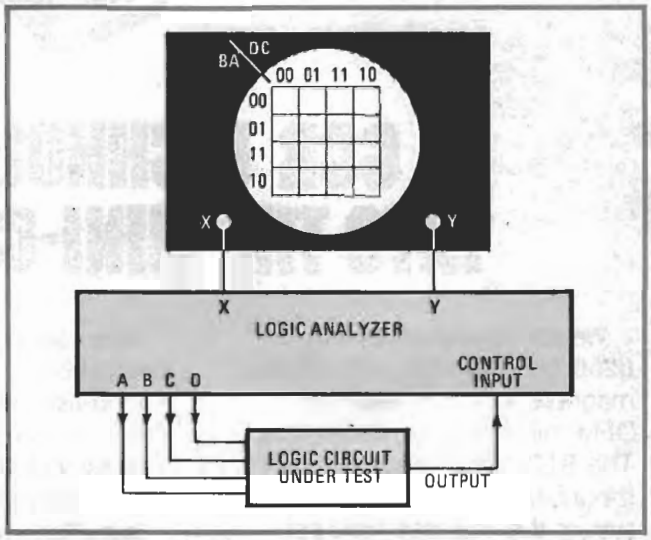
Low-cost logic analyzer displays Karnaugh map

by Prasert Jiraphasra
Chulalongkorn University, Bangkok, Thailand

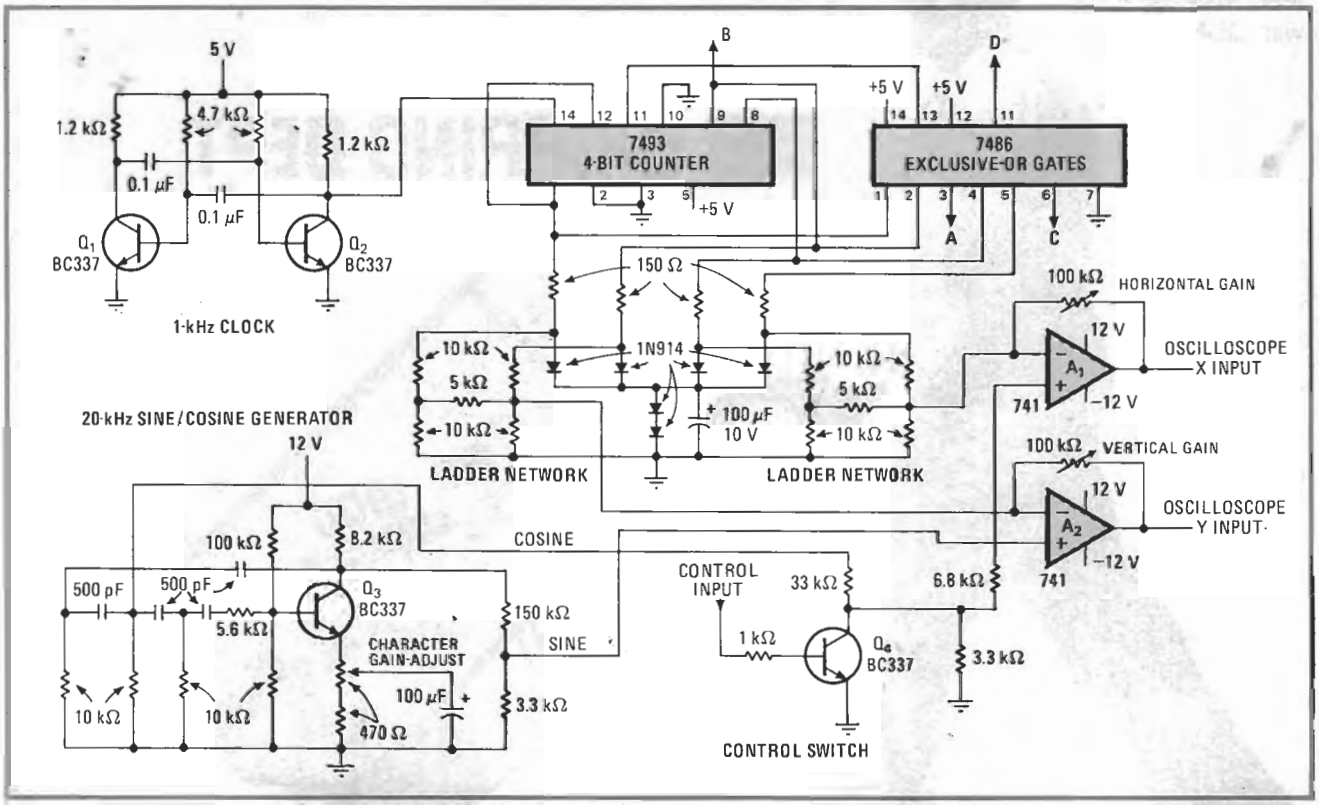
Combine this simple hybrid circuit with an oscilloscope, and the result is a low-cost logic analyzer. It generates the deflecting voltages required for displaying a Karnaugh map of a four-variable logic circuit on the scope's cathode-ray tube. Both linear and digital elements are used to generate either the 0 or 1 numerals at each of 16 positions on the CRT.

As shown in Fig. 1, Q_1 and Q_2 form a 1-kilohertz oscillator, which is used as the external time base for the scope. The clock circuit drives the 7493 4-bit counter and the 7486 exclusive-OR gate array, both of which in turn drive a resistive ladder network. The network produces two four-value staircase waveforms. Four signals from the 7486 and 7493, A through D, cycle through a binary count of 0 – 15 sequentially and drive the logic circuit under test.

The waveforms produced by the ladder network feed into the inverting inputs of A_1 and A_2, in order to provide stepped deflection voltages for the scope's vertical and horizontal amplifiers. These voltages deter-



2. Test layout. Points A to D of analyzer drive logic circuit with 0 – 15 binary sequence. Monitored output point of logic circuit drives analyzer's control input. X and Y outputs of analyzer connect to scope inputs. Scope displays 0 or 1 in each of 16 areas on CRT.



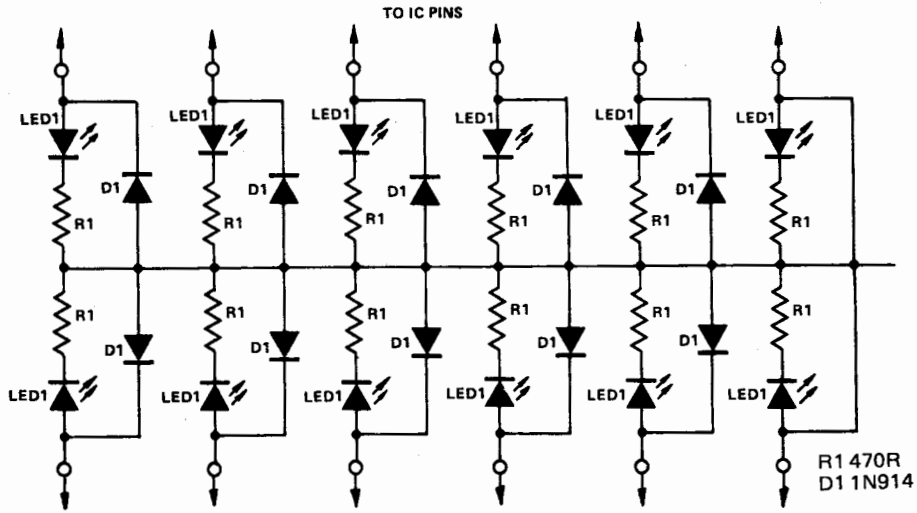
Logic analyzer. Circuit uses four-step staircase and sine/cosine generators to form 1s and 0s at any of 16 locations on scope. Logic 0 from circuit under test causes sine and cosine waveforms at A_1 and A_2 outputs, respectively, resulting in Lissajous pattern of a circle on scope. Logic 1 from device under test clamps A_1 to voltage produced by staircase generator, generating vertical straight line on scope.

mine the initial position of the scope trace at each of the 16 locations. To ensure that rows and columns line up and there is no uneven tilt in the numerals, clamping diodes are used. These diodes hold the output voltage from each pin of the counter constant and equal in amplitude throughout its switching interval. A sine/cosine generator running at 20 kHz is connected to the inverting inputs of A_1 and A_2; the sine wave directly, the cosine wave through control switch Q_4.

As illustrated in Fig. 2, only two interconnecting leads between scope and analyzer are necessary. The desired output of the circuit under test need only be connected to the control input of the analyzer, and the X and Y inputs of the scope to the X and Y inputs of the analyzer.

When the circuit point under test is at logic 0, then for a given set of logic signals A, B, C, and D, the output of A_2 is a sine wave offset by a voltage produced by the ladder network. The output of A_1 is an offset cosine waveform. Because the two signals are equal in frequency but 90° out of phase, the waveform produced on the CRT is a familiar Lissajous pattern at the given location—a circle—which is interpreted as a logic 0.

If the circuit point under test is at logic 1, Q_4 turns on, holding the noninverting input of A_1 low, while A_2 varies sinusoidally at 20 kHz. Thus the waveshape on the CRT is a straight line positioned vertically at the location in question, which may be interpreted as a logic 1. Since the staircase generator steps at a 1-kHz rate as all 16 positions are examined in sequence, it appears to the viewer that all positions are simultaneously filled with a 1 or 0. □



LED 'Logicator'
M. Kyrannis

This circuit can be used as a logic monitoring device to plug into an IC socket. A 'high' level on each of the pins will light its corresponding LED. One good idea might be to build the indicator onto the pins of an IC test clip. The indicator could then be simply clipped over the top of an operating IC. Be careful though that the circuitry can drive the LEDs.

PE TESTED

BREAKTHROUGH PROJECT

Low-Cost Digital Logic Analyzer

Data-domain instrument for troubleshooting any type of digital system including microcomputers.

BY G. MUETHING, I. SPECTOR, AND C. WONG

Digital circuitry has spawned a variety of troubleshooting aids, including logic probes, pulse generators, IC clip-type testers, logic comparators, and multiple-trace oscilloscopes. All are most useful—up to a point. That point is reached when the digital equipment contains a microprocessor, as in computers, scanning monitors, video games, microwave ovens, etc.

In such cases, how does one examine a number of operating interdependent circuit lines for debugging purposes? Industry knows how—with a "logic analyzer," an instrument with a bottom price of about $2500. Now, however, you can build your own logic analyzer for less than $190.

The Logic Analyzer presented here features eight input lines and an ability to examine sequential data before or after a reference event, displaying a truth table consisting of 1's and 0's on any oscilloscope CRT. This is called a data-domain logic analyzer. (There are, of course, other types of analyzers, one of which displays a timing diagram on a scope's CRT.)

Why a Logic Analyzer? Because digital logic operates at two different voltage levels (0's and 1's), the first special-digital test instrument was the simple digital probe. The digital probe uses some type of indicator, usually a LED, to indicate the presence or absence of a signal at any selected single point in a circuit. Since digital circuits usually consist of a number of IC's that all operate from a common timing clock, even if a single digital probe gives a proper indication at a given test point, there is no way of determining if the observed pulse is correctly timed.

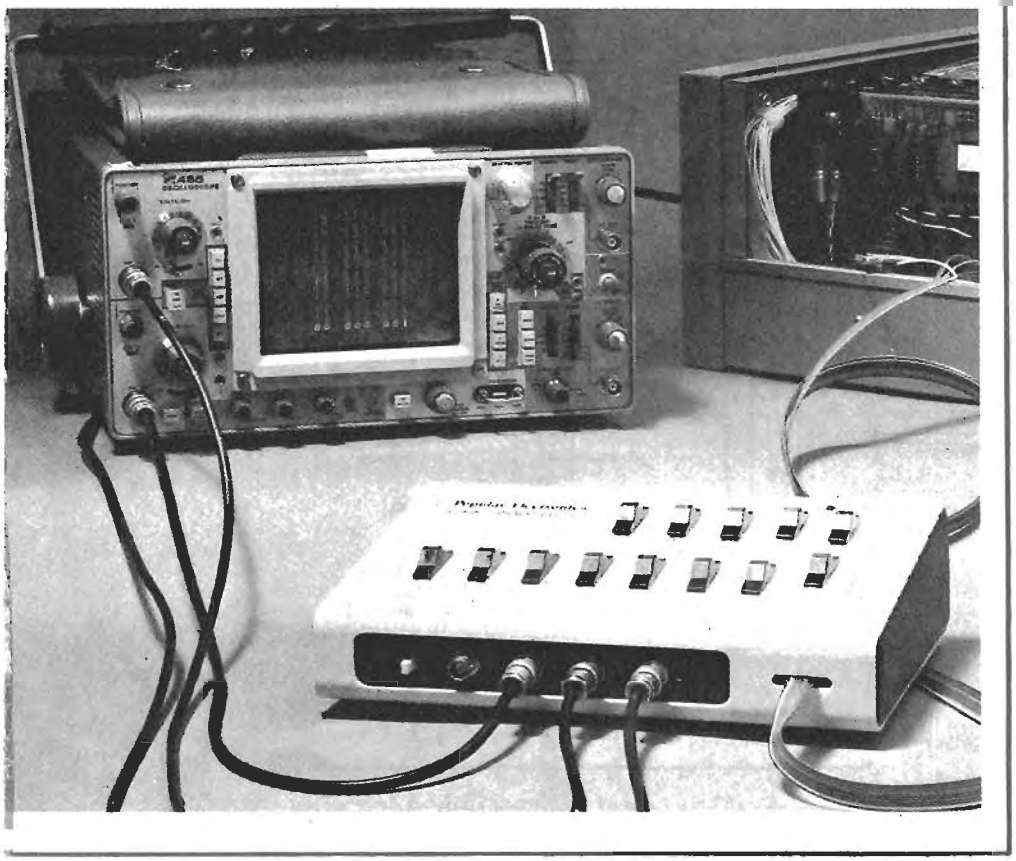
The shortcomings of the digital probe led to the development of the IC "clip" tester in which 14 or 16 LED's could indicate the logic states at each of the IC pins. Note that the status of the logic is of interest only at a specified instant in time related to the clock. This brings up another problem—clock speed. With most clock rates, single 14/16-pin LED indicator probes may display only a blur (except at the ground and power pins of the IC), with the blur rate, or light intensity, a function of the clock speed. Hence, unless you are able to drastically slow down the clock rate, you still will not be able to discover anything but the presence or absence of signals, whether or not they are correctly timed.

Using a logic analyzer with an oscilloscope, you can display a "truth table" of the digital circuit being tested under actual operating conditions. Simply by selecting a "trigger word" consisting of a particular set of 1's and 0's, the analyzer will freeze the 15 8-bit digital words that precede the selected trigger word and display the data so that it can be analyzed at your leisure. A switch also allows the observation of the 15 digital words that follow the trigger word if the problem is thought to lie in that direction. By changing the trigger word, which is brightness accented in the display, as you step through the truth table, it becomes possible to examine the digital logic from start to finish. In essence, then, the Logic Analyzer is a form of electronic "time machine" that can freeze digital events before or after any selected point in time.

Because a computer consists of a number of interlocking digital circuits, each carefully timed from a common clock signal, the misplacement of one bit among thousands can cause a great deal of trouble. Programs that can be properly written will not run because of an erroneous bit being generated within the system.

Why not use a conventional oscilloscope? True, you can see a small group of bits at any given time. But if the system under test is running at the usual clock rates, the picture displayed will keep changing and be blurred. The scope can display a signal only after it has been triggered. If you happen to trigger on the problem itself, you have further complications. Because computers, peripherals, ROM's, and other digital devices may not repeat the same state over and over again, a scope without storage capability cannot display a "snapshot" of a one-time logic event for subsequent analysis. In some cases, the scope is a necessity, as only a scope can display the detailed waveform information that can give the user an insight by an intuitive process where a waveform "just doesn't look right". A good scope can also show up fast transient "glitches" that, although they disturb circuit operation, may not show up on an analyzer. However, if you rely strictly on a scope for analysis, solving many system problems would be virtually impossible.

The low-cost Logic Analyzer in this article will add a form of storage to any oscilloscope, perform the sixteen 8-bit data word freeze as previously described, and provide the electronics experimenter with a state-of-the-art digital test instrument that rivals those costing several hundred dollars more. In use, you simply connect the three analyzer outputs to the horizontal, vertical, and



blanking inputs of a scope and connect the eight data-input and the clock and ground probes to the circuit being analyzed. When the trigger word keyed in via control-panel switches appears, the Analyzer will automatically trigger, collect, store, and display 16 sequential 8-bit words in either octal or hex format, as shown in Fig. 1. The analyzer will accept data rates as high as 8-million bytes/second.

Another front-panel control allows the user to select either "positive time" in which the selected trigger word appears intensified on the top of the CRT screen with the next 15 sequential data words below it, or "negative time" in which the 15 data words leading up to the trigger word appear first with the brightened trigger word at the bottom of the screen.

One other control provides the choice of a "snapshot" that catches and displays an individual 16-word table for as long as you like or a "moving picture" display in which the data for each table is collected and automatically displayed so you can dynamically observe the operation of the circuit. The specifications for the logic analyzer are shown in the box.

Circuit Operation. Operation of the analyzer can best be understood by referring to the block diagram of Fig. 2. (The complete schematic diagram is shown in sections in Figs. 3 through 7.) The inputs to the system are the 8-bit signals (BIT 0 through BIT 7), the system clock, and the common or ground bus of the digital circuit under test. The data and clock inputs are buffered by *IC1* and *IC2*. The eight data signals are latched by *IC4* and *IC5* before loading into data memory *IC6* and *IC7*. This 16-word data memory is the "heart" of the analyzer. It stores sequential data words from the digital system under test.

The buffered clock signal is fed to half of *IC2* that can be set to operate on either the negative or positive edge, depending on the setting of *S10*. This signal is applied to the display control logic made up of *IC11* through *IC15*. The other input to the display logic is from comparator *IC3*. This circuit uses *S1* through *S8* to set up the desired trigger word, with the switches set to either 1, 0, or X as required. (The X is a "don't care" state.) When the comparator receives the input data word that matches its switches, a signal is passed to the display control logic. When *S11* is set to the POS TIME position, for example, data collection begins when the comparator detects the trigger word. After 16 clock pulses, data collection stops so that the memory contains the trigger word followed by the next 15 data words. In the NEG TIME position of *S11*, the memory stores data continuously until the trigger word occurs. When this happens, data collection is halted, leaving the memory with the 15 data words leading up to the trigger, plus the trigger word itself.

During the data collection period, the display control logic sends a signal to the blanking logic system made up of *IC22* through *IC24*, *Q1*, and *Q2* to inhibit the display. At the end of this period, the blanking signal is removed and a bit-by-bit scan of the memory contents is initiated. Scanning is accomplished by data multiplexer *IC16*, which is controlled by three of the eight output bits of horizontal control ROM *IC19*. Thus, even though the data memory provides a full 8-bit wide data word to the input of the multiplexer, only one bit at a time is sent to the 1-0 character generator made up of half of *IC20*, and *Q3*.

The character generator uses this information and the CRT beam positioning signals from the *IC20* horizontal D/A (di-

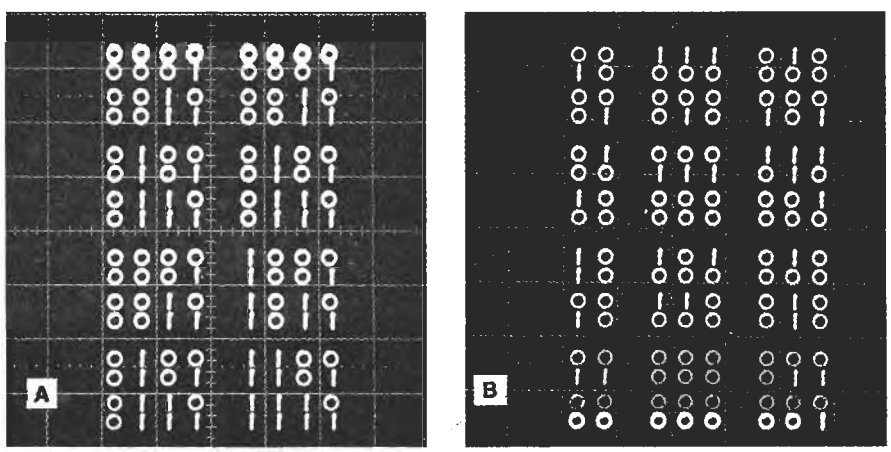


Fig. 1. Trigger word is intensified at top of hex display (A) with the 15 following data words. In octal display (B), trigger word is at bottom with the 15 data words leading up to it.

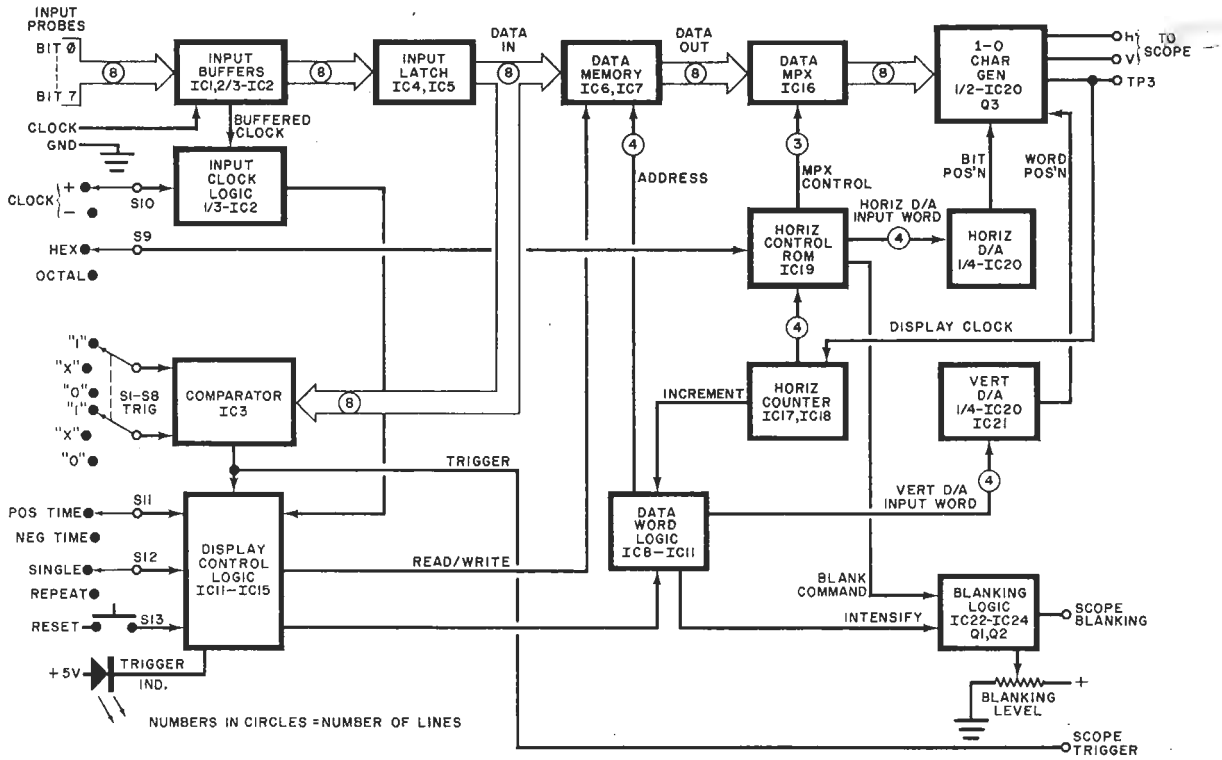


Fig. 2. Block diagram of analyzer shows basic signal routing.

PARTS LIST

C1—2200-μF, 16-volt electrolytic capacitor
C2—220-μF, 50-volt electrolytic capacitor
C3—10-μF, 50-volt electrolytic capacitor
C4,C5—150-pF, 10% disc capacitor
C6—15-pF, 10% disc capacitor
C7,C8,C9,C10—0.1-μF, 20% disc capacitor
C11—300-pF, 10% disc capacitor
C12—180-pF, 10% disc capacitor
C13—0.01-μF, 20% disc capacitor
D1,D2,D3—1N4002 or similar rectifier diode
IC1,IC2—74LS14 Schmitt-trigger input hex inverter (Fairchild 15-V input only),
IC3—74S15 open-collector output triple three-input AND gate
IC4,IC5,IC9—74LS175 quad latch
IC6,IC7—7489 RAM (16×4)
IC8—74LS161 four-bit synchronous counter
IC10—74LS83 four-bit adder
IC11,IC12,IC22—7400 quad two-input NAND gate
IC13,IC14,IC18—74LS73 dual JK flip-flop (do not substitute)
IC15—7473 dual JK flip-flop (do not substitute)
IC16—74LS151 8-to-1 multiplexer
IC17—74LS90 decade counter
IC19—8223 256-bit open-collector output PROM, or similar
IC20—LM3900 quad current amplifier
IC21—7407 open-collector output hex buffer
IC23—74LS21 dual four-input AND gate
IC24—7406 open-collector output hex inverter
IC25—LM309K 5-volt regulator
J1 through J4—UG-625 BNC connector
LED1—Light-emitting diode (any color)
Q1,Q3—2N3904 silicon transistor
Q2—2N3905 silicon transistor
The following resistors ¼ watt, 5%:
R1 through R27—4700 ohms
R28—3300 ohms
R29—470 ohms
R30—1000 ohms
R31,R32,R33—8200 ohms
R34,R35,R36—2700 ohms
R37—1800 ohms
R38—2000 ohms
R39,R40—33,000 ohms
R41,R42—56,000 ohms
R43,R44,R45—22,000 ohms
R46,R47—24,000 ohms
R48,R49—130,000 ohms
R51,R52—180 ohms
R53—47,000 ohms
R54,R55—11,000 ohms
The following resistors ¼-watt, 2% tolerance:
R56—4700 ohms
R57—2400 ohms
R58—5100 ohms
R59—2700 ohms
R50—5000-ohm trimmer potentiometer (Spectrol 43P502 or similar)
S1 through S8—double-pole 3-position pc-mounted switch
S9 through S12—dpdt pc-mounted switch
S13—momentary-action dpst pc-mounted switch
S14—spst switch (panel mount)
T1—dual-winding power transformer with 16-volt CT and 22-volt winding
Misc.—Line cord, strain relief, mounting hardware, 3 feet of Spectra-Strip multicolored flat ribbon cable (26 gauge), 16-pin DIP socket, 16-pin flat ribbon DIP plug, heat sink for voltage regulator, hookup wire, solder, suitable case and mounting brackets, probe tip connectors, etc.

Note: The following items are available from Paratronics, Inc., Dept. 100, Los Gatos, CA 95030: Complete kit of parts, No. LA-100KIT, with tested IC's, power supply, pc board, case, and manual for $189.00. For separate parts: drilled double-sided printed circuit board, No. LA-100 PC, $29.95; programmed horizontal control ROM, No. LA-100ROM, $15.95; power supply, No. LA-100PS, $39.95; complete set of switches, connectors, hardware and data probes, No. LA-100HW, $39.95; Case, No. LA-100CASE, $39.95. Comprehensive applications and assembly manual, LA-100MAN $4.95. Please add 5% to above items for shipping and handling within U.S., 10% outside the U.S. California residents, add 6% sales tax.

Free copies of etching and drilling guides for the pc board, components-placement diagram, and horizontal control PROM programming information are available on request by sending a self-addressed stamped 9" × 12" envelope with 26¢ postage to: POPULAR ELECTRONICS, Dept. LA, One Park Ave., New York, NY 10016.

gital/analog) and the *IC20-IC21* vertical D/A circuits to write a 1 or 0 at the proper location on the CRT screen.

The horizontal D/A circuit receives its 4-bit data word from the horizontal control ROM, which receives its address data from the horizontal counter made up of *IC17* and *IC18*. It is the incrementing of the horizontal counter that causes the beam to move from right to left across the face of the CRT as the data word is written.

When the last bit is displayed, horizontal counter *IC17-IC18* "rolls over" to 0 and sends the increment signal to the

data word logic *IC8* through *IC11*. This causes the address of the data memory to advance to the next word location and simultaneously sends a command to the vertical D/A converter that causes the CRT beam to move down one row in preparation for display of the next word. This process continues until all sixteen of the words of interest have been written on the CRT screen.

If *S12* is set to the SINGLE mode, the display control logic prevents the data memory from collecting new input data so that the same information is written on the CRT screen. The writing speed is fast enough so that a flicker-free "snapshot" of the memory contents is displayed. This snapshot will remain on the screen until the RESET switch *S13* is operated, at which time the TRIGGER LED comes on and the analyzer is armed to "capture" another 16-word data set. When *S12* is in the REPEAT mode, the display control logic provides an automatic reset signal after the display of each 16-word truth table.

Blanking between bits is provided by the remaining bit of the horizontal control ROM. This ROM performs three separate functions: control of the data multiplexer, control of the horizontal D/A converter, and blanking control. This use of a ROM as a controller is called "microprogramming," an efficient design technique used in a number of high-level computers. An "intensify" command from the data-word logic permits the trigger word to appear brighter than the other data words on the CRT screen.

The trigger pulse generated by comparator *IC3* occurs each time the trigger word appears. The resultant output pulse can be connected to the sync input of an oscilloscope anytime it is necessary to "look" at a specific signal in the circuit under test. This important feature is useful for troubleshooting equipment for glitches, timing, or intermittent problems that occur only during particular logic states.

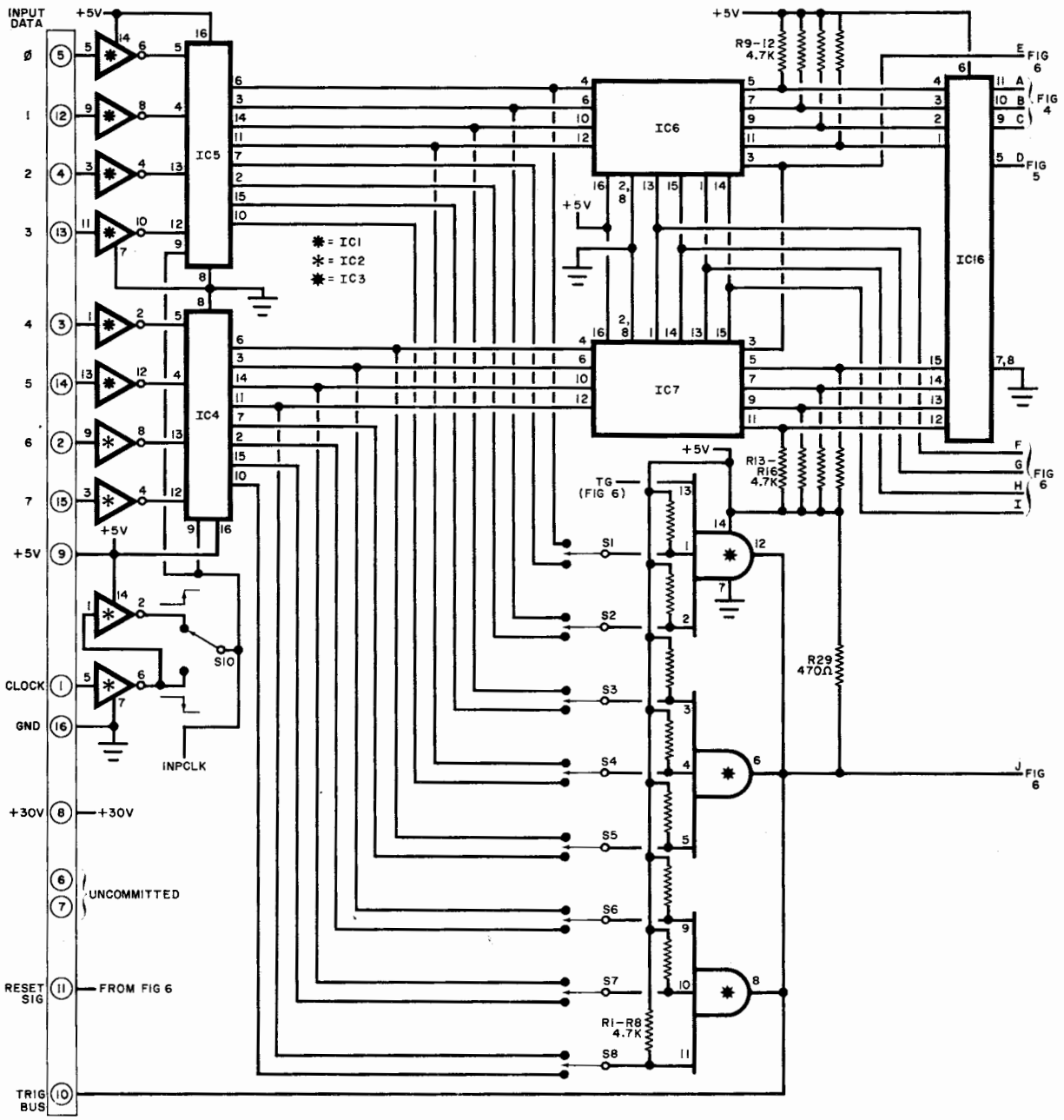


Fig. 3. Input buffers, trigger detector, memory, and data multiplexer.

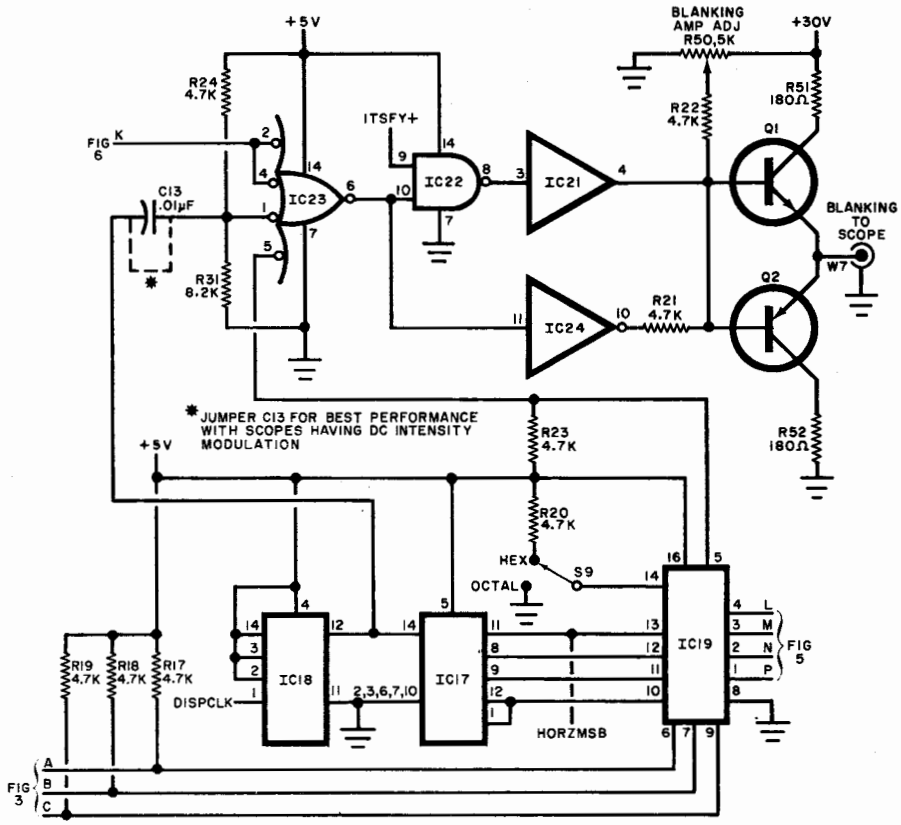


Fig. 4. Vertical control and blanking.

trude through its hole on the top of the case, mount *LED1*. Install the 16-pin DIP socket for the flat ribbon probe cable. This completes the assembly of the board.

Mount the BNC scope connectors and on-off switch *S14* on the front of the case. Then drill a hole so that the blanking amplitude potentiometer mounted on the pc board can be adjusted from outside the case. The top of the case should be punched to accept the 13 switches and the LED indicator. Make sure that all switches can be moved into all their positions. Then put a slot in the front apron to accommodate the flat ribbon cable.

Mount the transformer wherever convenient at the rear of the case. Bring the three-wire ac line cord into the case through a strain-relief.

The input probe cable is made up of a 3' (about 1-m) length of 10-conductor, flat-ribbon cable. The last conductor in the cable is coded black for ground. Connect the ribbon cable to the 16-pin DIP plug with the black cable (ground) mating with pin 16. The other conduc-

Construction. Because of the complexity of the circuit, and the critical placement of certain components, such as the 1-0 character generator, a high-quality, two-sided pc board with plated-through holes is highly recommended for this project. (See Note in Parts List for source from which etching and drilling guide, component layout diagram, and programming information for the horizontal control ROM can be obtained).

Both sides of the pc board contain components. Start assembly by installing the optional sockets for all the IC's on the side of the board labelled IC SIDE. Then mount all resistors, capacitors, and diodes, making sure that polarity-sensitive devices are correctly oriented.

Mount voltage regulator *IC25* in place, using silicone grease, or a thermally conductive gasket between its case and the board. A suitable heat sink should be used if the board is to be mounted inside a case. The case provided with the kit comes with a heat sink. Install the IC's, transistors, and blanking control *R50*. The IC side of the board should look like the assembled board shown in Fig. 8 when you are finished.

Turn the board over to the SWITCH SIDE and mount the 13 control switches. Then, making sure that its base is high enough off the board so that it can pro-

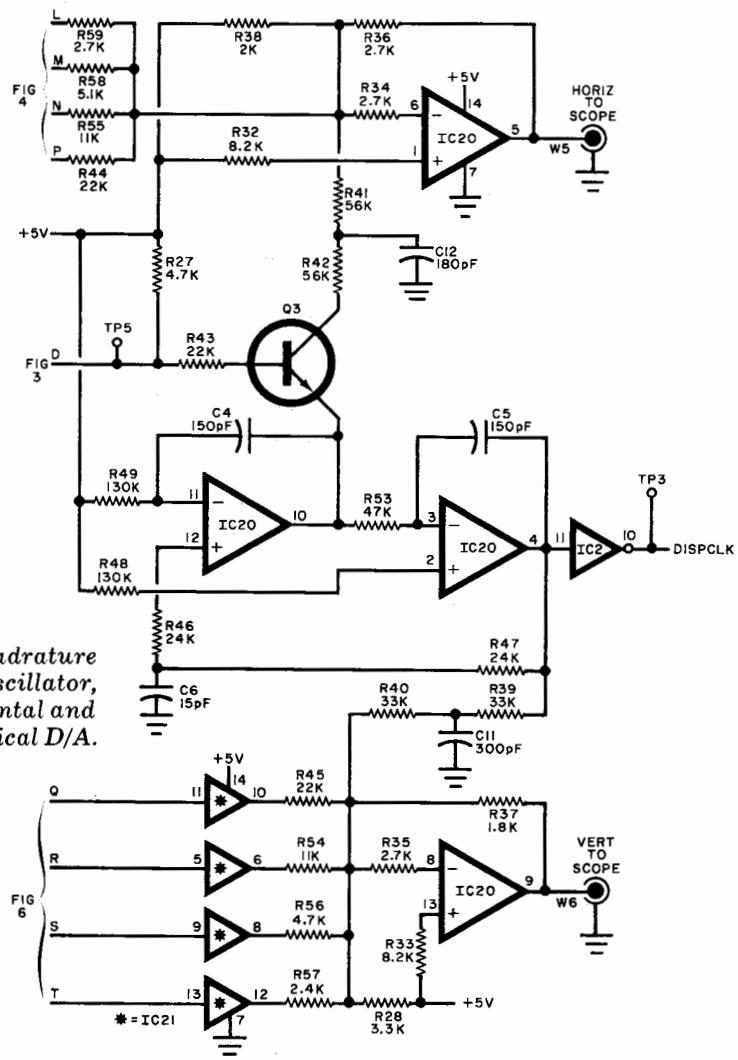


Fig. 5. Quadrature oscillator, horizontal and vertical D/A.

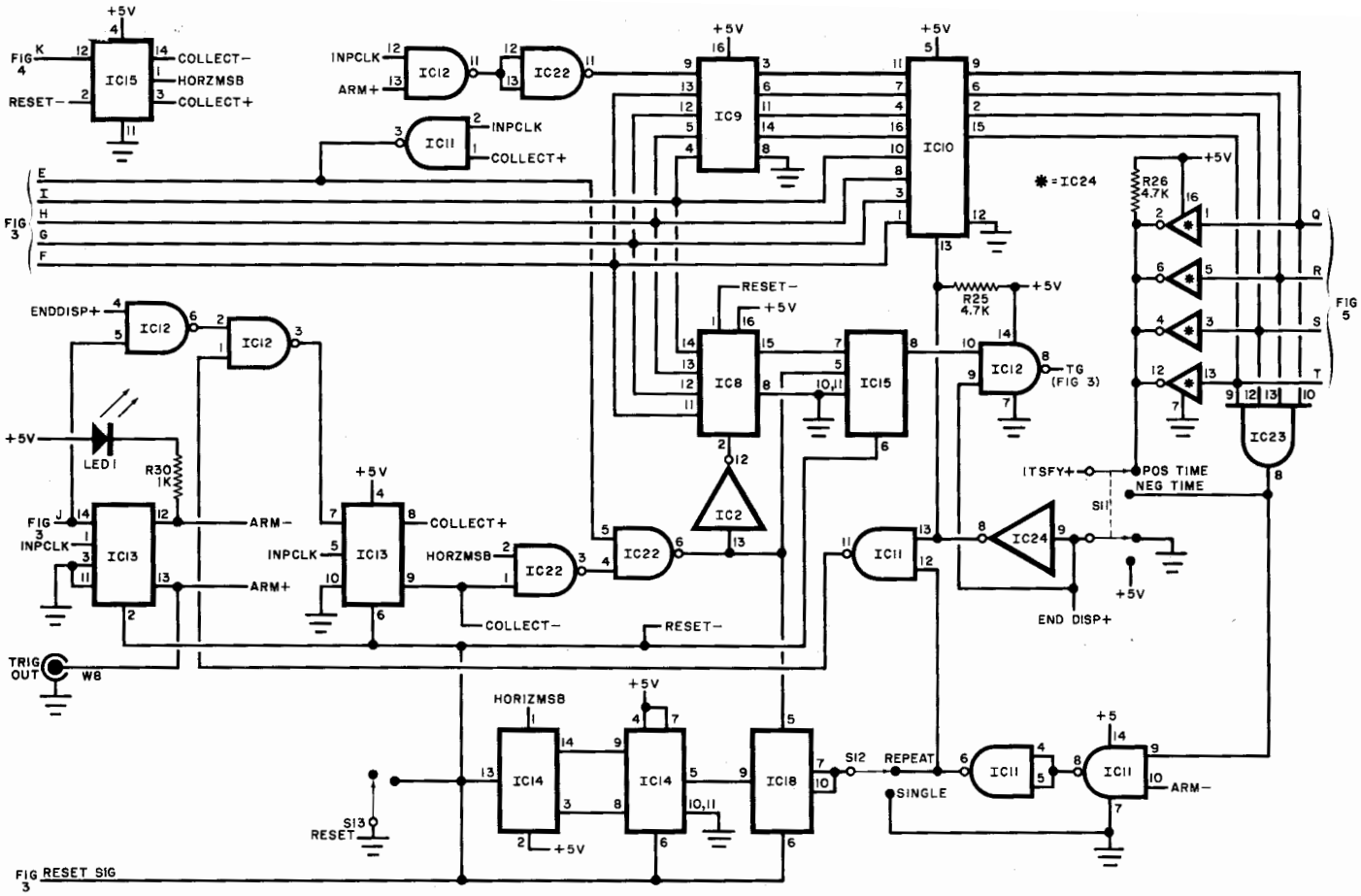


Fig. 6. Horizontal logic and mode control logic.

tors can go to the plug pins in a color-coding scheme.

At the free end of the ribbon cable, separate the 10 leads at least 4" (10.2 cm) and attach universal pin connectors. This type of connector will mate with conventional IC clips and wrapped-wire pins. If desired, ball clips or EZ hooks can be substituted. Plug the probe assembly connector into its socket on the pc board and pass the cable out of the case through its slot on the front apron and assemble the case.

Checkout. Plug the line cord into an ac outlet and turn on the power. Verify the output of the 5-volt power supply at *TP1* using a voltmeter. With an oscilloscope, check for the presence of an approximately 20-kHz clock at *TP3*.

Activate the blanking output at *W7* by placing the eight trigger switches to the "X" (center) position, selecting the SINGLE mode, depressing the RESET pushbutton to activate the front-panel LED, and flipping the clock polarity switch (*S10*) one or more times. This last step generates switch contact bounce that simulates an incoming clock pulse train. When the LED goes off, the blanking signal will appear at board pad *W7*.

Using the oscilloscope, measure the peak amplitude of the blanking pulse. This pulse can be adjusted up to approximately 30 volts by adjusting *R50*. ***Do not*** exceed the manufacturer-specified blanking requirements for your scope.

Set the scope vertical attenuator to approximately 0.5-volt/cm and check the D/A signals at *W5* (horiz) and *W6* (vert). The waveforms should appear as "descending staircase" waveforms, with the *W5* signal much higher in frequency.

Using the scope in the XY mode, connect the horizontal, vertical, and blanking outputs of the analyzer to the appropriate scope connectors. To assure a clean display, it is suggested that you use coaxial cables for the interconnections between the analyzer and scope.

Place the scope horizontal and vertical amplifiers to approximately 0.5-volt/cm. With the analyzer *input* probes unconnected, and the trigger switches still set to the "X" (center) position, depress the RESET pushbutton to illuminate the LED. When the clock polarity switch (*S10*) is flipped, a truth table should appear on the CRT. Adjust the scope controls until the display is centered on screen and fills most of it.

Adjust the focus and intensity controls to obtain a clear well-defined display.

One interesting feature of the Logic Analyzer is that it can be used to observe and learn its internal operation.

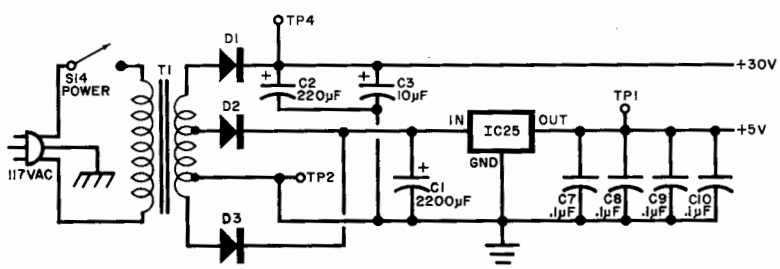


Fig. 7. Power supply is 5 volts, regulated.

For example, to see how the 4-bit address of the data memory sequentially changes during data collection, connect the first four data probes (BIT 0 through BIT 3) to pins 14, 13, 12, and 11 respectively, of *IC8*. The remaining four probes should remain unconnected. Connect the input clock probe to *IC2* pin 10 (or *TP3*) and set the analyzer controls to HEX, REPEAT, NEG TIME, and the clock-polarity switch to the falling edge position. Set the first four trigger switches (*S1* through *S4*) to 1111 and the last four to X. The selected trigger word should appear intensified at the bottom of the table, with the 15 prior binary address words listed in sequence above it.

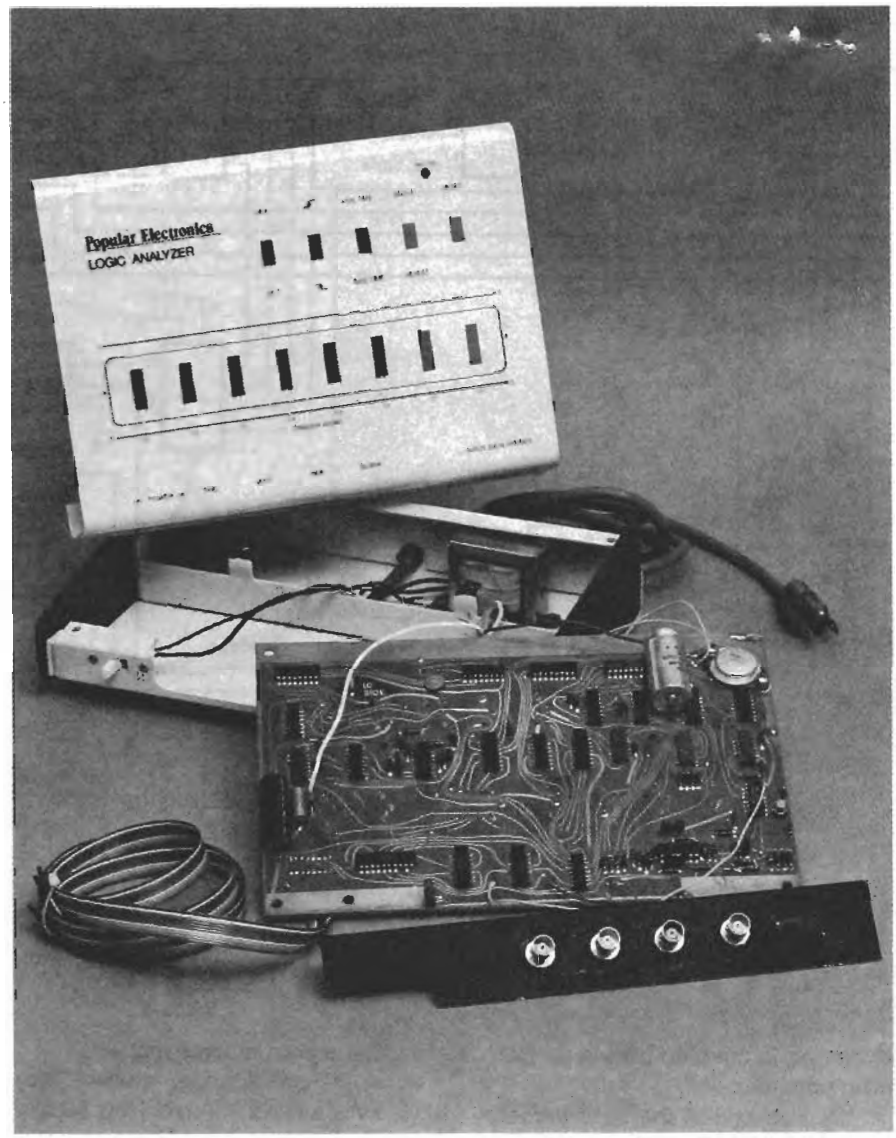


Fig. 8. Completed board and connector panel ready for assembly.

LOGIC ANALYZER SPECIFICATIONS

Trigger Word: 0 to 8 bits wide; selected by eight 3-position switches; choose 0, 1, or X (don't care).
Display Format: Sixteen sequential 8-bit words arranged in an octal or hexadecimal truth table.
Positive Time Display: Trigger word intensified at top of truth table with next 15 data words listed *below*.
Negative Time Display: Trigger word intensified at bottom of truth table with prior 15 data words listed *above*.
Single Mode: Continuous display of one 16-word truth-table until RESET button is activated.
Repeat Mode: Display of sequential 16-word truth tables.
Maximum Input Data Rate: 8 million bytes/second.
Input Clock: Provides timing reference for input data; selectable positive or negative clock edge.
Trigger Indicator: LED on front panel indicates when trigger word has occurred.
Trigger Output: Auxiliary scope sync pulse; generated when trigger word occurs.
Input Probes: Constructed of color-coded flat-ribbon cable terminated in universal pin connectors.
Input Load: Inputs are buffered for minimal loading and have hysteresis for noise rejection.
Power Supply: +5 volts at 700 mA, +30 volts at 25 mA.
Logic Family Compatibility: TTL, DTL, RTL, MOS, CMOS, to 15-volt logic swing.

Continue to familiarize yourself with the operation of the analyzer by triggering from different address locations and changing the settings of the display control switches. The probes can be moved to other portions of the circuit, such as the horizontal counter, display-control logic, and the data-word logic.

You can couple the first four probes to the counter (7490 or similar) in any digital counter circuit to examine the operation of that circuit. In fact, the right side of the hex portion of the display in Fig. 1 shows the output of a "good" 4-bit counter while the left side shows the output of a counter whose MSB (most significant bit) is stuck at 0. Using this technique, you can follow the signals through almost any digital circuit and be able to "snapshot" any block of pulses so that they can be examined for faulty pulses.

The analyzer shows its flexibility when used to check a computer or program. The octal portion of Fig. 1 shows the steps of a typical 8080 ADD and STORE program leading up to a branch instruction. The trigger word 00 000 001 is the branch address and is intensified at the bottom of the display.

In Closing. The Logic Analyzer we have described can be used for all types of testing and troubleshooting of digital circuits and systems. However, its true flexibility is revealed when the instrument is used for testing and troubleshooting digital-computer and other time-dependent circuits and systems. What makes our Logic Analyzer particularly attractive is its relatively low price. Used as an accessory to an existing oscilloscope and built from scratch, it costs only a fraction of commercially made logic analyzers on the market. ◇

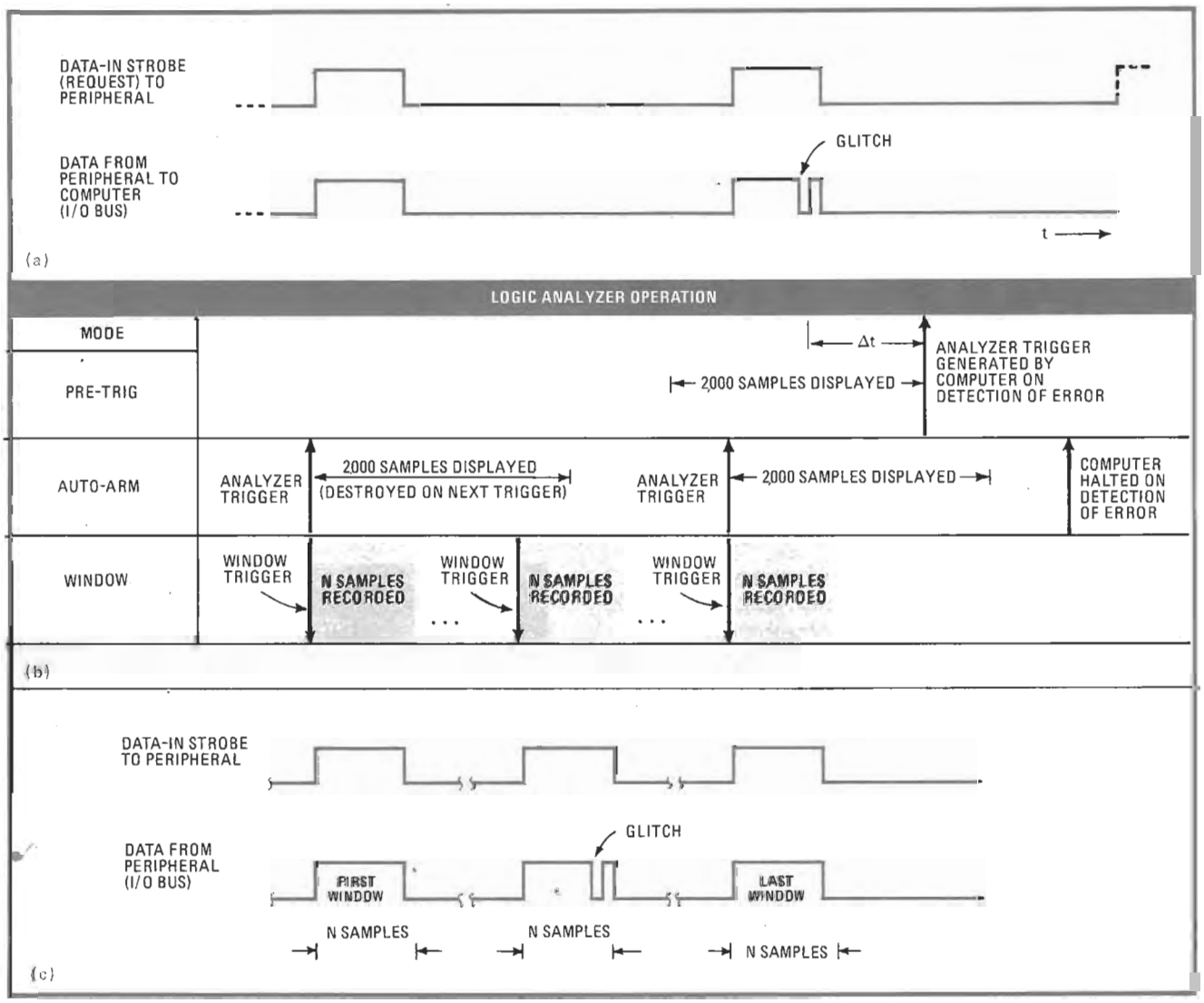
Window generator increases logic analyzer's capability

by Colin Gyles
Canadian Marconi Co., Montreal, Canada

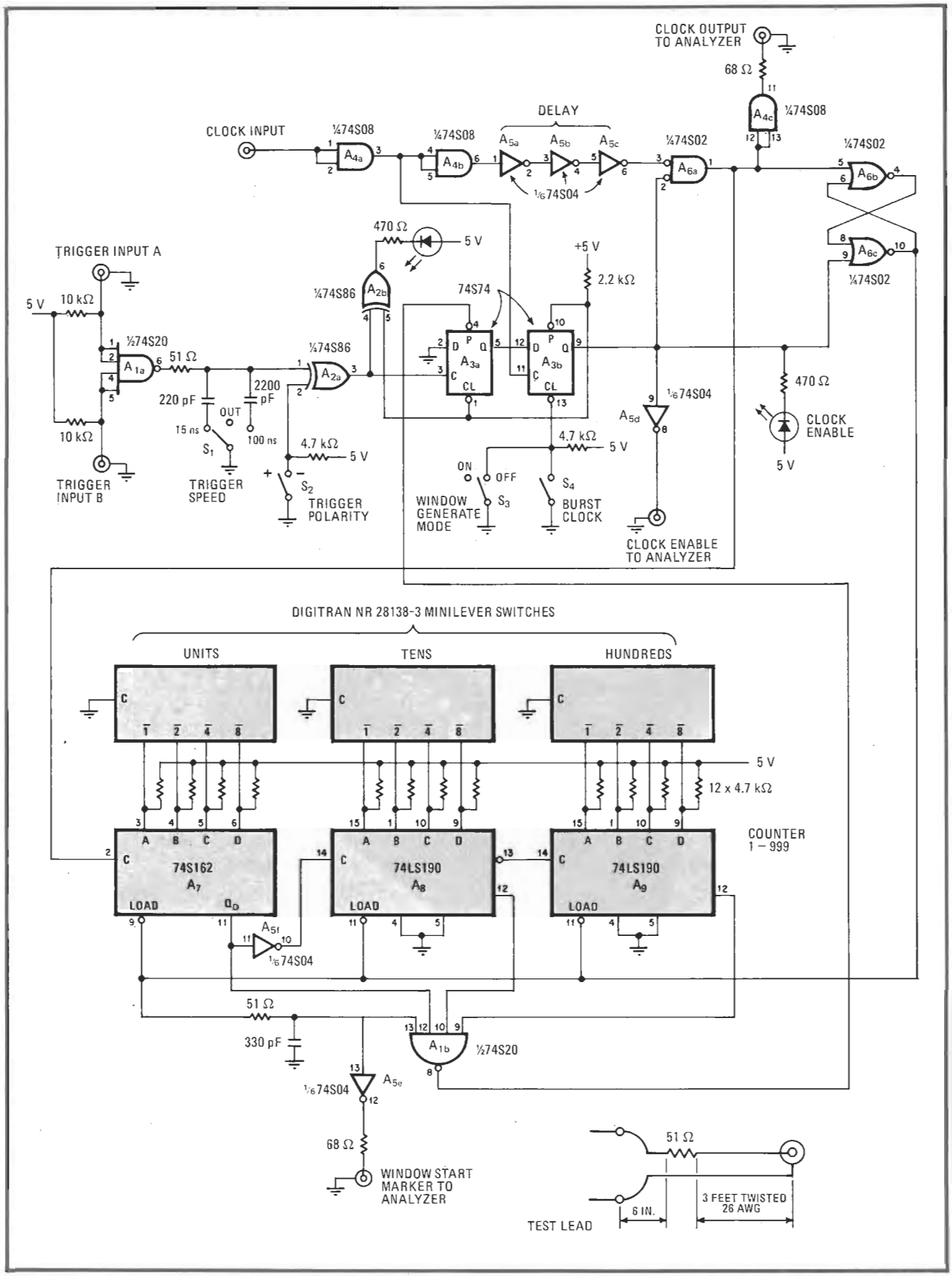
Although the diagnostic power of the logic analyzer is unparalleled for troubleshooting digital systems, its ability to detect the type of errors that lead to intermittent circuit failures leaves something to be desired. For example, the analyzer would have difficulty in detecting a random error in a computer system that passed data in short bursts separated by longer periods containing no relevant information. In such instances, this circuit vastly increases the recording range of analyzers of the time-domain variety, such as the Biomation 8100D.

It is necessary to understand the operation of a stand-alone analyzer to appreciate the difficulties involved in the display of certain data errors. In the example shown in the timing diagram of Fig. 1a, a strobe or similar data-request signal is sent from a computer or other control unit to a peripheral device. The peripheral then sends the data requested to the computer through the latter's I/O port. Note that the data has a glitch, perhaps caused by noise, so that when checked by the computer it is found to contain an error.

There are two methods of recording the error with an analyzer. The first method makes use of the analyzer's pre-trigger mode. Input data is recorded continuously,



1. Analyzer overview. In typical example, stand-alone logic analyzer records glitch in the last word received on computer I/O bus only, because of limited record range (a, b). Record range is vastly extended with window generator, which produces bursts of clock pulses during data-strobe time, permitting many data words to be recorded. Errors occurring in other than the last word received can thus be detected (c).



2. Window generator. Data-in strobe from control unit (computer) drives trigger inputs, initializing record period as circuit generates N clock periods, 1 microsecond wide, to analyzer through clock-output port. The value of N may be selected from 1 through 999.

and the analyzer is made to display the events causing the glitch. In the case of the 8100D, it displays the sequence of states that occurred in the interval, 2,000 sample units long, immediately preceding the trigger generated by the computer when the error was detected. Each sample unit corresponds to the period of the sampling rate of the analyzer's internal data clock. Thus, if the clock period is 20 ns, the events occurring up to 40 μs before the trigger can be displayed.

Needless to say, the larger the required recording range, the poorer the resolution and the harder it is to determine where an error occurs. And if the computer is so occupied with other duties that it cannot generate a trigger quickly enough after the error has occurred, the error will be missed altogether. Thus the time Δt, shown in Fig. 1b, must be minimized.

The second error-detection method uses the analyzer's auto-arm mode, which when triggered by an error records the following 2,000 samples. The circuitry is then rearmed. If a second trigger should occur, the analyzer destroys the previously recorded data and overwrites it with 2,000 new samples. The results of its operation are illustrated in Fig. 1b, with the trigger generated by the leading edge of the data-in strobe. With this method, the required range over which the analyzer records is small, so that the resolution will be high.

The error-detection problem cannot be solved satisfactorily by either method when the error is not contained within the last word received in a data stream (Fig. 1c). This condition might occur if the computer were making check-sum error determinations on a block of data from a paper-tape reader, where the results of the check would be revealed after the data word was read. In most instances, it would be impossible to display the error, since the time between strobes for a reader might be 100 milliseconds or so, but the strobe width might be only 1 microsecond.

Thus, to record a block of, say, 10 words, the record range would be 10(100 ms) = 1 second, but the resolution would be only 1/2,000 = 0.5 millisecond, and it is safe to conclude that an error lasting 1 μs would not be detected. Ideally it would be desirable to record the period in the vicinity of each strobe, where the error would occur, while holding the analyzer's internal clock off during the remaining time.

Therefore to detect the error, it is necessary to generate windows greater than 1 μs wide by a counter delivering N pulses to the external clock input of the analyzer after each window trigger, where N could be selected by the user. Then, on receipt of a trigger from the computer, due to detection of an error, the analyzer will stop recording (assuming pre-trigger mode) and display 2,000/N windows. The recording range would be equal to 4 seconds if N = 50 (that is, R = 100 ms [2,000]/50) for a resolution of 20 ns (equal to the analyzer's clock rate). This is an improvement of 100,000 times over the 40-μs recording range previously shown to exist for the same resolution.

The window-generator circuit for attaining the desired range magnification is shown in Fig. 2. The clock input is driven by a square-wave generator to provide the desired sampling interval. The logic analyzer is clocked by the signal emanating from the clock-output port. When a transition of the required polarity occurs at either of the trigger-input ports, the unit counts N clock pulses to the logic analyzer, N being set by the digital switch, which has a range of 1 to 999. During the time of the N-clock pulse burst, the trigger-input port is disabled.

The end result of the unit's operation is that N samples are clocked into the analyzer after each window-generator trigger. If the analyzer is set in the pre-trigger mode, then on receipt of an analyzer trigger from the computer, the recording will stop, displaying the last 2,000 samples, made up of 2,000/N windows side by side.

The window-start marker output may be fed to any one of the eight analyzer channels. This pulse is one clock period wide at the start of each window so that each frame may be identified at will. The clock-enable output can be recorded on a second logic analyzer to measure the time between window frames, if desired.

Note that the analyzer can be used in all trigger modes while using the window generator. In any of the post-trigger modes, the recording is complete when all 2,000 samples have been taken. If there are not a sufficient number of window triggers, the analyzer will hang up. The burst-clock switch is therefore included to enable the recording cycle to be completed manually whenever there are too few triggers to record the 2,000 samples.

The circuit relies mostly on sequential logic, as shown. S_1 and S_2 select the trigger speed and polarity, respectively. A positive transition at A_{3a}'s clock input brings its Q output low. At the next positive transition of the clock input, A_{3b} moves low. A_{4b} and A_{5a}–A_{5c} provide delay, in order that A_{6a} be enabled when the clock input is low. This is to prevent generation of a narrow clock-output pulse, which could upset the analyzer operation. The clock-output port now follows the clock-input signal. The circuit is designed to minimize the delay from the trigger-input pulse to the time the first clock-output pulse appears.

Just prior to the first clock at A_{6a}, the flip-flop A_{6b}–A_{6c} was set, which enables counters A_8 and A_9 to be loaded with the digital switches. A_7 is loaded during the first positive clock-input transition. This data is the 9's complement of what is displayed. A_{6c} is then set high, and the counters are free to advance from their set values up to 999, at which time the counters enable A_{1b} and preset A_{3a} to logic 1.

During the next clock input, A_{3b} moves high. The delay provided by A_{4b} and A_{5a}–A_{5c} disables A_{6a} before the clock-input transition arrives at its input, thus ensuring that no narrow glitches can be produced at clock output, as mentioned previously. The logic present at the output of A_{3b} then sets A_{6b}–A_{6c}, removing the preset signal from A_{3a} so that the trigger can be enabled for the next window.

Lead lengths should be minimized when building the circuit. The test lead for the trigger-input port should be built carefully also. It should not exceed 4 feet in length. A 51-ohm resistor on the hot side of the test lead will minimize ringing and reflections of energy from probed

circuits. Twisted-pair wires should be used to avoid undesirable coupling effects.

The circuit can work up to 60 MHz, with a one-count error between 33 and 60 MHz, which simply increases the window size by one. The size of the window does not substantially affect circuit accuracy. □

Three-chip logic analyzer maps four-input truth table

by C. F. Haridge
University of Ottawa, Ontario, Canada

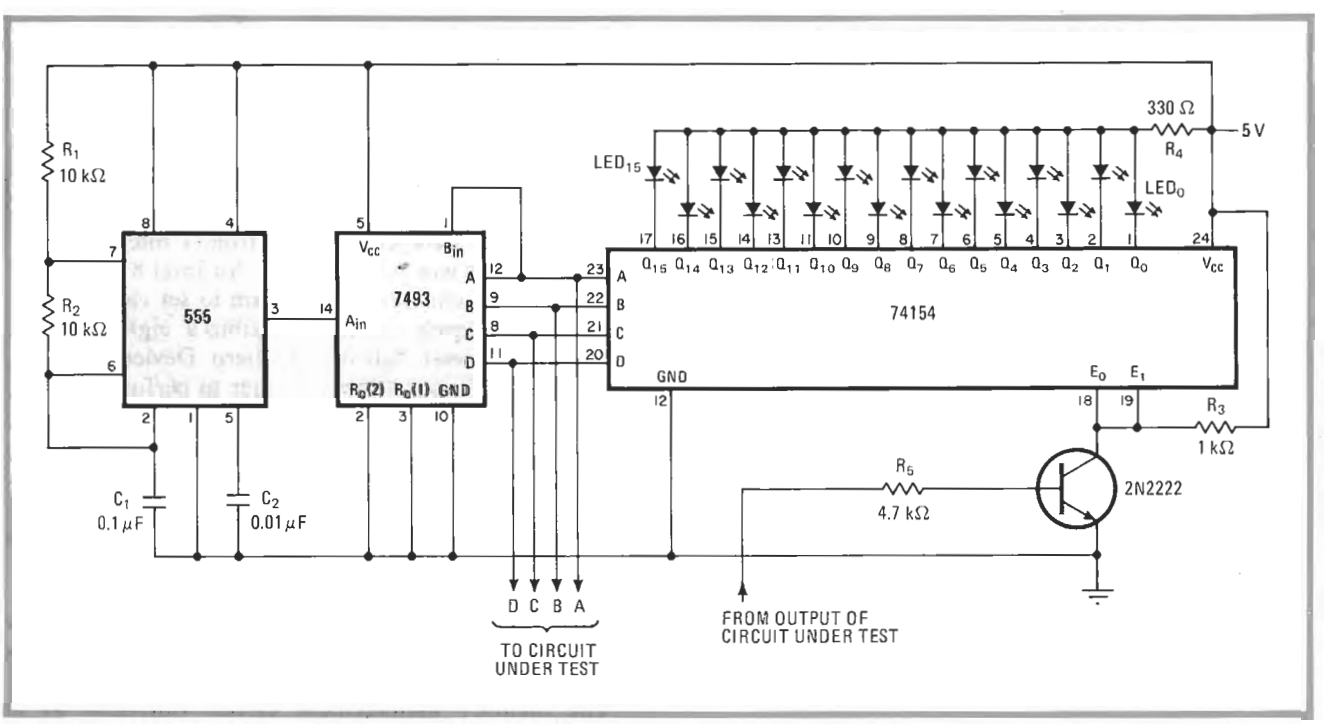
Providing an extremely simple and low-cost alternative to the use of an oscilloscope, this logic analyzer will determine the truth table of circuits with as many as four inputs. The state of the circuit for a single monitored output is displayed by a four-by-four array of light-emitting diodes arranged in a Karnaugh-map configuration. Resistor-, diode-, and transistor-transistor-logic circuits can be checked directly, and only one input/output buffer is required to check complementary-MOS designs.

The analyzer's three basic functions—timing, scanning, and display—are achieved with only three chips: the 555 oscillator, the 7493 4-bit counter, and the 74154 4-to-16-line decoder. The 555, running at a minimum frequency of 480 hertz to eliminate display flicker, clocks the 7493 through its 16 states continuously. As a result, a binary sequence of 0–15 periodically drives the four inputs of the circuit under test. These logic signals are also applied to the decoder chip. Consequently if the instantaneous output of the circuit point under test is high for any given set of input variables A–D, the LED corresponding to the 4-bit output number of the 7493 will light up.

The analyzer may be easily expanded to test circuits having more than four inputs by adding the appropriate number of counters, decoders, and LEDs. The clock frequency must also be increased to minimize flickering in the display.

A higher clock frequency will reduce the on-time of each LED, however. In order to compensate for this reduced brightness, resistor R_4 must be made proportionally smaller. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.



Logic functions. Low-cost logic analyzer, complete with light-emitting diodes arranged in Karnaugh-map configuration, monitor four-input circuit response. RTL, DTL and TTL circuits may be checked directly; only one I/O buffer is needed for C-MOS designs.