frequency counter

Logic IC's are nowadays so cheap that it is possible to build a digital frequency counter for a very small outlay. The circuit described here is based on the popular 74 TTL logic family. The first part deals with the basic counter, and in a subsequent article additions to the instrument will be described.

Specification

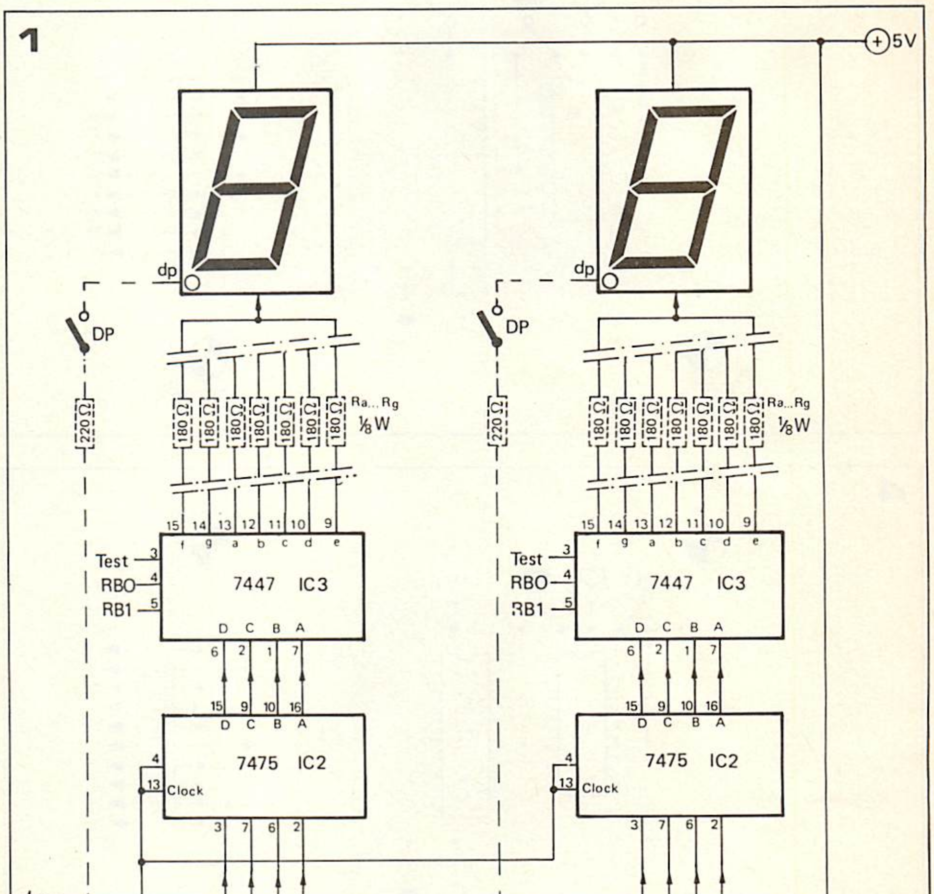
Input sensitivity (frequency measurement)	1.7 V p-p.
Input sensitivity (period measurement)	2.6 V p-p.
with an input risetime of 0.5 μs/V.	
Maximum input frequency	18 MHz.

n its basic form the instrument is a sixigit frequency/period meter. The basic ounter/latch/display is shown in figre 1, which is the circuit of two stages f the counter, showing how the 7490's re cascaded, and how the interconections between the latch and reset nputs are made. The segment series reistors are shown dotted, as the circuit nay be used with either Minitron or LED displays, and series resistors are ot required with Minitrons.

. p.c. board for one stage of the ounter/latch/display decoding is given n figure 2. Six of these boards are reuired for the six-digit counter. The isplays are all mounted on a single oard to which the counter boards are vired, either with wire links, as in figre 3, or if LED displays are used, via egment resistors, as in figure 4.

Figure 5 shows the pinout and voltage/ urrent curve for a Minitron display ype 3015F. Note that for use with a 447 decoder the points shown as round are in fact commoned to +5 V. . p.c. board for use with Minitron dislays is shown in figure 6, and the component layout in figure 7, showing the onnections to a counter board.

1



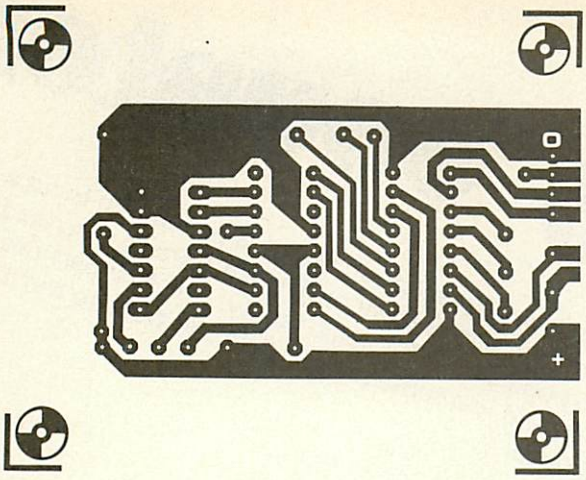
Parts list for figure 1

IC's:
IC1 = 7490
IC2 = 7475
IC3 = 7447

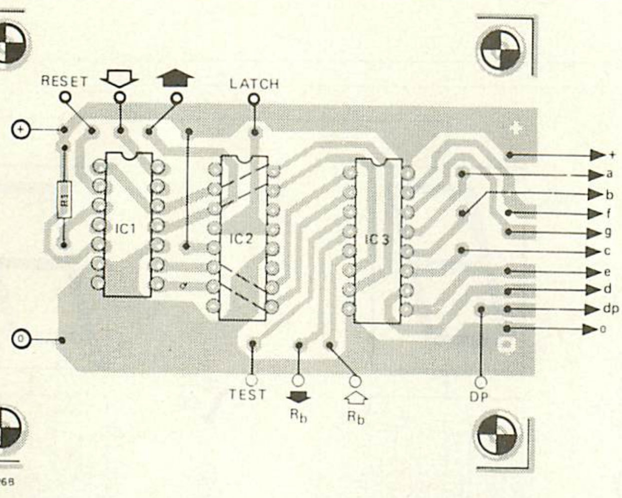
Resistors:
R1 = 1 k
$R_a \ldots R_g$ = 180 Ω (LED display only)

igure 1. Two stages of the counter/latch/ isplay circuit, showing how the counters are ascaded.

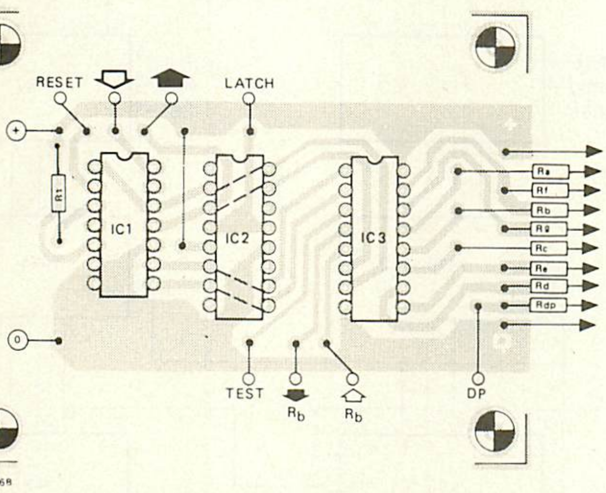
2



3



4



5

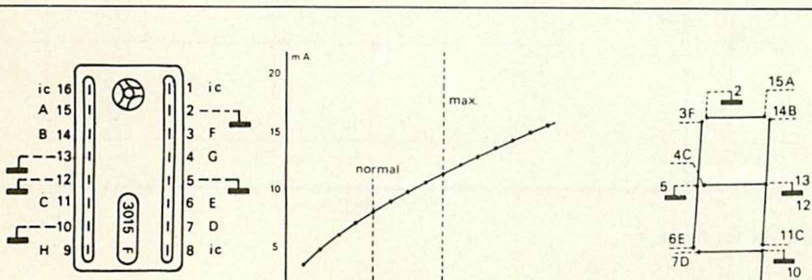


Figure 2. P.c. board for one decade of t counter, latch and display driver.

Figure 3. Component layout for figure 2 usi Minitron displays.

Figure 4. Component layout for figure showing segment resistors for LED displa

Figure 5. Pinout and characteristics of Mi tron.

Figure 6. P.c. board for Minitron displa

Figure 7. Component layout for Minitr display.

Figure 8. Pinouts of three popular LED d plays.

Figure 9 shows the corresponding boar for use with LED displays. Most com mon anode LED displays are pin com patible with respect to the cathode (se ment) connections, but some types hav multiple anode connections (usuall pins 3 and 9). These are catered for o the board, but if a display is used th does not have anode connections t these pins it may or may not be neces ary to cut them off, depending o whether or not they are N.C. (no con nection).

The pin connections of three popula LED displays are given in figure 8. Fo further data on common-anode LED di plays see Elektor No. 3 page 451.

Photographs 1 and 2 show the genera appearance of the display/counter boar assembly, and also how the segmen resistors are soldered to the back of th display board when using LED displays

Control logic

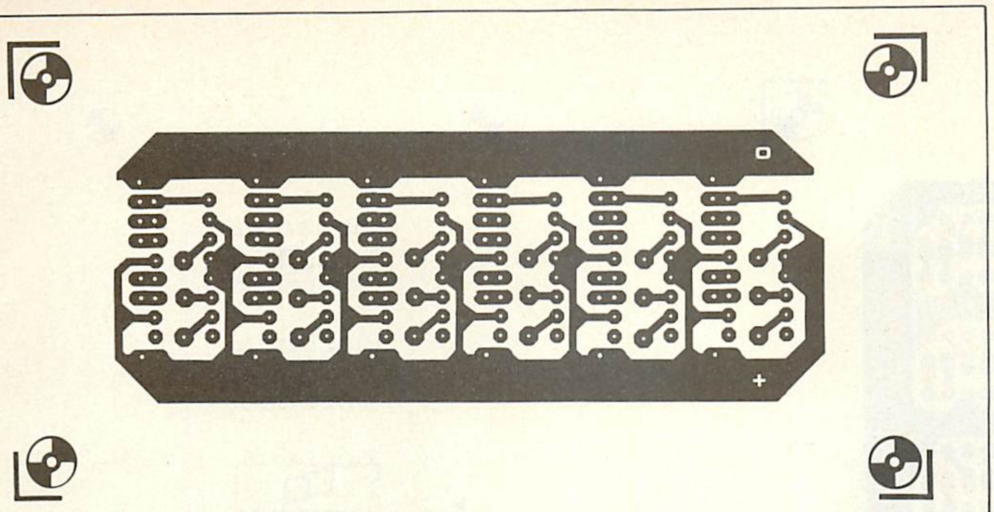
To make the decade counter just de scribed function as a frequency counte various control signals must be applie to it. Firstly, the pulses to be counte must be gated into the first stage of th counter. Secondly, after the coun period has ended the count must b stored in the latch. The counter mus then be reset ready for the next count All these functions are performed b the control logic, the circuit of which i given in figure 10.

The counter will operate in two basi modes, frequency and period. In th frequency mode incoming pulses ar counted for a period of time dependen upon the counter gate period. Thus i the incoming frequency was 100 kH and the gate period 1 s then the coun displayed would be 100000.

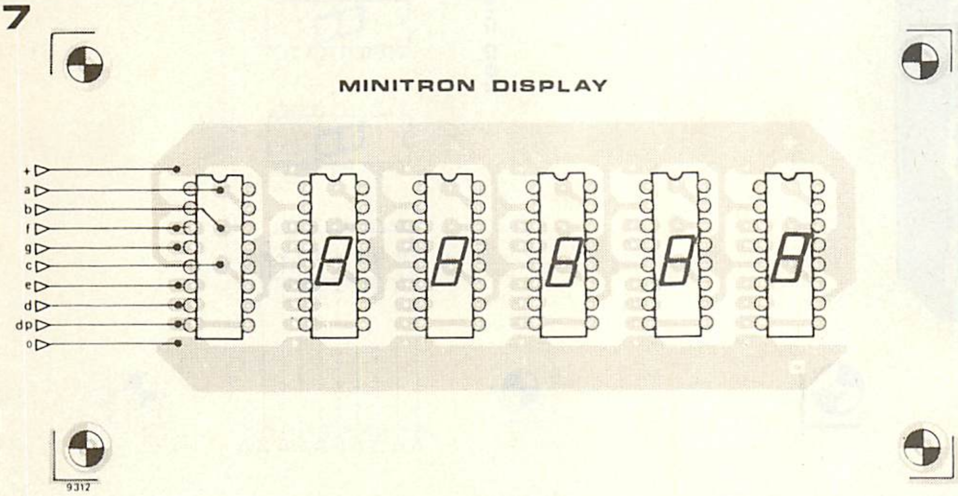
In the period mode the internal fre quency reference of the counter is itsel counted and is gated by one cycle of th incoming signal. Thus, if the interna reference frequency was 100 Hz, an the signal to be measured had a perio of 1 s, then the count displayed woul be 000100. Of course the decimal poin on the display board can be shifted s that this could be displayed as 1.00 (se below).

The control logic operates as follows. I

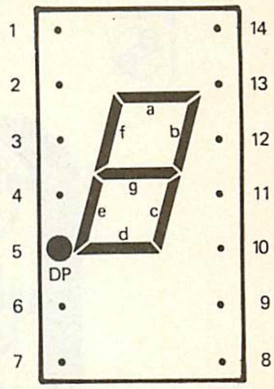
6



7



8



Opcoa SLA 1

Pin

1 Cathode a
2 Cathode f
3 NC
4 NC
5 NC
6 Cathode DP
7 Cathode e
8 Cathode d
9 NC
10 Cathode c
11 Cathode g
12 NC
13 Cathode b
14 Common Anode

Hewlett-Packard

Pin 5082-7730

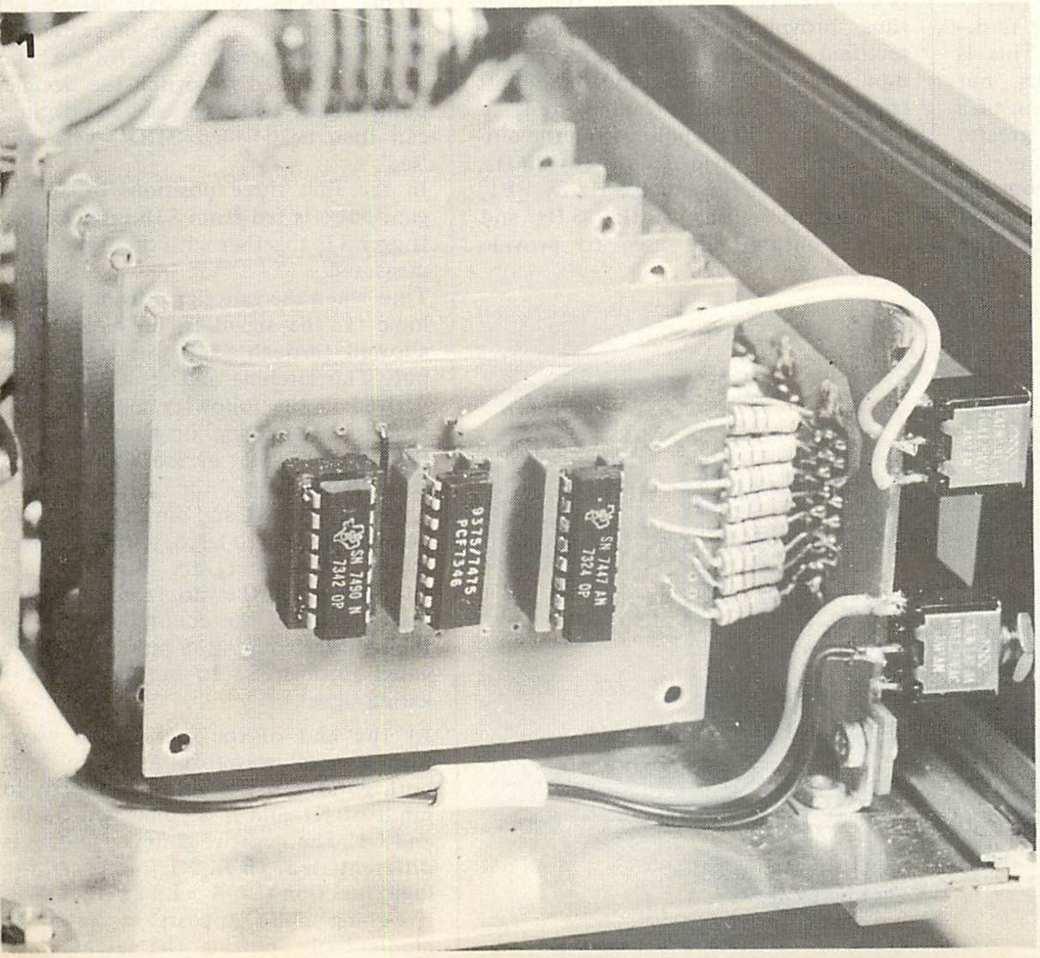
1 Cathode a
2 Cathode f
3 Common Anode
4 No pin
5 No pin
6 Cathode DP
7 Cathode e
8 Cathode d
9 NC
10 Cathode c
11 Cathode g
12 No pin
13 Cathode b
14 Common Anode

Data Lit 707

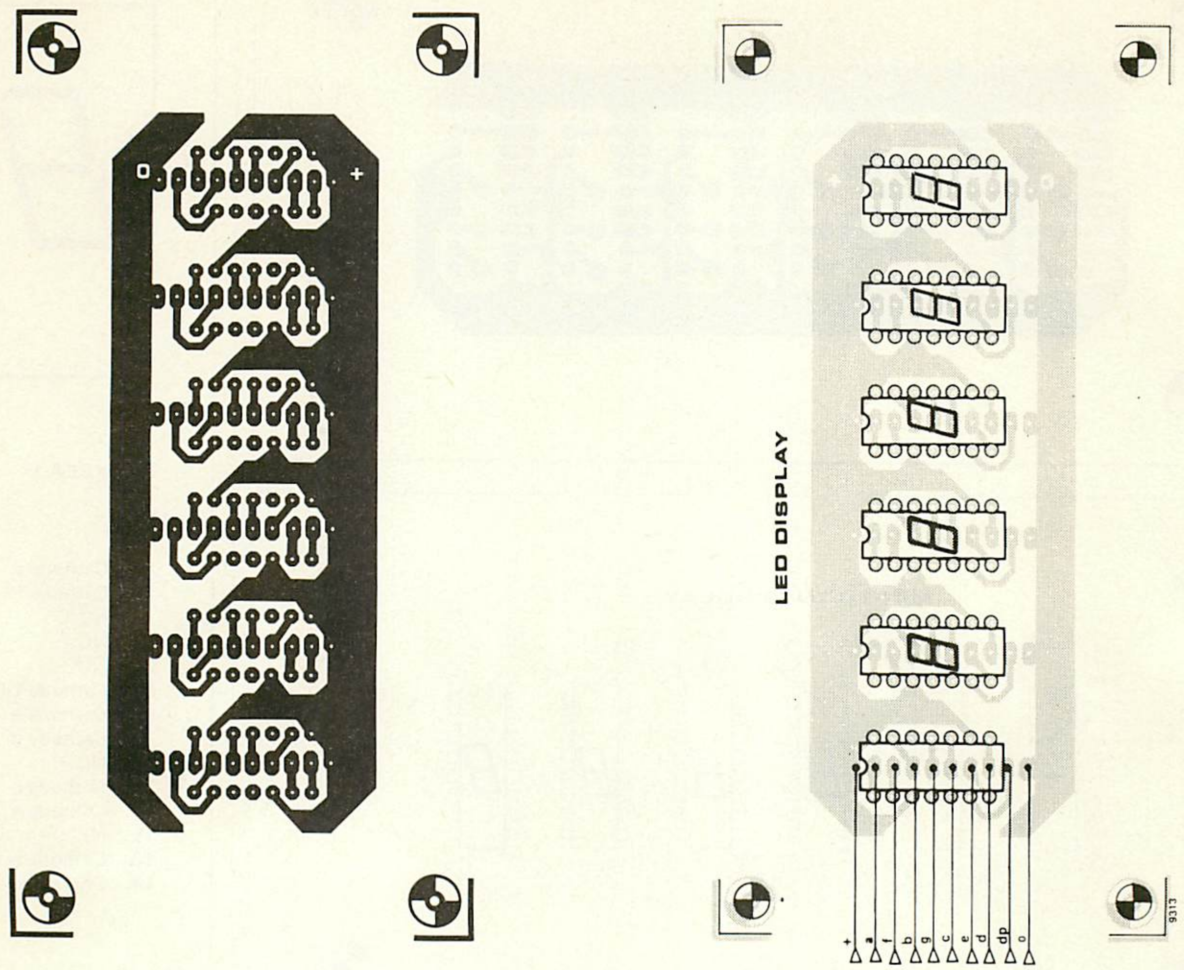
Pin

1 Cathode a
2 Cathode f
3 Common Anode
4 NC
5 NC
6 Cathode DP
7 Cathode e
8 Cathode d
9 Common Anode
10 Cathode c
11 Cathode g
12 NC
13 Cathode b
14 Common Anode

1



9



the basic version of the frequency counter the reference frequency is derived from the 50 Hz mains. This is adequate for many applications, but provision is made for the addition of a crystal-controlled reference for greater accuracy and versatility.

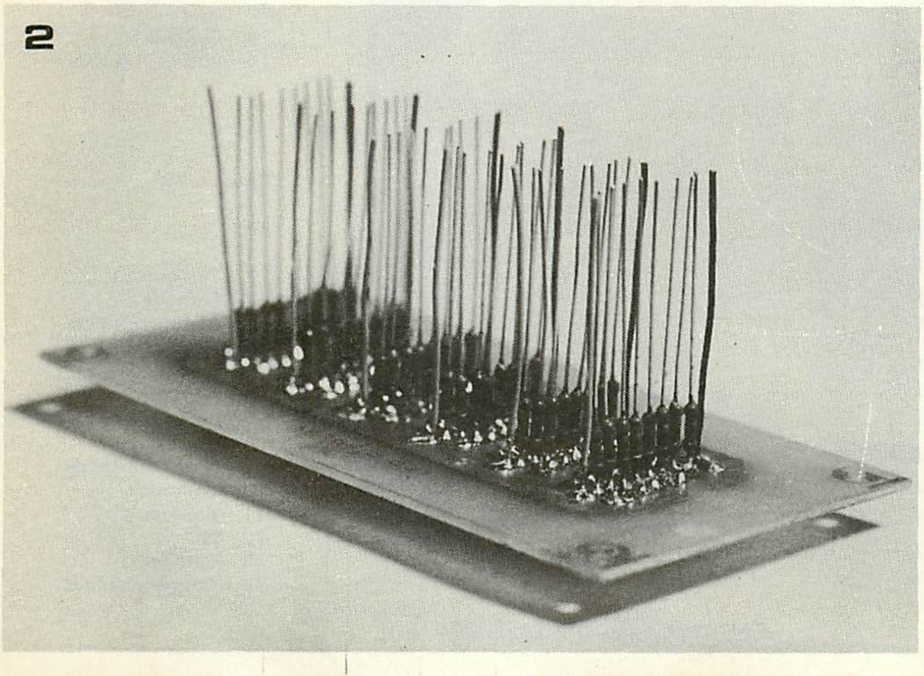
The 50 Hz reference is taken from the secondary of the mains transformer that supplies power to the counter. The A.C. waveform is rectified by the bridge thus providing a 100 Hz full-wave rectified waveform. This is fed to the input of S1 (½ 7413 NAND Schmitt trigger) via R1, and is clamped to 4.7 V by D1. The 100 Hz pulses from the output of S1 are divided down to 50 Hz, 10 Hz, 5 Hz, 1 Hz and 0.5 Hz by FF1, IC4 and IC5. The 50 Hz, 5 Hz and 0.5 Hz outputs are used to provide 10 ms, 100 ms or 1 s gate periods depending on the position of switch S1. For ease of operation, a fifth deck on S1 can be used to switch the decimal point (figure 10b). The switch positions can then be labelled 'MHz', 'kHz' and 'sec'.

In the first three positions of S1 the gate pulse is fed from S1b into Schmitt trigger S2, together with the signal to be measured.

Thus when the gate signal from S1b is at logic '1' the signal to be measured is allowed through S2 to the counter input. The latching and reset signals are derived in the following manner, referring to the timing diagram figure 11. During the gate period (waveform B from S1b 'high') the gating signal B holds pin 9 of N1 and pin 11 of N2 high. The outputs C (to latch) and D (to reset inputs of counter) are thus low. The latch is thus in the 'store' mode and the reset inputs of the counter are low, so the counter counts the pulses which are gated through S2 to output E by the gating signal.

At the end of the gate period waveform B and waveform A (from S1a) both go low. A is connected directly to pin 8 of N1 and B is connected via R4 and C1. The negative-going edge of B is differentiated (B'). N1 performs the logic function $C = \overline{A + B}$ so a short positive-going pulse appears at output C, momentarily putting the latches into

2



10a

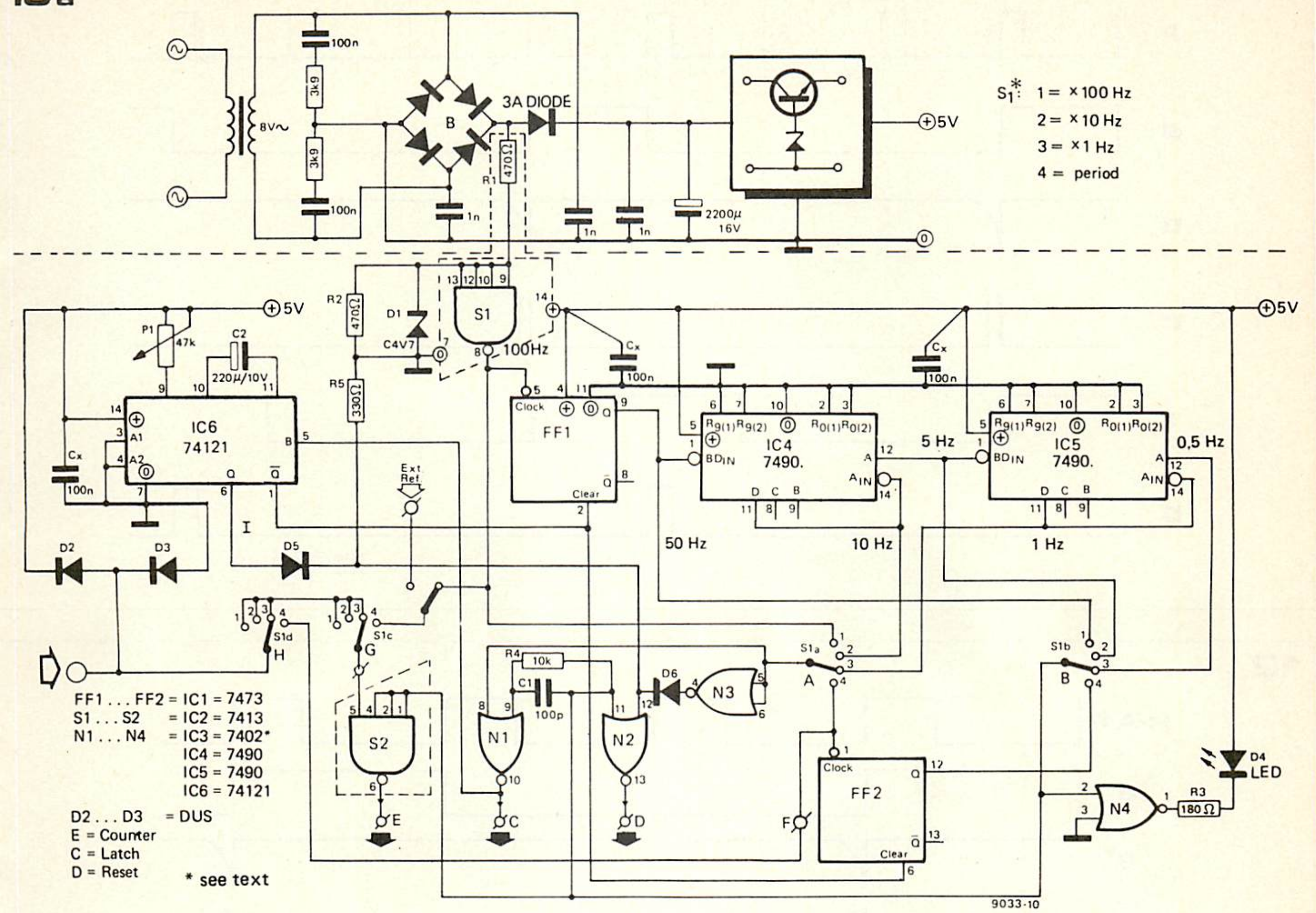
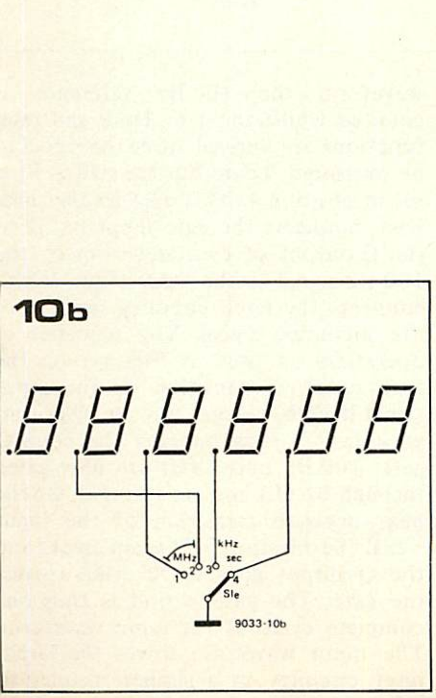


Figure 9. P.c. board and component layout for LED display.

Figure 10. Circuit diagram of control logic.

10b



the 'enable data entry' mode and thus storing the count. This pulse also triggers the monostable IC6, which performs several functions. Firstly, its Q output holds the input to S1 high, thus blocking the 100 Hz pulses to FF1. It also holds pin 12 of N2 high, so the output remains low. The $\overline{Q}$ output clears FF1. When the monostable resets the timebase will restart. The next positive transition of the A signal will be inverted by N3, and the input (pin 12) of N2 will be pulled low by R5. Since the other input is connected to the B signal, which is already low, the output of N2 goes high for the duration of the positive A pulse, thus resetting the counter. When the B signal goes high again the counter commences another count and the sequence repeats. D4 lights when the gate is open.

The pulse length of the monostable IC6 can be varied by P1. It is apparent that this pulse length determines the time for which the timebase is disabled, and hence the interval between counts. This facility is useful, as with a short count interval the continual variation in the last digit can be annoying. A longer count interval will alleviate this. On the other hand, when a rapid succession of measurements is to be taken then a short count interval is useful.

Period Measurement

To measure the period of the incoming

Parts list for figure 10

Resistors:
R1,R2 = 470 Ω
R3 = 180 Ω
R4 = 10 k
R5 = 330 Ω
P1 = 47 k, lin.

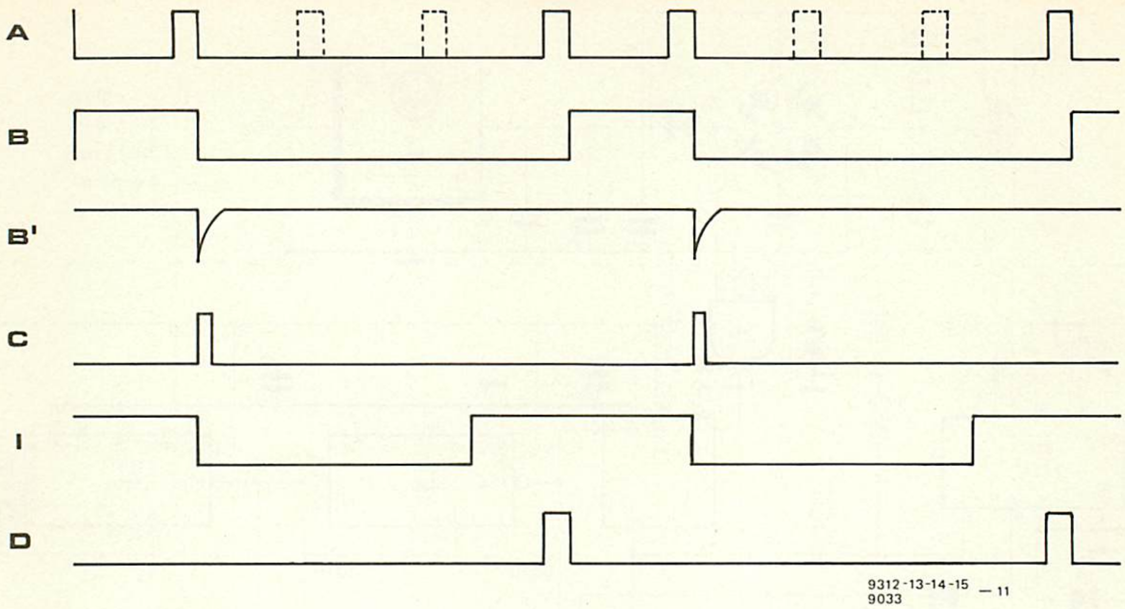
Capacitors:
C1 = 100 p
C2 = 220 µ, 10 V
C_x = 100 n

Semiconductors:
D1 = zener 4.7 V, 250 mW
D2,D3,D5,D6 = DUS
D4 = LED

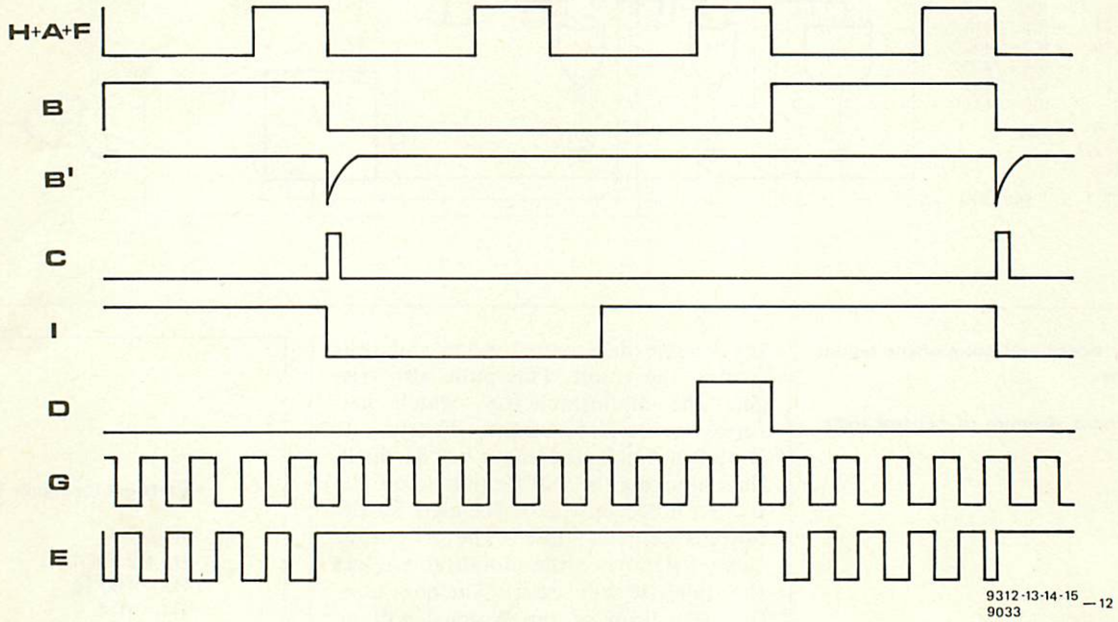
IC's:
IC1 = 7473
IC2 = 7413
IC3 = 7428 (7402)
IC4,IC5 = 7490
IC6 = 74121

Sundries:
S1 = 4-pole 4-way switch (or 5-pole 4-way, see text)

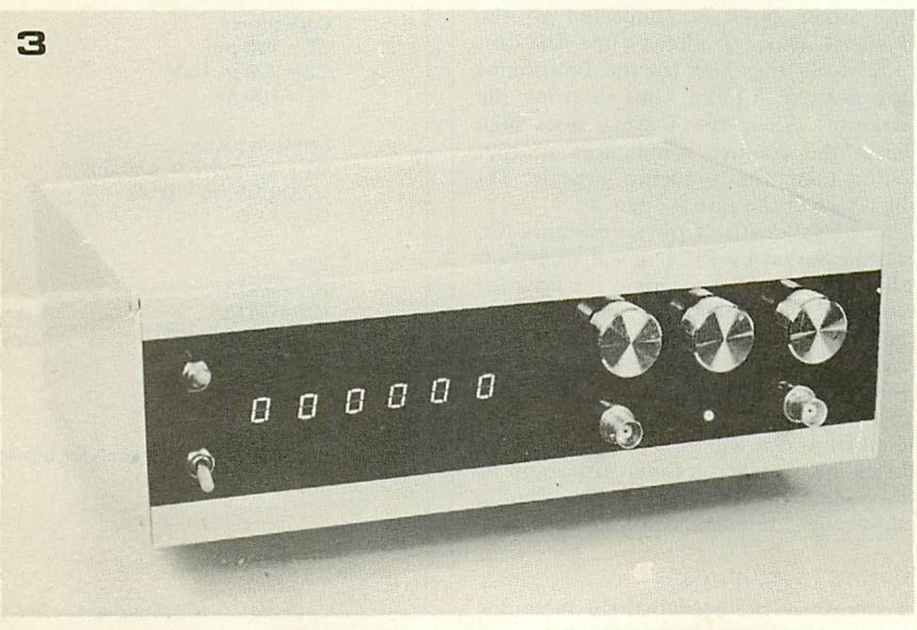
11



12

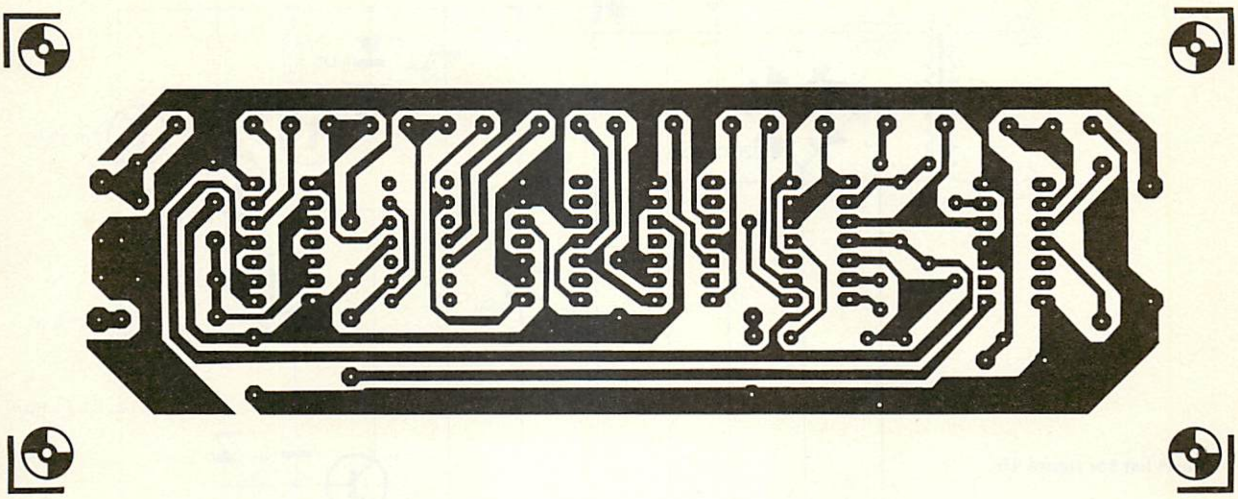


3

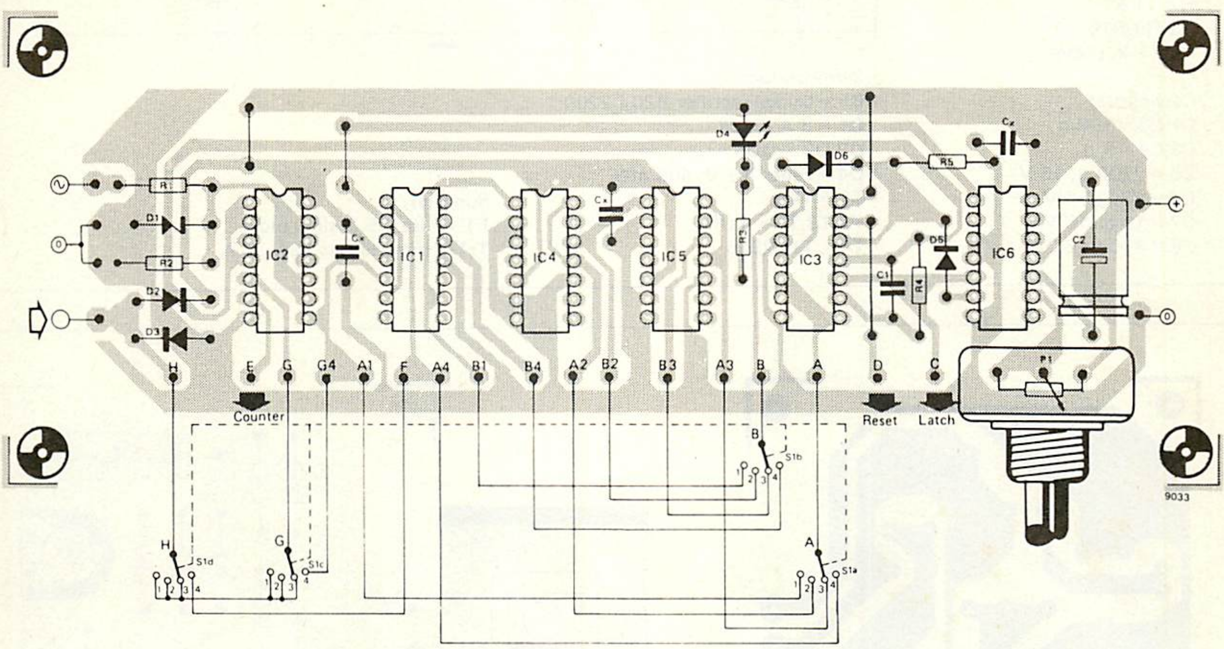


waveform the 100 Hz reference i counted whilst the gate, latch and rese functions are derived from the signal t be measured. To do this the switch S1 i set in position 4. This disables the time base, connects the gate input of S2 t the Q output of FF2 and connects th 100 Hz signal to the other input. It als connects the latch circuitry input A t the incoming signal. The sequence o operations is thus as follows: on th first negative transition of the inpu signal H FF2 clocks and its Q outpu goes to '1' thus opening the counte gate. 100 Hz pulses (G) are now gate through S1 (E) and are counted. On th next negative transition of the inpu signal the flip-flop FF2 again clocks an the Q output goes to '0', thus closin the gate. The gate period is thus on complete cycle of the input waveform The input waveform drives the latch reset circuitry in a similar manner t

13



14



igure 11. Timing diagram of counter in frequency measuring mode.

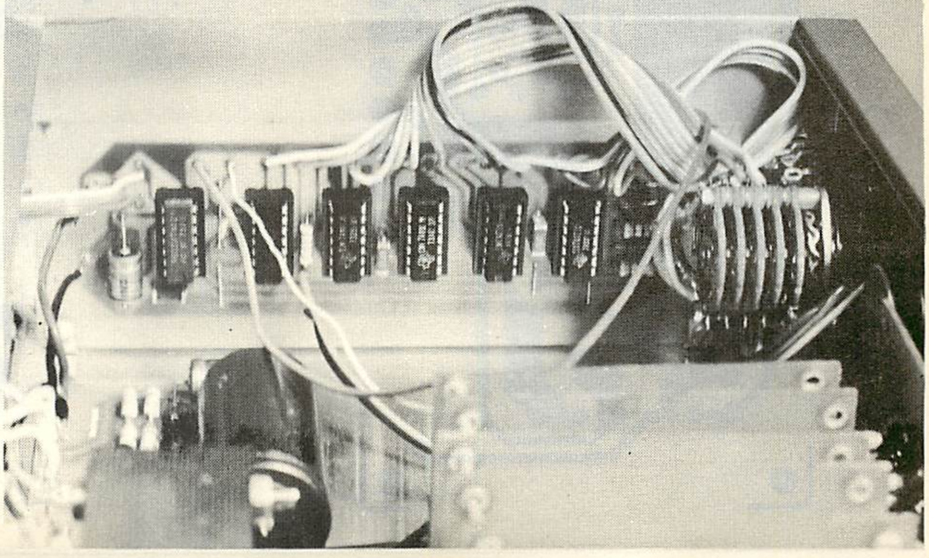
igure 12. Timing diagram of counter in eriod measuring mode.

igure 13. P.c. board for control logic.

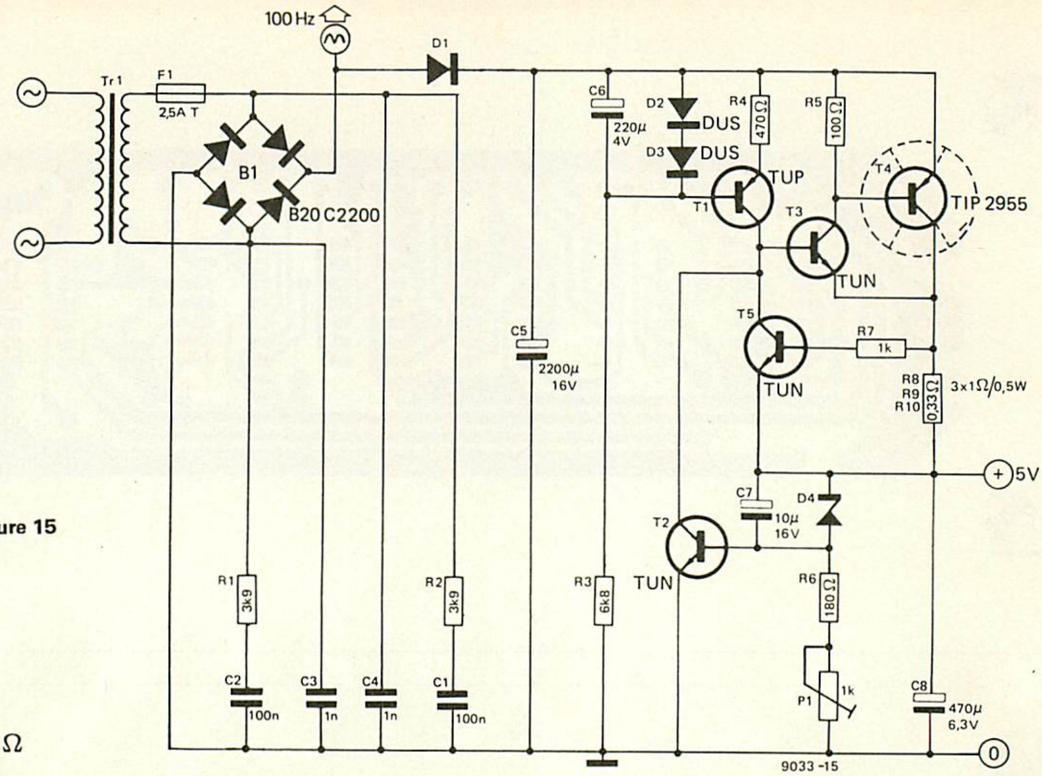
igure 14. Component layout for control ogic.

hat for a frequency measurement, and he timing diagram is shown in figure 12. Of course, the A signal is now he input signal, and the B signal is the Q output of FF2.
With a 100 Hz reference frequency and

4



15



Parts list for figure 15

Resistors:
R1,R2 = 3k9
R3 = 6k8
R4 = 470 Ω
R5 = 100 Ω
R6 = 180 Ω
R7 = 1 k
R8,R9,R10 = 1 Ω
P1 = 1 k, preset

Capacitors:
C1,C2 = 100 n
C3,C4 = 1 n
C5 = 2200 μ, 16 V
C6 = 220 μ, 4 V
C7 = 10 μ, 16 V
C8 = 470 μ, 6,3 V

Semiconductors:
B1 = bridge rectifier B20 C2200
D1 = 3 A diode
D2,D3 = DUS
D4 = zener 4.7 V, 400 mW
T1 = TUP
T2,T3,T5 = TUN
T4 = TIP 2955

Sundries:
F1 = fuse 2.5 A slow blow
Tr1 = transformer 12 V, 2 A

16

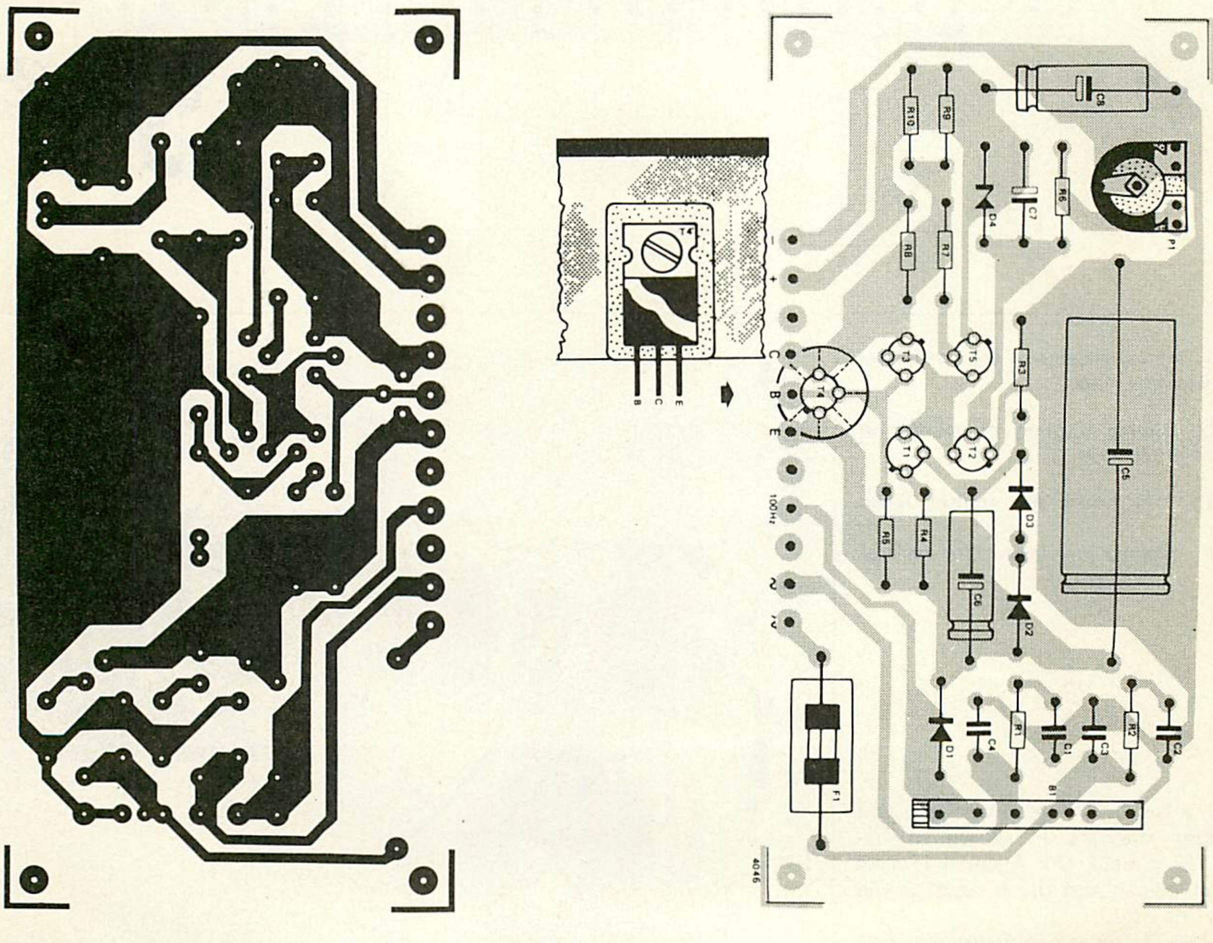


Figure 15. Power supply for frequency counter.

Figure 16. P.c. board and component layout of power supply.

he gate periods of 10 ms, 100 ms and s the range of the instrument is mited. It is only possible to obtain a ull-scale reading in the period mode when the period is 9,999.99 seconds. For a period of 1 s the display will be nly 000100, a resolution of one art in a hundred. Clearly, for short eriod measurements a higher reference requency is necessary to obtain a larger ount and hence a better resolution. rovision is made for feeding in an external reference frequency by breaking he circuit at the point marked 'EXT REF'. In the frequency mode the maximum and minimum frequencies which an be measured are limited by the gate eriods. For instance with a 1 s gate eriod a frequency of 100 Hz will only e measured with a resolution of one art in a hundred, whilst with a 10 ms ate period an input frequency of reater than 99.9999 MHz would cause he counter to overrange. However, ince the upper frequency limit of the TL counters used in the circuit is only 8 MHz anyway, this problem does not rise.

A printed circuit board and component ayout for the control logic board are iven in figures 13 and 14, showing the onnections to the switch.

Power supply

A suitable power supply for the frequency counter is shown in figure 15. This is well decoupled against mains-borne interference and has a 100 Hz utput for the reference frequency. A oard and component layout for the ower supply are given in figure 16. As the complete frequency counter raws about 2 amps, the series regulator ransistor T4 should be mounted on an dequate heatsink. If the unit is housed n an aluminium case then the back of he case should prove suitable.

n a future issue we shall be describing dditions to the frequency counter, otably an input preamplifier to increase the input sensitivity.

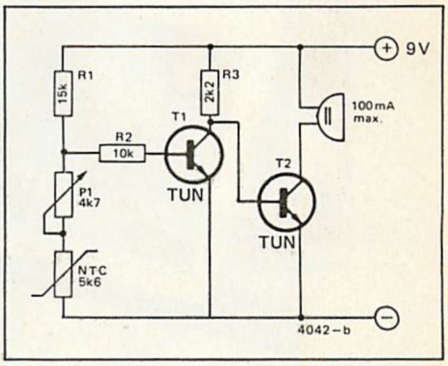
J.P. Kuhler jr.

humming kettle

Those who have in the course of time lost the whistle of their domestic kettle and the unfortunate ones who do not possess a whistling kettle at all, who must boil water without the aid of an acoustic signal, are encouraged by the author not to resign themselves to this unsatisfactory situation. A very modest amount spent on components together with a little work puts a 'humming kettle' within everyone's grasp!

The circuit is so simple that further explanation is hardly necessary. As the temperature increases, the resistance of the NTC drops until at a certain moment (adjustable with P_1) transistor T_1 cuts off, so that T_2 conducts and the buzzer is activated.

Of course the circuit must be mounted in, on, or in the immediate vicinity of the kettle.



R. Buggle

active flash slave

For those who have often been annoyed by badly illuminated flash photographs and also dislike the tangle of cables involved in using two flashguns, the flash slave is the only solution.

The author spent quite some time building several slave units before arriving at the design presented here, which has the advantages that it requires no separate supply voltage and that both electronic and ordinary flashguns can be operated. Four silicon photovoltaic cells (BPY 11) form a light sensor. Undoubtedly other types will do, too. The thyristor must be of a type with a very low firing voltage; the TIC 46 used here performs quite well. The circuit itself needs little comment: only that the polarity of the flash connection should be correct; the 'plus' should be connected to the centre pin of the connecting cable. The circuit can best be housed in a small, transparent plastic box.