Build this up-to-the-minute LSI design

500MHz 7-digit frequency meter

Want a high-performance digital frequency meter that's easy to build? This new design uses just five ICs, measures period and frequencies up to 500MHz, and features a bright seven-digit display. At around $135 for the kit, it represents a considerable saving over comparable commercial units.

by RON DE JONG

Once again, advances in IC technology have enabled us to present a new DFM with better performance, yet fewer components, than any of our previous designs. In 1970, for example, we published a design for a three-and-a-half-digit 70MHz counter which employed a total of 43 ICs. That was superseded in 1973 by a four-and-a-half-digit 200MHz design employing 24 ICs, and followed by 200MHz seven-digit versions in 1977 and 1978 using 12 ICs.

Confirming this trend, our latest offering more than halves the number of ICs used previously, reducing the count to just five (not including the power supply regulators). There is far less internal wiring than before and construction is more straightforward. Construction should take you no longer than three or four hours.

Prototype (below) measures to 500MHz and features period measurement, 7-digit resolution and switchable gating times.

We think that you'll like the new styling too. Because there are fewer components, the PCB assembly is much more compact and fits comfortably into an attractive PacTec high-impact plastic case. Add a fancy Scotchcal front panel and you've got a high-performance DFM with looks and performance to rival commercial units costing many times the price.

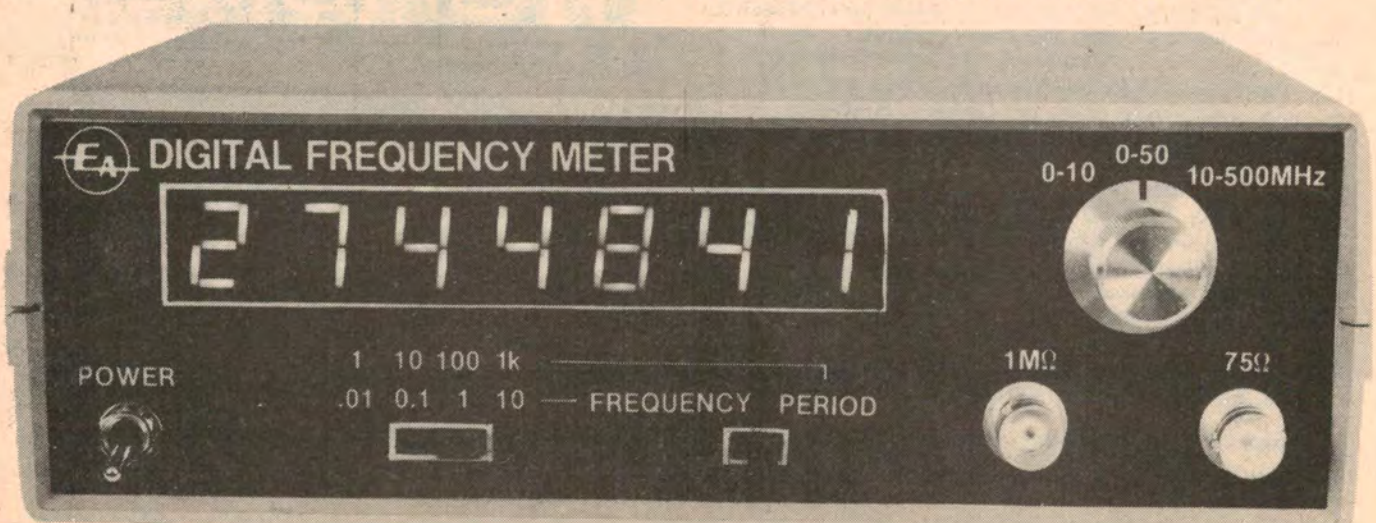
FEATURES

Use of the latest LSI circuitry means new features at minimum extra cost. As can be seen from the photograph, there are just four front-panel controls: a power on/off switch, a gating time switch, a function switch to select frequency or period measurement, and a range switch. In addition, the front panel carries two BNC input sockets and the seven-digit 12.7mm display.

Features not seen on previous "Electronics Australia" DFMs, but included here, are: leading zero blanking; provision for period measurements; and switchable gating times. Our new DFM will also run to 500MHz – compared to 200MHz (max) for previous designs – provided that you build in the optional prescaler circuitry.

Essentially, you have two options when building this new DFM – you can either build the full 500MHz version, or you can save yourself around $30 by building a 50MHz version. If you are not involved in VHF work, then the 50MHz version is the one to go for. All you have to do is leave out the two prescaler ICs (IC4 and IC5) associated with the 500MHz range. More about this later on.

Gating time is selected by a four-position slide switch which selects either .01, 0.1, 1 or 10 seconds. The longer the gating time, the more digits displayed and the greater the resolution. Of course, the update time also increases with increasing resolution. Selectable gating makes for a more versatile DFM – you can opt for fast update times when the situation demands it, or opt for maximum resolution.



Period measurement is another quite useful feature of this DFM and is not normally found on commercial units priced below $1000. It enables very accurate measurements of low frequency signals, ie, those below about 10kHz. In period mode, the gating time selector switch also selects the number of input cycles over which the period is to be measured – either 1, 10, 100 or 1000 input cycles – while the display reads in multiples of 0.1μs. For example, if 100 cycles was selected and the display read 8266312, then inverting this on a calculator gives 120.9729Hz – which is far more accurate than a direct frequency measurement of 120Hz.

The range selector switch has three positions: 0-10MHz, 0-50MHz and 10-500MHz. On the first range, measurements can be made up to 10MHz with 1Hz resolution (one second gating time), while the second range measures frequencies up to 50MHz with a resolution of 10Hz (the input frequency is divided by 10 on this range). The third range is for measurements from 10MHz to 500MHz and, since the input frequency is now divided by 100, the resolution is 100Hz.

As noted earlier, two BNC input sockets are provided on the front panel. One of these has an input impedance of 1MΩ shunted by about 50pF, and is used for the first two frequency ranges up to 50MHz. The second input has a nominal impedance of 75Ω and is used for the third range, ie, 10-500MHz. Input sensitivity is about 10mV RMS up to 30MHz, rising to about 100mV RMS at 50MHz.

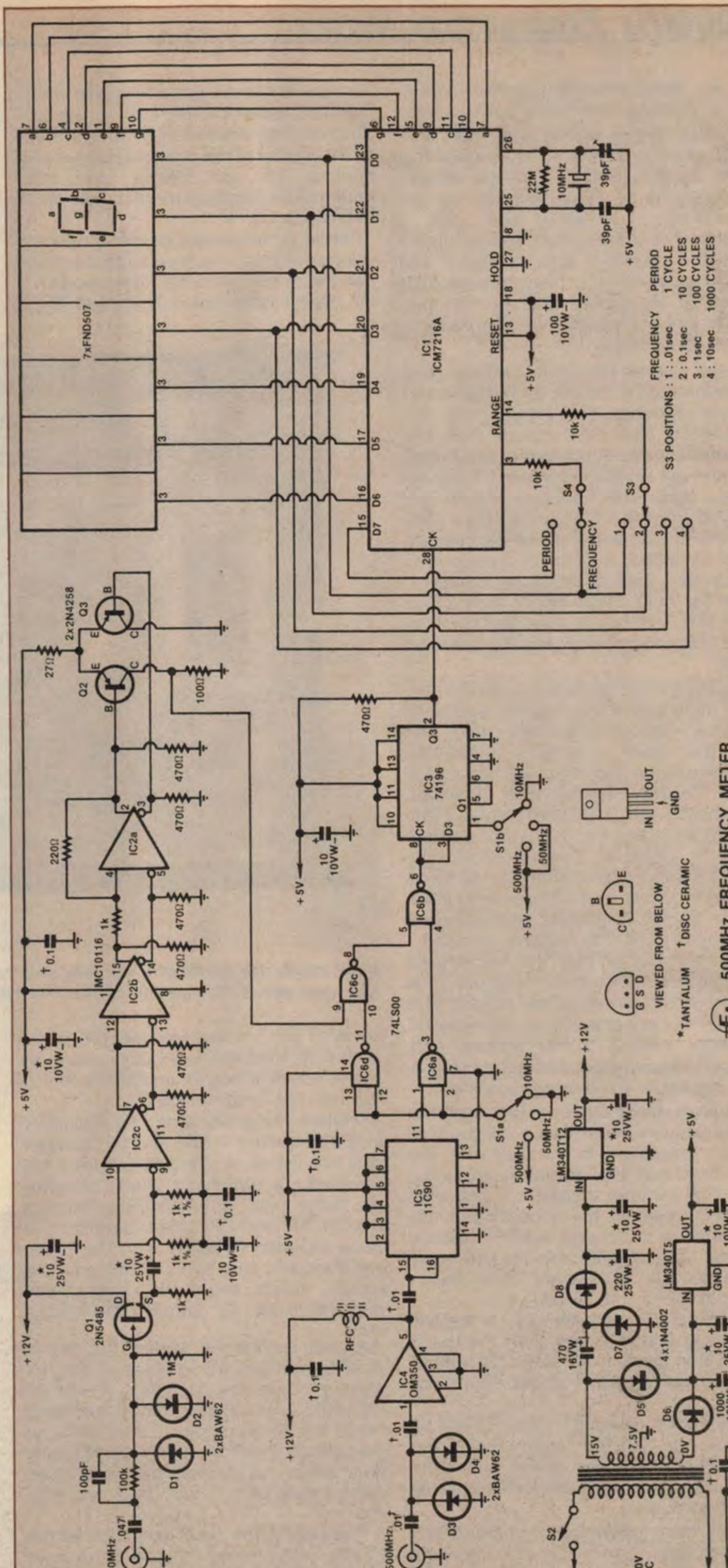
Accuracy of the frequency meter will depend on the accuracy and stability of the crystal timebase. This can be expected to be about 50 parts per million for most available crystals, which is quite adequate for this type of instrument.

Power consumption is fairly modest because of the multiplexed display. The unit is powered from the 240V AC mains and has a current drain of about 300mA from the +5V rail and about 70mA from the +12V rail. Overall power consumption is less than 7W.

HOW IT WORKS

Heart of the circuit is IC1, a 7216A counter chip made by Intersil, Inc, USA. This new LSI chip is virtually a complete 10MHz frequency counter and contains a high-frequency oscillator, a decade timebase counter, an 8-decade data counter and latches, a 7-segment decoder, digit multiplexers, and interface circuitry to drive 7-segment LED displays. All that has to be added to produce a working DFM is a power supply, input preamplifiers and prescalers, a 10MHz crystal, and a LED display.

Referring to the circuit diagram we can see that the 7216A directly drives a 7-digit display consisting of FND507 common-anode 7-segment LEDs. These displays feature large 12.7mm high digits and an integral red plastic filter. This, together with the fact that the displays



can be directly butted together, means that a separate red filter is not required.

Multiplexing is a common technique used when there are a large number of digits in a display since it greatly reduces the amount of wiring and the current consumption. Basically, one digit is displayed at a time, starting with digit 0 then progressing in turn to digit 7 and then back to 0. This sequence is repeated so quickly that, due to persistence of vision, all of the digits appear to be continuously lit.

In the case of the 7216A, multiplexing is performed by pulling each digit driver high in sequence, thus enabling the corresponding digit. At the same time, the appropriate segment drivers are pulled low turning on the segments for the required digit. The multiplex signals are derived from the 10MHz oscillator used in the timebase and the multiplexing rate is set at 500Hz; ie, it takes 2ms to scan the display. Each of the digits, however, is on for only 244μs rather than 250μs since the 7216 has an interdigit blanking time of 6μs to prevent ghosting between digits.

Segment drive current is quoted as being a minimum of 25mA while typically it is 35mA – quite a respectable value and one that gives a bright easy-to-read display even in high ambient light conditions. Readers should note, however, that there is also a "B" version of IC1 (the 7216B) intended for use with common cathode displays. Unfortunately, the 7216B is only capable of providing 10mA segment current and this results in insufficient display brightness, particularly if the popular FND500 displays are used.

The oscillator on the 7216A is actually a high gain CMOS inverter with pin 25 as the input and pin 26 as the output. This inverter is connected in a "pi-network" oscillator with a 22MΩ resistor connected between input and output to provide biasing of the inverter amplifier.

The load capacitance of the crystal in this circuit consists of the crystal shunt or static capacitance in parallel with the 39pF fixed and 39pF trimmer capacitors. The 39pF trimmer capacitor is provided to compensate for the normal frequency tolerance of the crystal, which is usually around 30ppm, and also for any stray capacitance, including the input capacitance of the 7216A.

Temperature stability of a typical 10MHz crystal is better than five parts per million (ppm) from −20°C to +80°C and the aging rate is about 5ppm per year.

Incidentally, although the 7216A is capable of driving eight digits we decided to only use seven, since the accuracy of the timebase does not justify 8-digit resolution.

Apart from operating as a frequency counter, the 7216A can also measure period. This is accomplished internally by using the input signal to gate through the 10MHz clock to the counter section. The resulting count will be proportional to the period of the input waveform and, because of the 10MHz clock, the counter will display period in units of 0.1 microseconds.

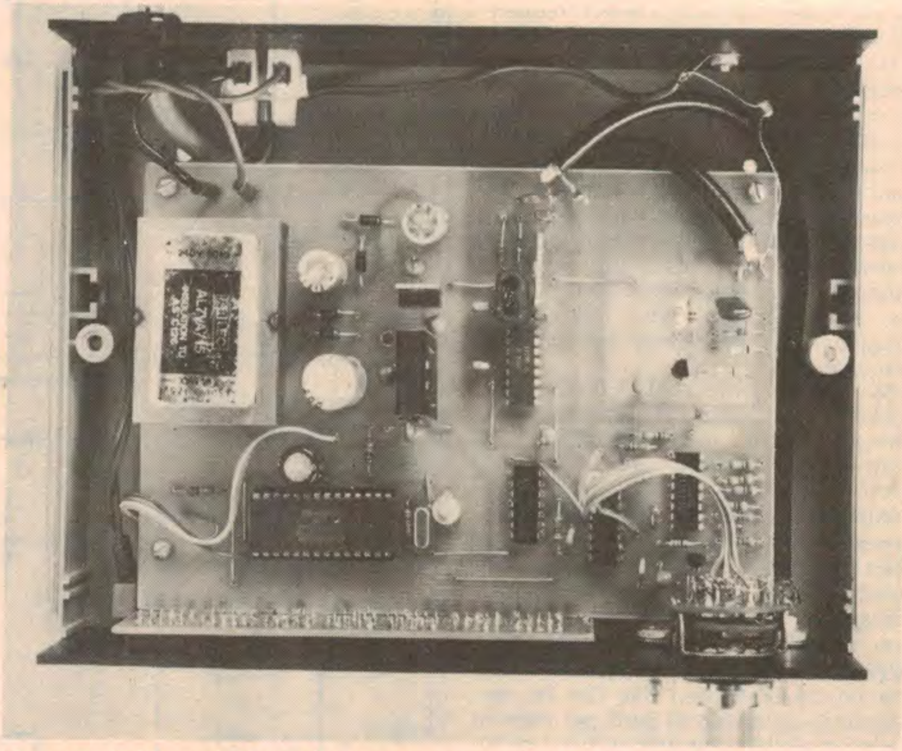
Period or frequency mode is selected using switch S4 which switches the Function input, pin three, to either the D0 or D7 digit enable lines. The internal circuitry of the 7216A compares this signal against its digit multiplex information to see which digit output and hence which function has been selected.

Similarly the gating time of the counter in the frequency mode and the number of input cycles in the period mode are selected via switch S3 which switches the range input, pin 14, to digit outputs D0, D1, D2 and D3. 10kΩ resistors have been included in series with the range and function pins to filter out any fast spikes which might be capacitively coupled from the other digit enable lines.

As we mentioned earlier the gating times which can be selected in the frequency mode are 0.01, 0.1, 1 and 10 seconds. The update times for each range are the same plus 0.2 seconds, so the update time for a one second gating time will be 1.2 seconds and for a 0.1 second gating time it will be .3 seconds, etc.

That covers the basic operation of the 7216A. Let's now take a look at the input preamplifier and prescaler circuits.

Looking at the 50MHz input first, the input signal is coupled in via a .047μF capacitor and a 100kΩ resistor and 100pF capacitor in parallel. Together with two BAW62 diodes, D1 and D2, this input circuit clips the input waveform to 600mV amplitude to prevent damage to the input preamplifier. The 100pF capacitor bypasses the 100kΩ resistor at higher frequencies to prevent attenuation due to the input capacitance of the following FET buffer stage Q1.

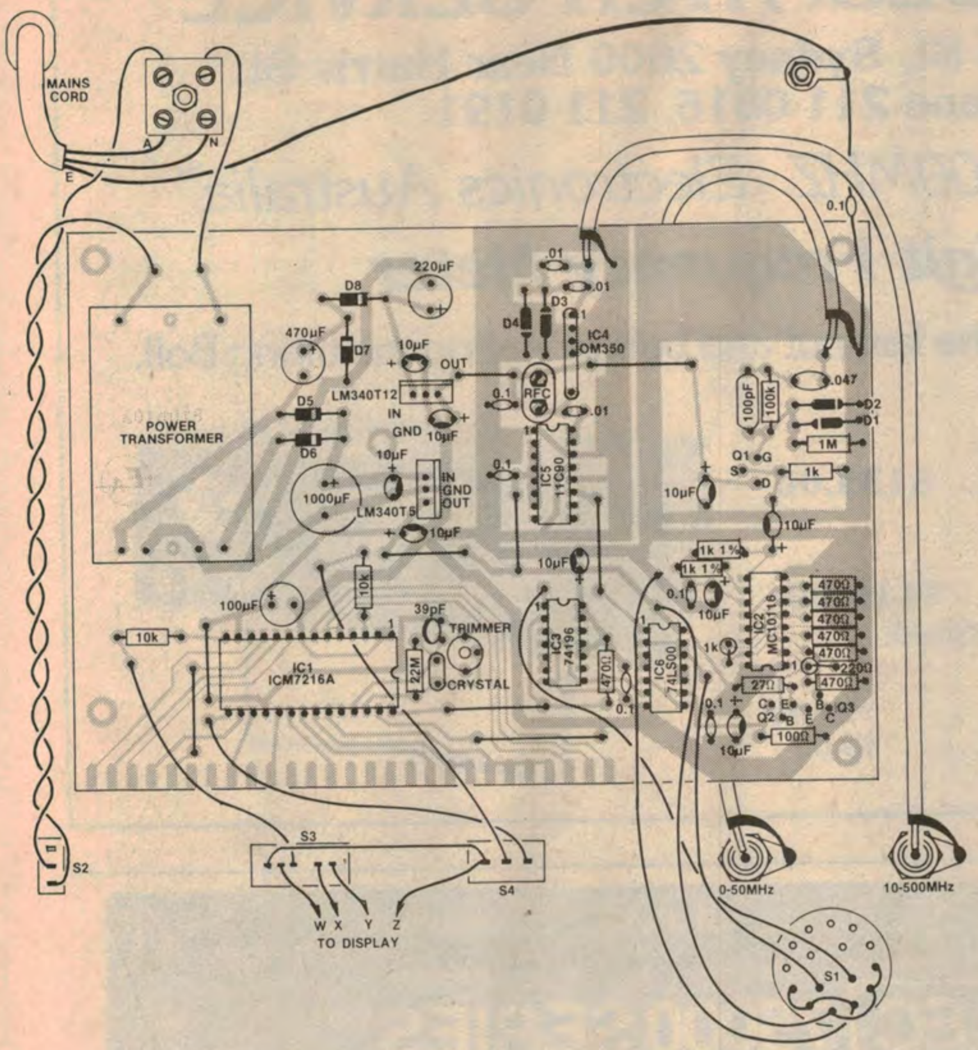


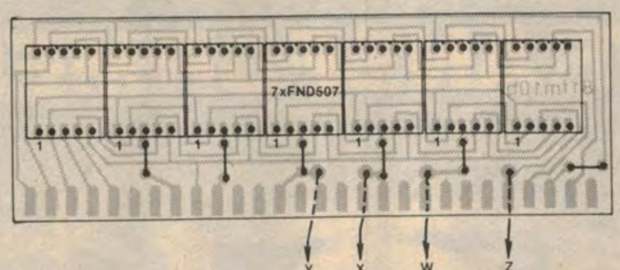
View inside the prototype, showing the completed PCB assembly. Keep all wiring tidy and use 75Ω coax between the BNC connectors and the PCB inputs.

Q1 is a 2N5485 VHF FET arranged as a source follower with the gate connected to ground via a 1MΩ resistor and self-biased via a 1kΩ source load resistor. This drives three cascaded ECL (emitter-coupled logic) receivers IC2c, IC2b and IC2a which comprise an MC10116 triple differential line receiver IC. This basic circuit is used in many commercial designs as well as in the last DFM we described in 1978.

Essentially, each ECL line receiver consists of an NPN differential pair with a constant current source in the "tail" and resistor collector loads. The collector of each transistor is buffered by an emitter follower providing complementary outputs. The emitter outputs are left open – ie, there are no internal pull-down resistors, so that ECL outputs can be OR-ed together to reduce the number of gates in a design. However, in this circuit external pull-down resistors are required on each output.

ECL outputs usually swing ±0.2V about





These wiring diagrams show the PCBs from the component side. The display PCB (right) butts against the main PCB at right angles and is soldered to it via the edge connector strips. Use mains-rated cable for all mains wiring.

SPECIFICATIONS

RANGES (FULL SCALE): 0-10MHz, 0-50MHz and 10-500MHz (optional).

OPERATING MODES: Switch selectable frequency or period measurement.

SENSITIVITY: 10mV RMS to 30MHz; 100mV RMS at 50MHz; typically less than 200mV on 500MHz range.

INPUT IMPEDANCE: 1 MΩ/50pF on 0-10MHz and 0-50MHz ranges; 75Ω on 10-500MHz range.

RESOLUTION: 1Hz on 0-10MHz range; 10Hz on 0-50MHz range; 100Hz on 10-500MHz range.

GATING TIMES: .01s, 0.1s, 1s and 10s; update times 0.2s longer.

ACCURACY: Typically better than .005% ±1 count uncalibrated.

POWER REQUIREMENTS: 240VAC, 7W.

PARTS LIST

1 PacTec plastic case, Model CM 86-225
1 printed circuit board, code 81fm0a, 160 × 110mm
1 printed circuit board, code 81fm10b, 115 x 40mm
1 Arlec AL7VA/15 transformer
1 10MHz crystal (parallel resonant)
1 13mm balun core
1 3-pole 3-position rotary switch
1 panel mounting 1-pole 4-position slide switch
1 panel mounting 1-pole 2-position slide switch
2 BNC panel mounting sockets
1 mains cable and plug
1 grommet/cable clamp
1 2-way mains terminal block
2 solder lugs
1 Scotchcal front panel, 197 x 59mm
1 TO-220 heatsink
½ metre 75Ω coaxial cable
1 tilting bail (optional)
4 19mm tapped brass spacers
½ metre 22B&S enamelled copper wire

SEMICONDUCTORS
1 11C90 prescaler
1 MC10116 triple differential line receiver
1 7216A universal counter
1 OM350 VHF preamplifier
1 74196 decade divider
1 74LS00 quad NAND gate
1 LM340T-5 regulator
1 LM340T-12 regulator
4 1N4002 diodes
2 2N4258 PNP transistors
1 2N5485 VHF FET
4 BAW62 diodes
7 FND507 common anode LED displays

CAPACITORS
1 1000µF 16 VW PC electrolytic
1 470µF 16VW PC electrolytic
1 220µF 25VW PC electrolytic
1 100µF 10VW PC electrolytic
5 10µF 25VW tantalum
4 10µF 10VW tantalum
5 0.1µF miniature ceramic
1 .047µF polyester
3 .01µF miniature ceramic
1 100pF ceramic or polystyrene
1 39pF NPO ceramic
1 39pF trimmer

RESISTORS (¼W, 5% unless stated)
1 x 22MΩ, 1 x 1MΩ, 1 x 100kΩ, 2 x 10kΩ, 2 x 1kΩ, 2 x 1kΩ 1%, 7 x 470Ω, 1 x 220Ω, 1 x 100Ω, 1 x 27Ω

MISCELLANEOUS
Mains-rated hookup wire, rainbow cable, machine screws and nuts, solder, etc.

a reference voltage of around 3.7V. This reference voltage is actually provided by the 10116 on pin 11 and we have used it to bias the first line receiver IC2c via two 1kΩ resistors. A 0.1μF capacitor and 10μF tantalum capacitor provide decoupling of the reference voltage.

The stage following IC2b is IC2a which operates as a Schmitt trigger by virtue of the positive feedback network consisting of the 220Ω and 1kΩ resistors. Input signals to this Schmitt trigger must exceed its two hysteresis trigger levels before the output of the trigger will change, so this stage provides a good deal of noise immunity as well as squaring up the input signal.

Assuming a swing of ±0.2V at the output of IC2a, the hysteresis voltage levels are ±0.15V which is greater than the maximum output offset voltage of IC2b so no bias adjustment of IC2c is required. Incidentally, we can also work out the theoretical sensitivity of the amplifier by dividing the hysteresis voltage by the gain of the two previous stages. This calculation gives a typical sensitivity of 6mV and since the gain of the FET buffer is about 0.5, the expected sensitivity of the unit is about 12mV peak.

The ECL outputs of IC2a are converted to TTL levels by transistors Q2 and Q3, both 2N4258 high speed switching transistors. Since the two ECL outputs from pin 2 and pin 3 swing ±0.2V about 3.7V then either Q2 or Q3 will be on. If, for example, pin 3 is low then Q3 will turn on and Q2 will turn off. Since one transistor will always be on, the current through the 27Ω emitter resistor will be virtually constant at around 32mA or so. The output from the stage is taken from the 100Ω collector resistor of Q2 and will swing between about 0.1 and 3.2V which is directly compatible with the following TTL stage IC6c.

IC6 is a 74LS00 quad NAND gate which we have connected up as a two-input multiplexer. One input, pin 9 on IC6c, goes to Q2 (the 50MHz preamplifier output) while the other input, pin 1 of IC6a, goes to the 500MHz prescaler. One of these two inputs is selected via switch S1a and passed to the output of the multiplexer, pin 6 of IC6b.

With switch S1a set to the 10MHz and 50MHz positions, pin 2 of IC6a is pulled low, disabling it and forcing its output, pin 3, high. IC6d inverts the low signal from S1a, setting pin 10 of IC6c high. IC6c is then enabled and acts as an inverter, passing the signal from Q2 to pin 5 of IC6b. Now since the other input of IC6b is high, the output of IC6b is just the signal from Q2.

When S1a is switched to the 500MHz position, IC6d is enabled and IC6c disabled so that the signal from the 500MHz prescaler is passed to the output of the multiplexer.

THE PRESCALER

The optional 500MHz prescaler circuit is quite straightforward. Diodes D3 and D4 clip the input signal as before, and this is then fed to an OM350 hybrid VHF preamplifier which offers about 18dB of gain. The output of the preamplifier and the power supply are combined on pin five of the OM350.

Power is applied to the OM350 via an RF choke and the output capacitively coupled to IC5, an 11C90 ECL decade divider. Pin 16 of this device is the clock input and pin 15 is an internal bias reference specifically intended for biasing an AC-coupled clock input.

Complementary ECL outputs are provided from the 11C90 as well as a separate TTL output which we have connected to the multiplexer IC6. A separate TTL earth is also provided on the 11C90 so that the crowbar currents of its TTL "totem pole" output stage are not fed back to the input.

So far we have a 50MHz and a 500MHz prescaler and a multiplexer to switch from one to the other. What we also require is a programmable divider to divide by one for signals up to 10MHz and divide by 10 for signals up to 50MHz and from the 500MHz prescaler. This could be done by simply switching a decade divider in or out but we decided to use an electronic switching circuit that avoids taking any signal lines to the range switch.

This is accomplished by using a standard 74196 decade divider which features four outputs (Q1, Q2, Q3 and Q4) as well as four parallel inputs (D1, D2. D3 and D4) which can be loaded into the counter using the load input, pin 1. To get the counter to divide by 10 the load input is switched high and the counter functions normally.

For frequencies below 10MHz switch S1b sets the load input of IC3 (pin one) to ground, which effectively disables the counter and forces the outputs of the counter to follow the parallel inputs. Since we have also connected the multiplexer output to the parallel input D3, corresponding to output Q3 of the counter, the input signal is just passed through as is – in other words it is divided by one.

Note that we have used the Q3 output of the counter rather than Q4 because, if you examine the normal BCD counting sequence, Q4 is low for counts zero to seven and high only for counts eight and nine. Since the 7216A has a minimum input pulse length (50ns high or low), the clock waveform must be as square as possible for it to reach its maximum specified frequency of 10MHz. The Q3 output is high for four consecutive counts and low for six, and thus has the advantage of a much squarer output.

View of the prototype fitted with the optional tilting bail. The 1MΩ input is used for the 0-10 and 0-50MHz ranges while the 75Ω input is used for the 500MHz range.

The electronic switching used in the multiplexer and the divider is slightly more complex than if the signals had been switched directly but it really simplifies construction in that wiring layout is non-critical – at least as far as the constructor is concerned!

One final point about the divider circuit: we have added a 470Ω pull up resistor on the output of IC3, pin 2. This is to raise the voltage level of a logic high from the TTL output to make it acceptable to the CMOS input of the 7216A. According to specifications, the 7216A requires a clock signal of 2.5Vp-p centred about 2V, ie, a high is 3.25V.

The power supply consists of an Arlec AL7VA/15 PCB mounting transformer which is full-wave rectified by diodes D5 and D6 and filtered by a 1000μF 16VW capacitor. This is then regulated down to 5V via an LM340T-5 three-terminal regulator. The 10μF tantalum capacitors at the input and output of the regulator provide decoupling and stability.

A regulated 12V supply is also provided for the OM350 preamplifier and the FET input stage by using a voltage doubler consisting of the 470μF and 220μF capacitors plus diodes D7 and D8 to generate around 18V. This is then regulated down to +12V via an LM340T-12 regulator.

CONSTRUCTION

Construction is simplified by having all of the components mounted on a main printed circuit board (PCB) labelled 81fm10a and measuring 160 x 110mm. The FND507 displays are mounted on a separate display board labelled 81fm10b and measuring 115 x 40mm. This butts against the main board and is soldered to it via edge connector strips on each board.

The first step in construction is to mount the links, resistors and capacitors on the main PCB. Use the component overlay diagram as a guide to component placement and pay particular attention to the orientation of the tantalum capacitors and diodes. Mount all of the ICs but use a 28-pin socket for the 7216A, which should be left out until the board has been completed.

The appearance of the OM350 bears no resemblance to the familiar DIP or TO-5 can IC package. Instead, it has five leads in line and has a small resin-coated body. It looks rather like a multi-lead miniature ceramic capacitor.

The RF choke forms the output load for the OM350. It is wound on a 13mm balun core with six turns of 22 B&S enamelled copper wire. Carefully scrape away the enamel insulation from the leads before soldering the choke into circuit.

If you elect to leave out the 500MHz range, then omit ICs 4 and 5, D3 and D4, the RF choke, and the four associated 0.1μF disc ceramic capacitors (the 0.1μF disc ceramic on pin 14 of IC6d should be left in circuit). Pin 1 of IC6a should be pulled high by connecting a wire link between the vacant pin 6 and pin 11 holes of IC5.

Mount the FND507 displays on the display board, soldering just two diagonally opposite pins on each display first. Now check to see that the displays are properly seated and aligned before soldering the remaining pins.

The display board and main board can now be soldered together by butting them together at 90 degrees with the tops of the edge counter strips on the display board just visible on the top (component) side of the main board. Solder two of the strips together first, then adjust the boards so that the displays are parallel to the main PCB. Now solder the remaining strips.

We mounted our unit in an attractive PacTec plastic case, Model CM-86-225, measuring 206 x 159 x 64mm. Before drilling the mounting holes it is necessary to fit the Scotchcal front panel. As supplied, the label will not be cut to size so score along the border with a sharp knife, then bend the aluminium back and forth to effect a clean break. Carefully apply the Scotchcal label to the plastic front panel, making sure that it is correctly positioned.

Note: Before fitting, the Scotchcal label should be given a coat of hard-setting lacquer, such as "Estapol", to prevent scratching.

Drill mounting holes for the BNC sockets and switches and file out the square cutouts for the LED display and slider switches. The board is mounted next using 19mm tapped brass spacers and positioned so that the displays just protrude through the front panel. We glued our slider switches into position with epoxy adhesive in preference to using countersunk screws beneath the Scotchcal.

To keep the unit running cool and thus minimise any variation in crystal frequency we recommend that ventilation holes be drilled. In our unit, we drilled a row of five 5mm holes in the bottom of the case, about 20mm from the front, and a second row of five holes along the top of the back panel to facilitate convection.

The LM340T5 5V regulator becomes quite hot during operation and should be fitted with a small TO-220 heatsink. Readers should note that the 11C90 IC also runs quite hot, while the 7216A counter IC gets warm. The transformer also runs slightly warm.

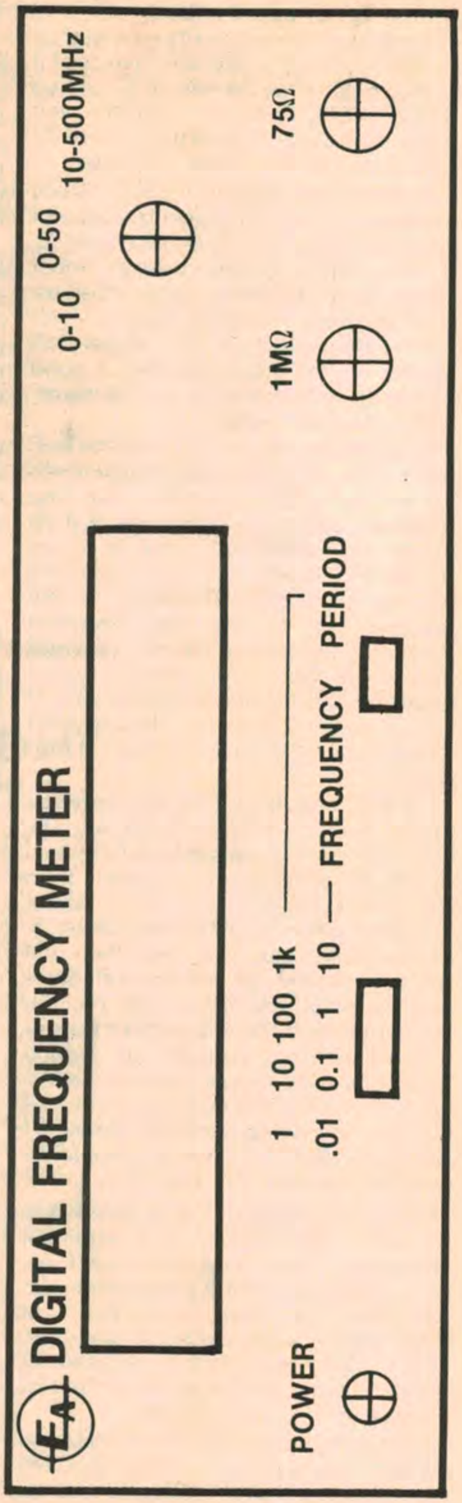
Complete the wiring to the board using the wiring diagram as a guide. Note that 75Ω shielded coax is required to connect the two input BNC sockets to the PCB inputs (see photograph). Rainbow cable can be used to make a neat connection to the slider switches and range switch, and for the four connections to the display board.

The mains cord enters through a hole in the rear panel and is clamped in position using a cord grip clamp. The active and neutral leads are terminated in a two-way mains terminal block, while the earth lead is terminated to a solder lug on the right-hand side of the rear panel (see wiring diagram).

Be sure to use mains-rated wire for connections to the power on/off switch.

A 0.1μF capacitor is used to earth the circuit to prevent interference from noise spikes. This capacitor is connected between the earth lug on the rear panel

FRONT PANEL ARTWORK



We estimate that the cost of parts for this project is approximately.

$110

for the 50MHz. Extra parts for the 500MHz version will add another $25. These price include sales tax.

and the earth lead to the 0-50MHz input preamplifier.

As you may have noticed from photographs of the unit, we installed a tilting bail so that the unit can be inclined for a better viewing angle. For readers who want to add this extra feature, we understand that the bails are available from Radio Despatch Service, 869 George St, Sydney 2000 [phone (02) 211 0816].

Recheck your wiring and component orientation and, satisfied that all is correct, switch the unit on and check the +5V and +12V supplies. If these are OK switch the unit off and insert the 7216A, taking the usual precautions against static damage.

When the unit is subsequently switched back on, the display should show four zeros with the gating time switch set to the 10s position, three in the 1s position, two in the 0.1s position and one in the .01s position. Don't worry if the display shows an occasional low random count. That's just due to electrical noise in the immediate environment getting into the sensitive input stages of the counter and is perfectly normal.

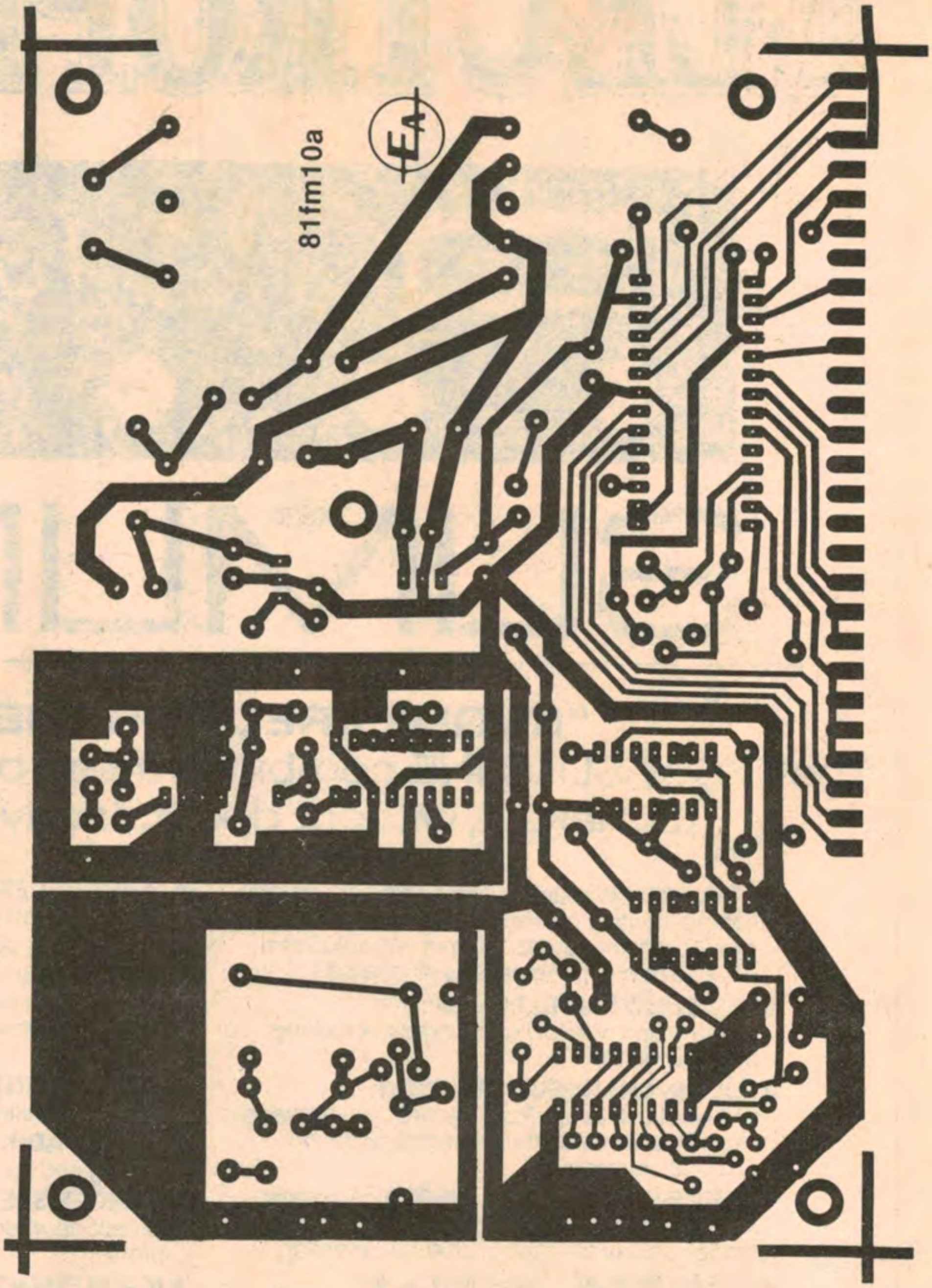
In fact we can use this noise to help check out the counter. As a quick test, insert a short length of tinned copper wire into the 1MΩ input and set the unit to 0-10MHz, frequency and 1s gating. The display should now show a high random reading and, by touching the wire, you may even get all seven digits to light. The other ranges can be checked in similar fashion, the actual number of digits displayed depending on the frequency of the noise.

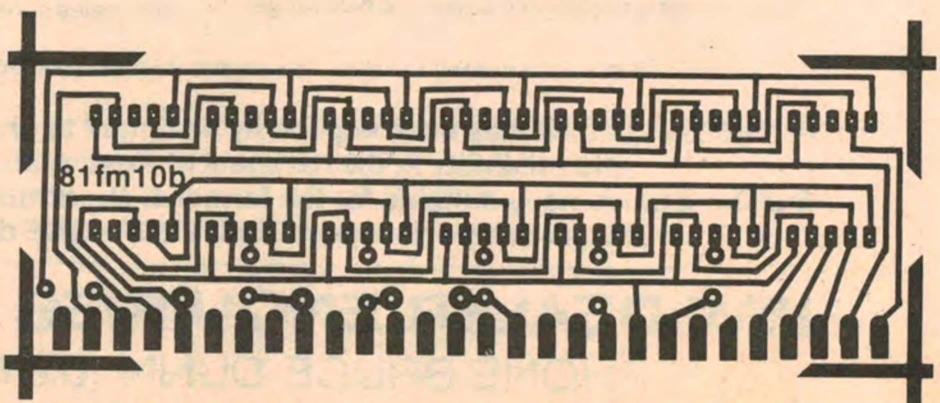
Don't forget to use the 75Ω input for the 10-500MHz range.

If you have access to a signal generator, it may be used to give the DFM a final checkout. Alternatively, you can use the meter to measure several known frequencies, eg, the output of a CB radio or amateur transceiver, or the 4.433619MHz PAL ident frequency found in colour TV receivers.

Accuracy of the frequency meter without calibration is typically .005% ±1 count, which is adequate for most applications. For those requiring greater accuracy, we shall detail an accurate calibration procedure next month. Also featured will be a useful troubleshooting procedure that you can follow in the event of difficulty.

NOTE: We are aware that at least one retailer will be offering a version of this design using the ICM7216B counter IC and common cathode displays. We regret that "Electronics Australia" will not be in a position to offer detailed advice to readers who encounter difficulties with this modified version.





Here are actual-size artworks for the two PCB patterns. Finished boards are available through the usual retail outlets.