PC-BASED TEST BENCH

In this series of articles we'll be building various PC-controlled test equipment—but first we need a universal interface card.

STEVE WOLFE

A PC IS THE PERFECT THING to use to accumulate, manipulate, plot, and store the results of an experiment. PC-based test equipment has an advantage over traditional instruments: since various instruments share the same PC, the money that would normally be spent duplicating the display, keyboard, etc., can be saved. That's the idea behind this series of articles. We'll build a number of PC-based test instruments, including a capacitance meter, a 100-MHz frequency counter, a logic IC tester/identifier, and an oscilloscope. We'll start this month with an interface card.

The search for the perfect PC interface begins with the serial port. Unfortunately, the serial port is too slow for transferring large quantities of data needed to control and monitor test equipment. Another possibility is the parallel port which can transfer 8 bits in 500 nanoseconds (best case). Unfortunately, the parallel port is not truly bidirectional. A couple of handshake lines can be used as data inputs, but that means converting fast parallel data into slower serial data. Also, several data lines would have to be sacrificed so that they could be used as address lines. Another possible solution would be to connect a circuit directly to the computer's expansion bus. That would be very fast and easy to program, but it would require giving up an expansion slot every time you added another device.

What's needed is a general-purpose, fully bidirectional parallel port that can select and drive different peripherals all connected to a single generic ribbon cable. That is all contained in the I1000 Data Interface that we'll build this month. The I1000 can address up to 256 peripheral devices, all connected in parallel, using 25-conductor ribbon cable. The I1000 is simple to program; an "out" or "write" command sends a byte, and an "in" or "read" command receives a byte.

I1000 operation

Each card in a PC has it's own address. That is necessary to ensure that information intended for a certain card is received only by that card, and to ensure that only one card can place data on the bus at a time. Typically, the I1000 is set to address 768 (hex 300)—an address that IBM left available for prototyping. The I1000 can be re-addressed as needed by changing an address DIP switch. As far as software goes, we'll use BASIC due to it's broad popularity, but almost any other language can be used.

Sending a byte

Refer to Fig. 1 for the following example. When the BASIC instruction, "OUT 768,85" is executed, the byte "85" (01010101) is sent to address "768" (where the I1000 resides). The PC expansion bus address lines A5–A9 are attached to the card-address block, along with the ADDRESS ENABLE (AEN) line, which indicates that the address data is valid, and the WRITE (WR) line, which indicates that an "out" was performed. If the AEN and WR lines are low (logic 0) and the address lines match the DIP switch settings, an 8-bit magnitude comparator in the card-address block changes state (goes low). That tells the I1000 that the CPU has selected it.

The PC's WRITE pulse, in conjunction with the ENABLE pulse from the card-address block, causes the address latch to store the address, and the data latch to store the PC bus data. At that point, the I1000 is finished using the expansion bus, and it places the data, address, and SEND pulse on the interface cable that is going to the peripheral. The SEND pulse is sent along as confirmation that the data and address information is valid. Approximately 750 nanoseconds later, the I1000 sends a 500-nanosecond peripheral WRITE pulse. By the time the WRITE pulse reaches the peripheral, the data, address, and SEND pulses have finished any ringing associated with parallel interfacing. Additionally, each of the signals mentioned are terminated and buffered on the I1000 and at the peripheral. That defeats any error and noise (reflection, bounce, and

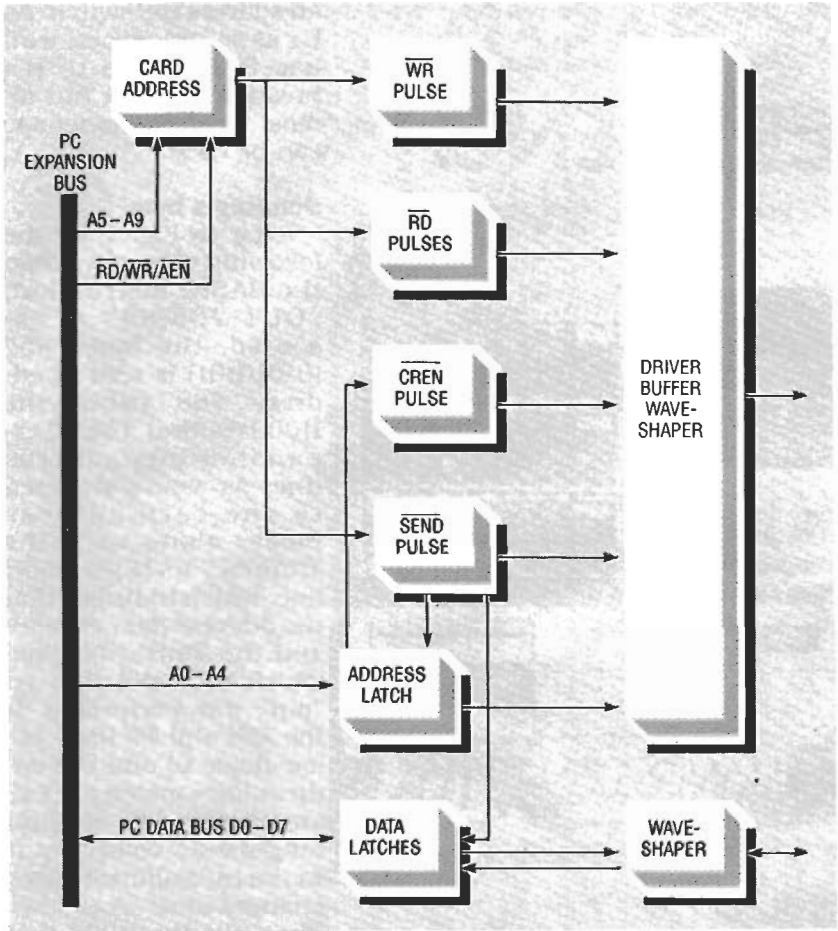


FIG. 1—I1000 BLOCK DIAGRAM. This interface will let your PC communicate with the test equipment we'll be working on in future articles.

crosstalk) problems commonly associated with parallel data transfer. The peripheral responds to the $\overline{\text{WRITE}}$ pulse by storing the data byte (D0–D7) within the location dictated by the address information (A0–A4) that it received.

Receiving a byte

For the following example, we will execute the line of BASIC: A=INP(768) : A=INP(768) : PRINT A. When the $\overline{\text{ADDRESS ENABLE}}$ ($\overline{\text{AEN}}$) and the PC's $\overline{\text{READ}}$ ($\overline{\text{RD}}$) lines are low, the card-address section once again goes low, and the send and address information is sent to the peripheral. A $\overline{\text{READ}}$ pulse is sent to the peripheral 500 nanoseconds later, which causes the peripheral to send the data back to the I1000. The data from the peripheral is stored in the I1000 250 nanoseconds later. The second input statement moves the data from the I1000 to the variable (A). Finally, the byte is displayed on the PC's monitor.

Control register enable

The I1000 has the ability to talk to 32 locations within 256 peripheral devices. That tremendous flexibility is accomplished through the use of the control register. When the I1000 is set to a base address of 768, it is actually active from 768 to 799, and covers 32 addressable bytes. If we say that the variable "bas" is equal to 768, then one I1000 can cover bas+0 (768) to bas+31 (799). Within the I1000, bas+31 has been decoded to a single line. In other words, when an "out" is sent to bas+31, the $\overline{\text{CREN}}$ line goes low.

When the $\overline{\text{CREN}}$ line goes low, any peripheral attached enters a comparator mode. While in that mode, each peripheral compares the information on the data bus with it's own hard-wired identification byte. If they match, that peripheral will attach itself to the data bus. In a peripheral where the bytes do not match, that peripheral will ignore or disconnect itself from the data bus. Once a peripheral has been called, it continues to be connected to the data bus until another bas+31 activates a different peripheral.

Suppose peripheral 1 is an A/D converter with a unit address of 0 and peripheral 2 is a capacitance meter with a unit address of 4. An "out bas+31,0" would select the A/D converter unit. The A/D would not actually do anything other than connect to the bus. After that, outs and ins to addresses between bas+0 (768) and bas+30 (798) would cause the A/D peripheral to perform it's job. An "out bas+31,4" at this point would remove the A/D converter from the cable and connect the capacitance meter. Again, outs and ins in the range bas+0 to bas+30 would control the instrument selected.

Finally, an "out bas+31,99" would disconnect both of the peripherals from the interface cable. That occurs because there is no device currently connected with a hard-wired identification byte of 99. The data bus is eight bits wide, so 256 (2^8) different peripherals can be addressed. Leaving bas+31 for addressing different units, 31 addresses (0–30) remain for accessing IC's within each unit. The total number of locations accessible by one I1000 is 7936 (256×31).

Detailed operation

Take a look at the timing diagrams in Figs. 2 and 3 and the schematic in Fig. 4. A 74LS688 8-bit magnitude comparator (IC1) compares DIP switch S1's settings to the address present at address lines A5–A9 (P1, pins A22–A26). It also checks to see that $\overline{\text{WR}}$ and $\overline{\text{AEN}}$ are low. When those conditions are met, IC1 pin 19 goes low, telling the I1000 that it has been selected by the CPU. Address lines A0–A4 (P1 pins A27–A31) are connected to IC10, a 74LS573 address latch. When pin 19 of IC1 goes low, it causes pin 6 of IC2-b (a 74LS86) to go high, latching the address information into IC10. When

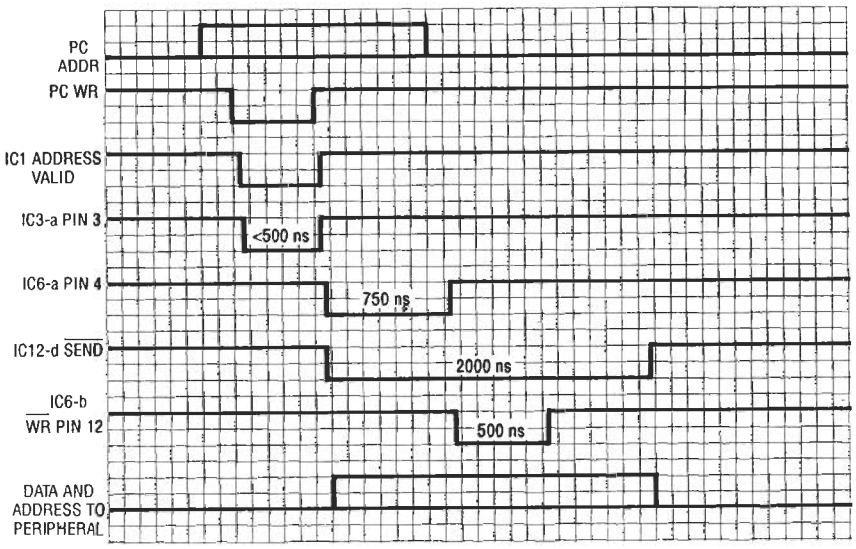


FIG. 2—I1000 WRITE, or "out" timing sequence.

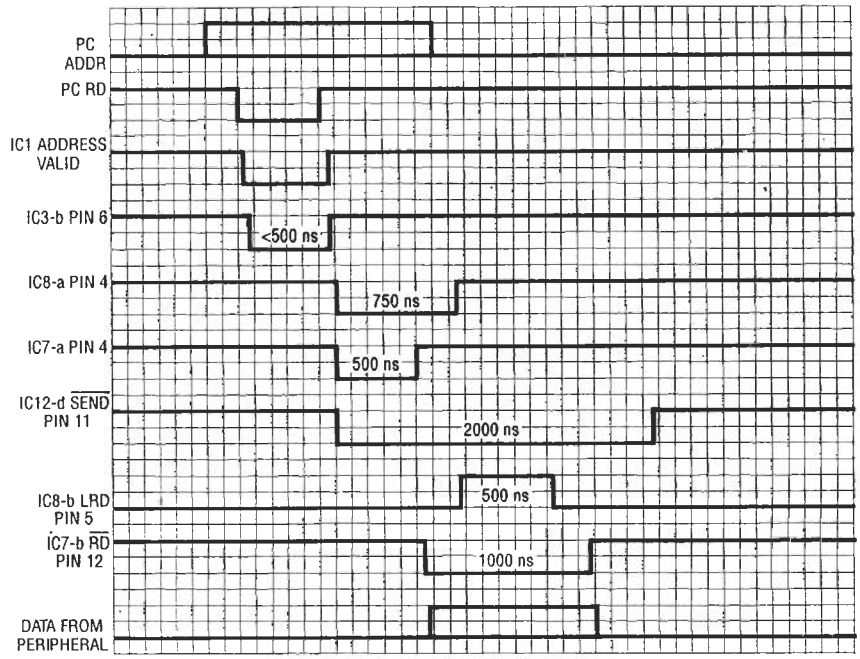


FIG. 3—I1000 READ, or "in" timing sequence.

the WR and EN pulses at the inputs of IC3-a (a 74LS32) go low, the output of IC3-a does the same. That causes the output of IC2-c to go high and moves D0–D7 data from the PC into data latch IC4.

Components IC6–IC9 (74HCT221's) are rising-edge triggered monostable multivibrators (one-shots) triggered by rising pulses. After approximately 500 nanoseconds, the WR and EN pulses return to their inactive high state and, as a result, the output of IC3-a returns to a high state. The rising edge produced by IC3-a triggers IC9-b and IC6-a. The WEND pulse, generated by IC9-a, when ANDed with the REND pulse, produces the SEND pulse. The SEND pulse tells the peripheral that the bus information is valid. The WEND and SEND pulses also enable IC10 and IC4, allowing A0–A4 and D0–D7 onto the peripheral buses.

At the same time IC9-b is triggered, IC6-a is triggered, producing a 750-nanosecond delay pulse. As IC6-a times out, it triggers IC6-b, which produces a 500-nanosecond WR pulse that is centered within the 2-μs SEND timing window. The WR and SEND pulses pass through IC13, a 74LS541 line driver/buffer. The WR pulse is reshaped by R9 and C30 to a waveform more suited to a long cable with inductive reactance. The SEND pulse is similarly reshaped by DIP resistor R10 (pins 6 and 11) and C27. During a WR operation, the data lines D0–D7 are conditioned by R11, R16, and C31–C38 on the way to the peripheral device. The address lines at the output of IC10 (A0–A4) are conditioned by R10 and C22–C26. Those address lines and the WEND pulse are applied to IC11, a 74LS138 demultiplexer. If WEND is low and the address is equal to the base address (768) plus thirty one (as discussed earlier), pin 7 of IC11 goes low producing the CREN pulse.

I1000 PARTS LIST

All resistors are ¼-watt, 1%, unless otherwise noted.
R1, R3, R5—1000 ohms, 5%
R2, R6—4320 ohms
R4—9090 ohms
R7, R8—20,000 ohms
R9—33 ohms
R10, R11—33 ohms, 16-pin DIP resistor
R12–R14—10,000 ohms, multiturn potentiometer
R15—4700 ohms, 10-pin SIP resistor
R16—2200 ohms, 10-pin SIP resistor
Capacitors
C1–C13—0.15 μF, 50 volts, monolythic or polystyrene
C14–C21—105 pF, 100 volts, dipped mica
C22–C29—1500 pF, 63 volts, polystyrene
C30—0.001 μF, 100 volts, ceramic disc
C31–C38—220 pF, 100 volts, ceramic disc
C39—100 μF, 25 volts, electrolytic
C40–C45—10 μF, 35 volts, electrolytic
Semiconductors
IC1—74LS688D 8-bit magnitude comparator
IC2—74LS86D quad 2-input XOR gate
IC3—74LS32D quad 2-input OR gate
IC4, IC5, IC10—74LS573D octal latch
IC6–IC9—74HCT221D dual one shot
IC11—74LS138D demultiplexer
IC12—74LS08D quad 2-input AND gate
IC13—74LS541D octal buffer
Other components
J1—Right-angle PC-mount female DB25 connector
S1—8-position DIP switch
Miscellaneous: I1000 PC board, PC mounting bracket and hardware with DB25 cutout, solder, etc.

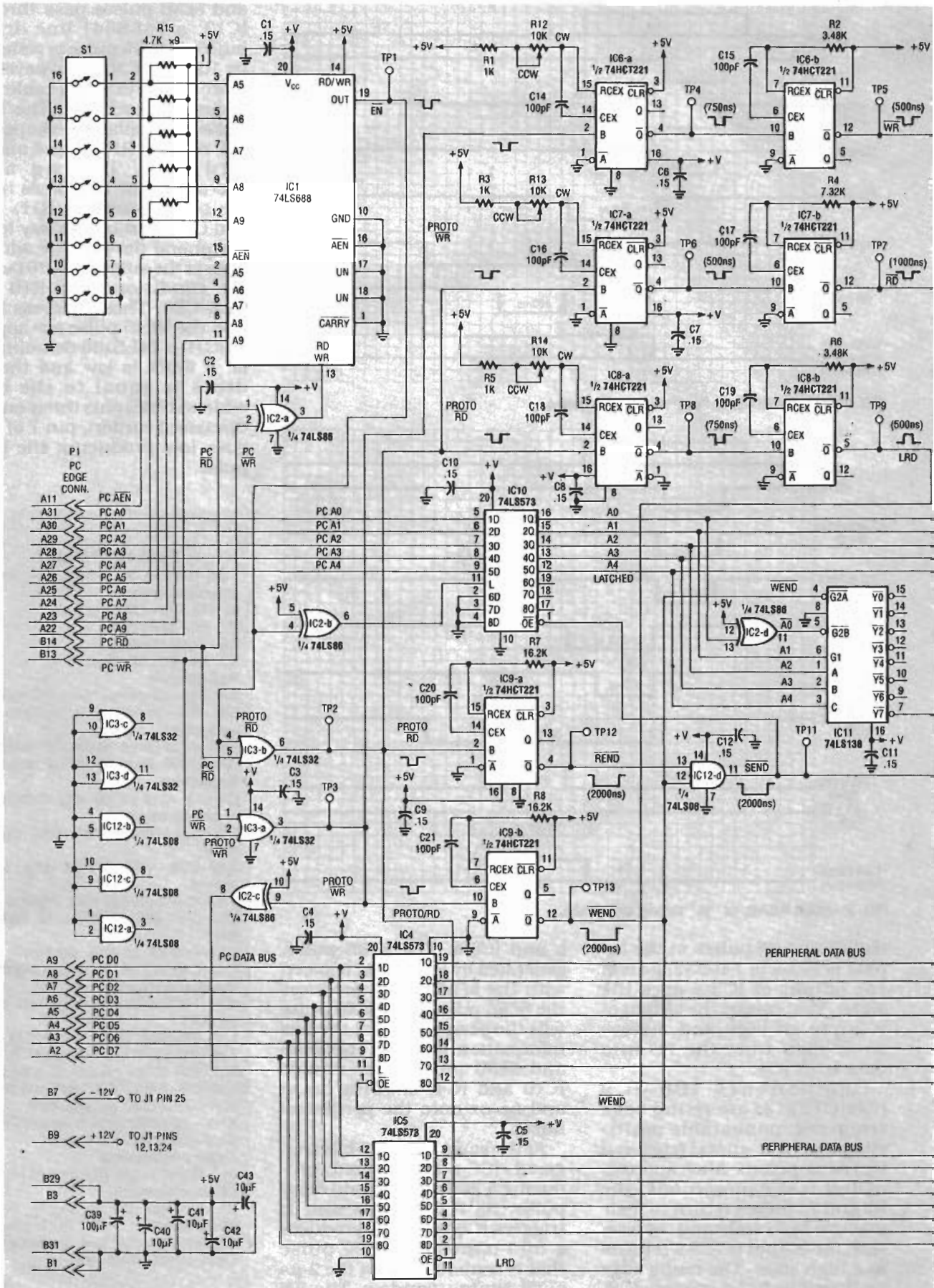
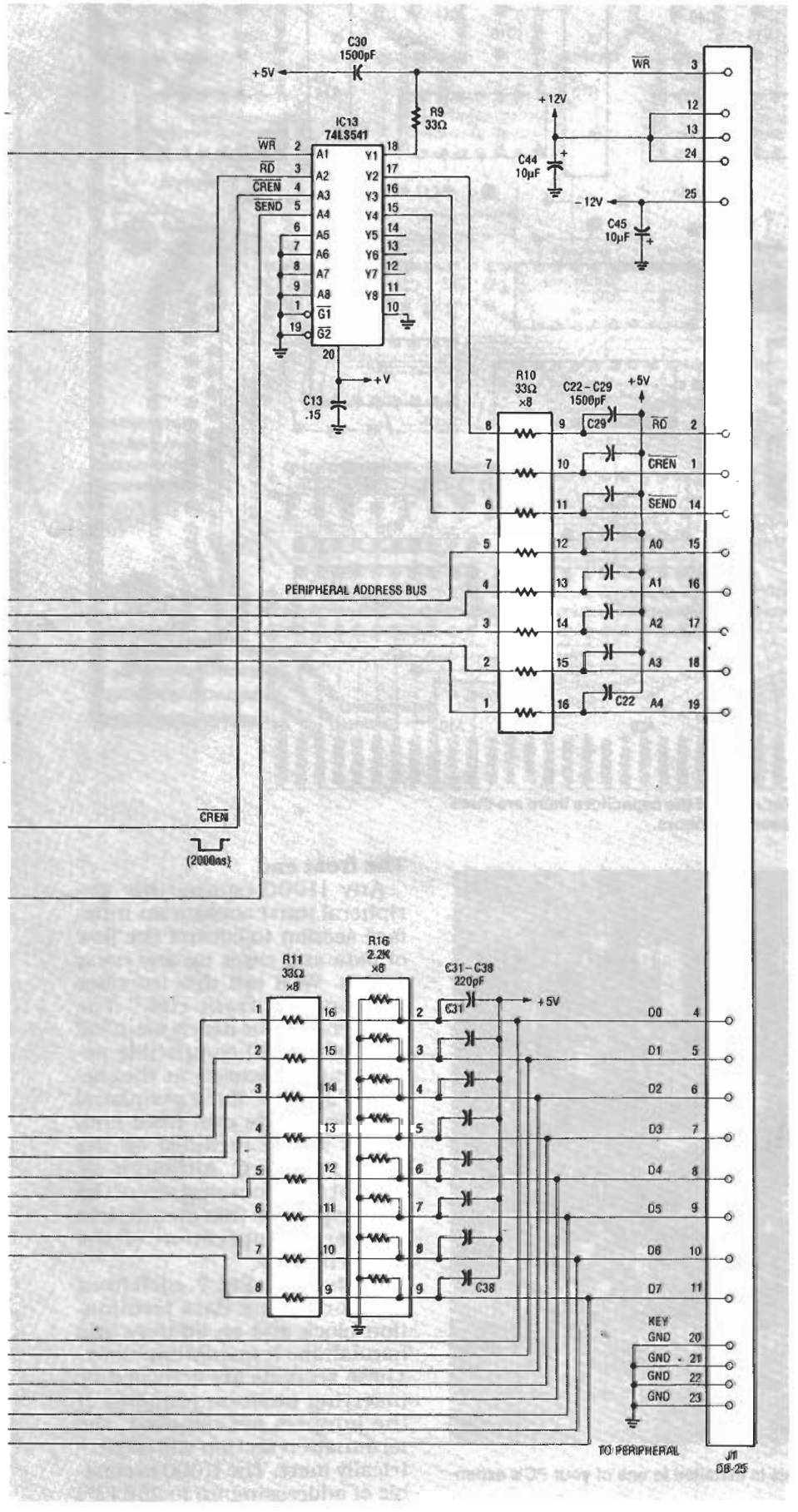


FIG. 4—I1000 SCHEMATIC. The I1000 can talk to 32 locations within 256 peripheral devices to provide tremendous flexibility.



Receiving a byte

When receiving a byte, IC1 operates the same as when it is sending except that the $\overline{RD}$ line goes low. The address data (A0–A4) is again stored in IC10. The $\overline{RD}$ and $\overline{EN}$ pulses go low, and as a result IC3-b transitions low. The PC then reads back the contents of IC5. (The information read back at this point is irrelevant, since information from the peripheral unit has not reached the I1000 yet.) As the $\overline{RD}$ and $\overline{EN}$ pulses end, a rising pulse edge occurs at IC3. That activates IC7-a, IC8-a, and IC9-a.

The $\overline{REND}$ pulse is produced by IC9-a, which, when it passes through IC12-d, becomes $\overline{SEND}$. A 500-nanosecond delay pulse is produced by IC7-a; as IC7-a times out, it triggers IC7-b, which produces a 1000-nanosecond $\overline{RD}$ pulse which is sent to the peripheral unit. (The $\overline{SEND}$ pulse and address information arrived at the peripheral 500 nanoseconds earlier.) Upon receiving the $\overline{RD}$ pulse, the peripheral sends the $\overline{D0–D7}$ data to the I1000 (IC8-a went active at the same time as IC7-a, and produced a delay pulse of 750 nanoseconds). As IC8-a times out, it triggers IC8-b to produce a 500-nanosecond latching pulse. The pulse controls the LATCH line of IC5 and stores the information sent by the peripheral during the (still active) 1000-nanosecond $\overline{RD}$ pulse. A second identical input statement will now cause IC3-b to go low. That again activates IC5 and returns valid data to the PC.

I1000 construction

To build the I1000 interface, you can either buy a PC board from the source mentioned in the Parts List or make one from the foil patterns we've provided. Install parts on the board as shown in Fig. 5. You will notice that for many of the capacitors, there are three holes on the board, with two of them electrically the same. Those two holes are for mounting capacitors of different sizes. Use the pair of holes that best fit the capacitors you use. Figure 6 shows a completed card.

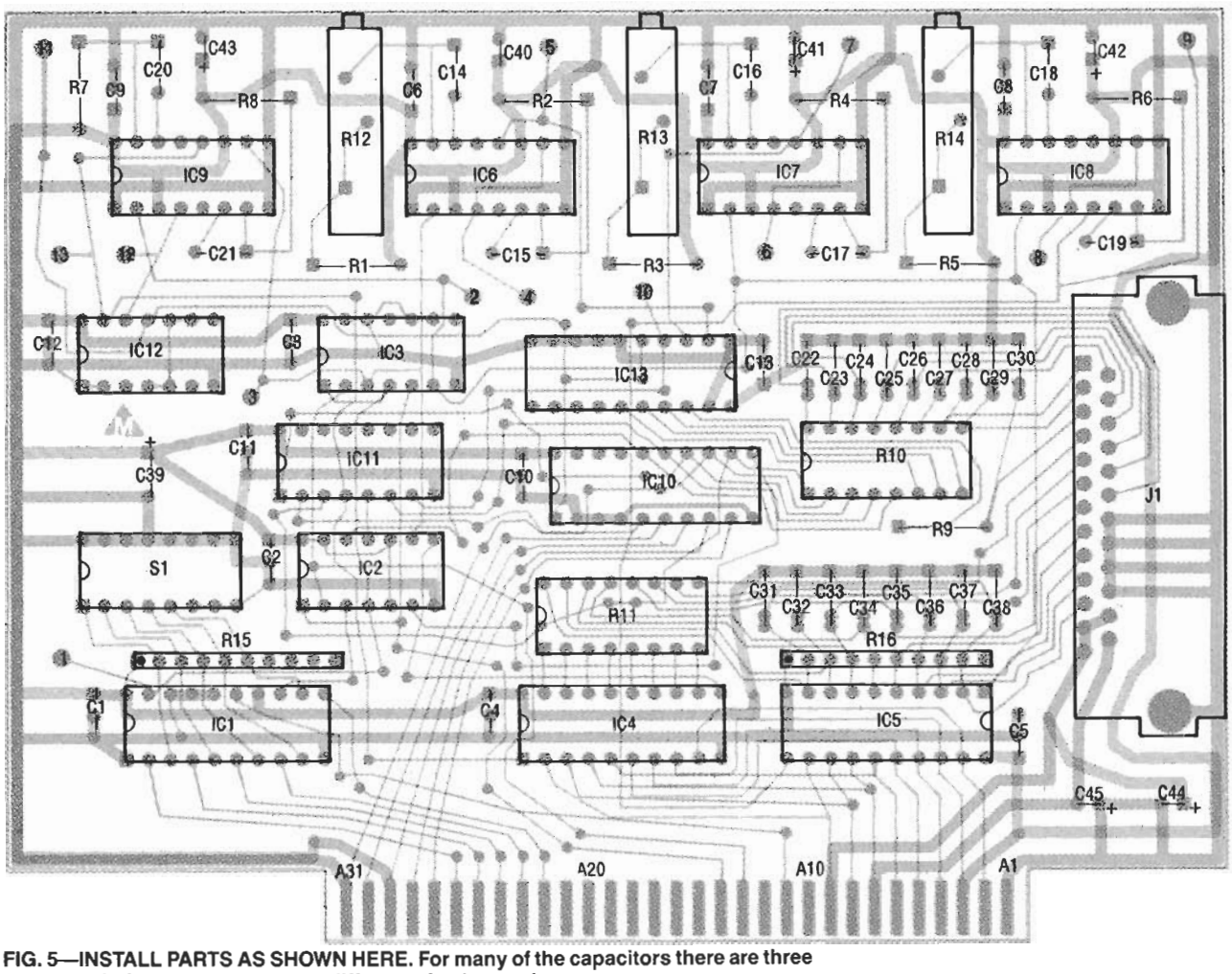


FIG. 5—INSTALL PARTS AS SHOWN HERE. For many of the capacitors there are three mounting holes to accommodate different-sized capacitors.

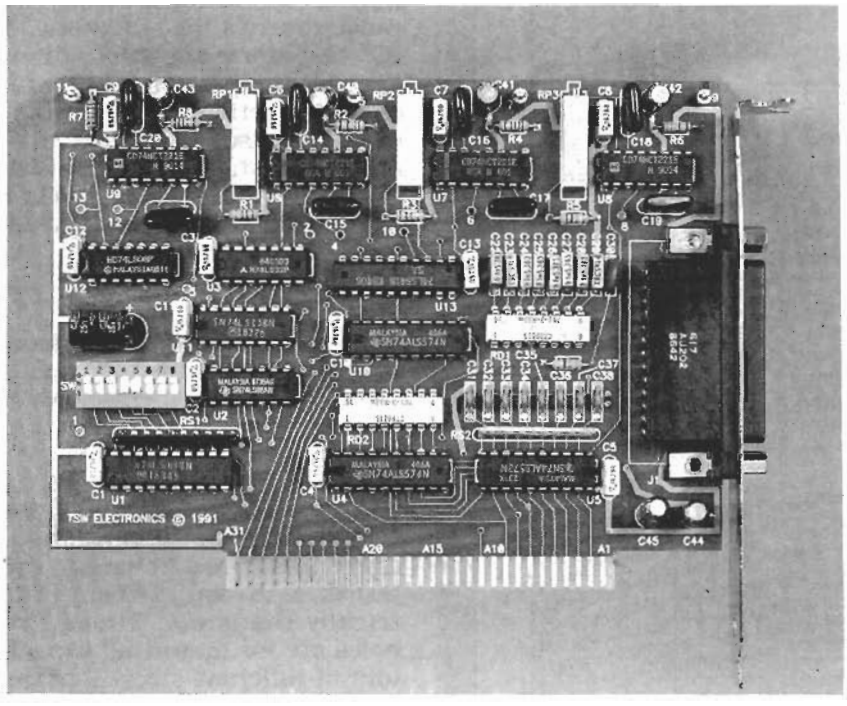


FIG. 6—COMPLETED INTERFACE CARD. This is installed in one of your PC's expansion slots.

The front end

Any I1000-compatible peripheral must contain an interface section to control the flow of data and clean up any noisy pulses. We'll call this interface section the "front end." The front end will be nearly identical for each I1000-compatible peripheral showcased in this series of articles. Each peripheral will contain its own front end, which will be included on the main PC board. Although we will not be discussing any of the PC peripherals this month, let's go over the operation of the front end now.

As shown in Fig. 7, each front end contains a data termination block and an address and handshake termination block. These sections are activated by inserting push-on jumpers. If the jumpers are removed, the termination section will be electrically inert. The I1000 is capable of addressing up to 256 (2^8)

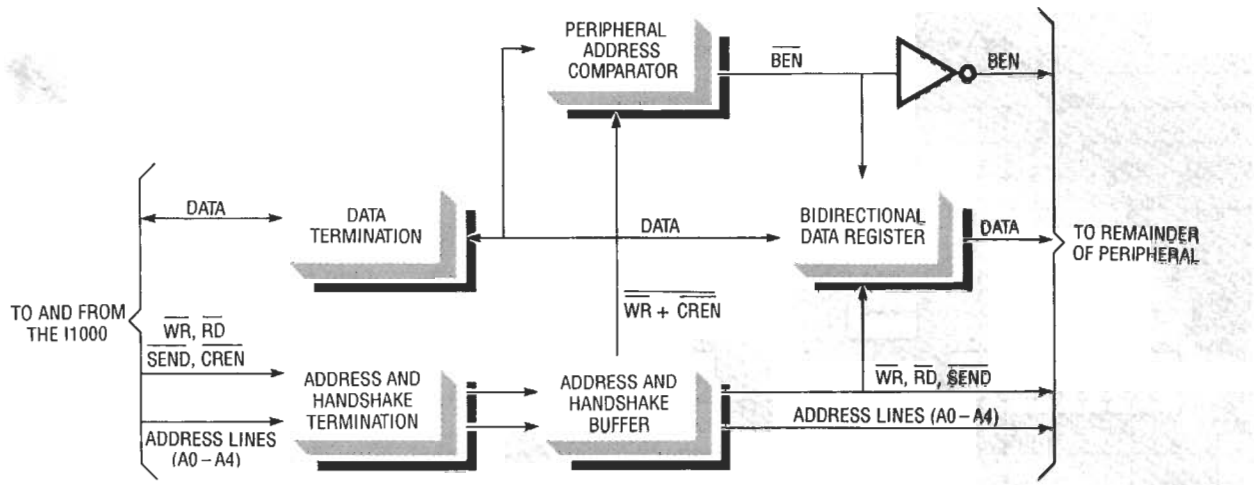
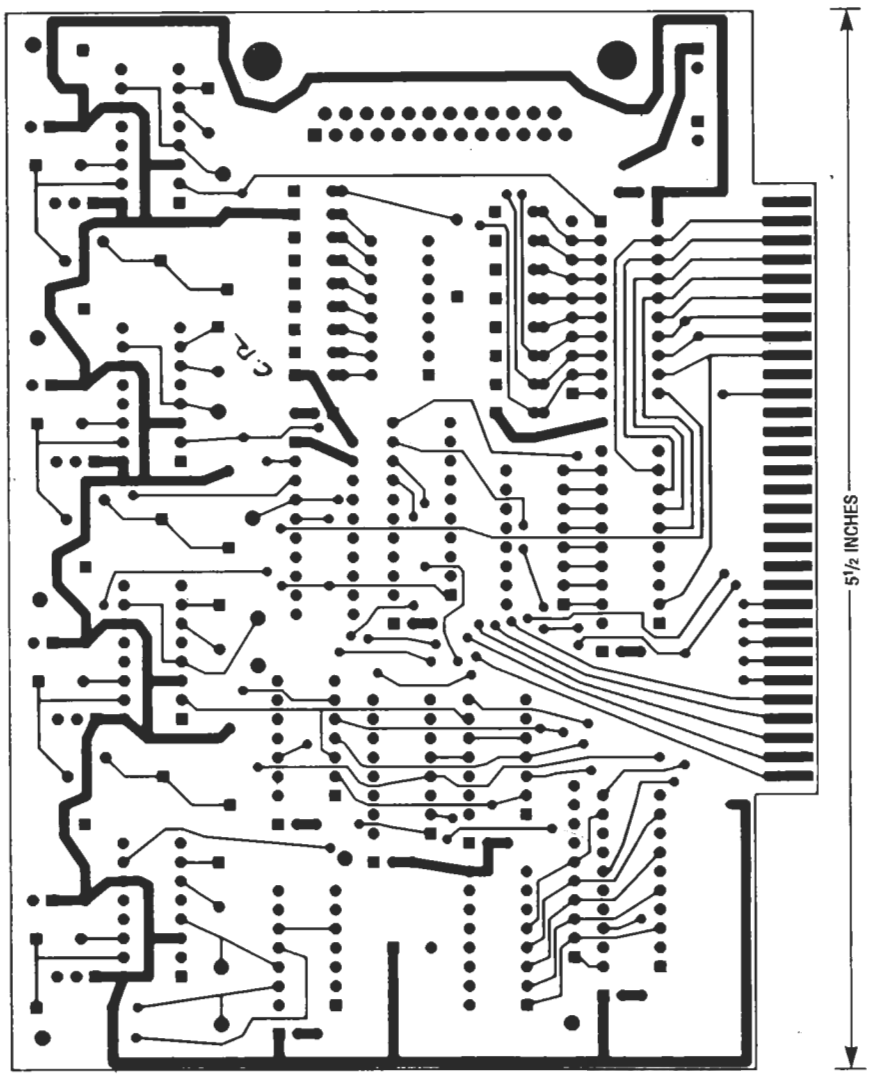


FIG. 7—ANY I1000-COMPATIBLE PERIPHERAL must contain an interface section to control the flow of data and clean up any noisy pulses. This front end will be nearly identical for all of the peripherals.



COMPONENT SIDE of the I1000 interface board.

peripherals. The DB-25 connectors on the rear of each peripheral are simply connected in parallel with one another. Termination of the data bus must occur at the most distant point on the bus and only at that point. If more than one peripheral were terminated at the same place, the termination impedance and its location would be altered, thus distorting the performance of the front ends.

After passing the active or inactive termination section, the data bus is attached to the Peripheral Address Comparator (PAC) and the Bidirectional Data Register (BDR). The PAC is responsible for activating a peripheral called by $\overline{\text{CREN}}$ as previously described. Each peripheral's PAC section contains its own unique address. If, during an active $\overline{\text{CREN}}$ pulse, the data on the bus matches the PAC address, the PAC section produces a low $\overline{\text{BOARD ENABLE}}$ handshake ($\overline{\text{BEN}}$). That signal and its complement (BEN) connect the remainder of the peripheral to the data bus and handshake lines ($\overline{\text{RD}}$, $\overline{\text{WR}}$, etc.).

The BDR is now capable of passing data to, and receiving data from, the main peripheral circuitry. The BDR is controlled by $\overline{\text{RD}}$, $\overline{\text{SEND}}$, and $\overline{\text{BEN}}$. Those lines tell the BDR the direction of data movement as well as the timing of that movement. After passing the active or inactive termination section, the address and handshake signals enter the address and handshake buffer. The signals are rounded by the termination sections to minimize crosstalk and other noise associated with fast rise and fall times. The address

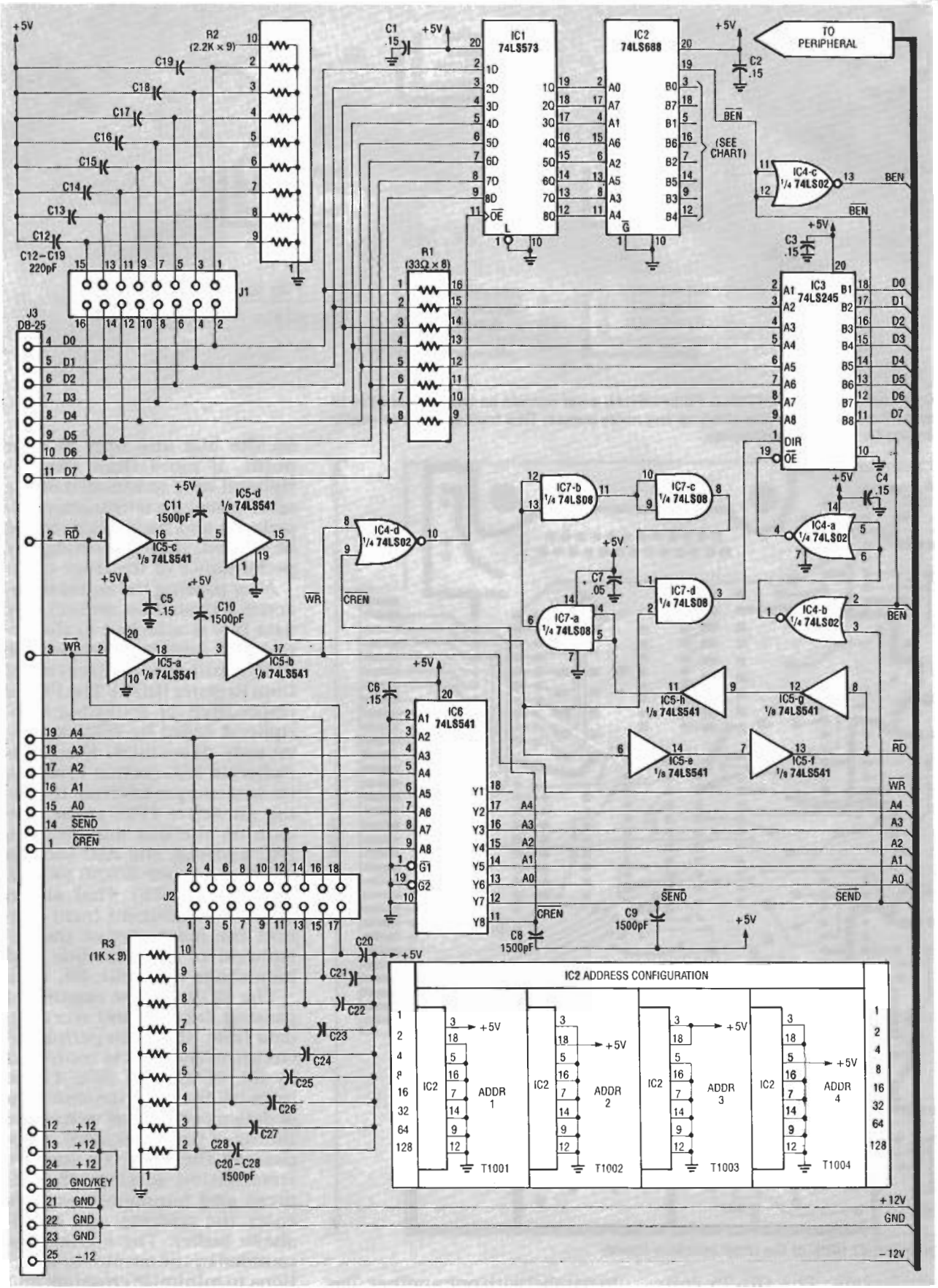
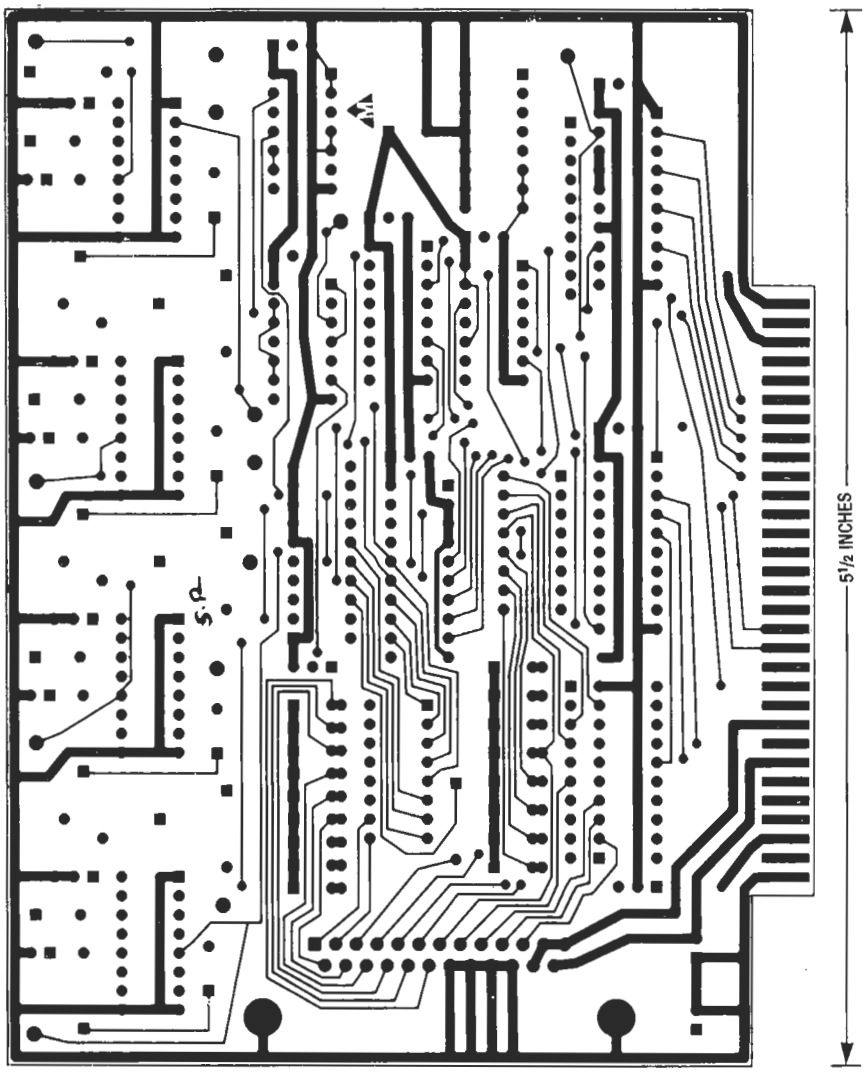


FIG. 8—FRONT-END SCHEMATIC. Each front end contains a data termination block and an address and handshake termination block that use push-on jumpers.



SOLDER SIDE of the I1000 interface board.

FRONT-END PARTS LIST

Resistors
R1—33 ohms, 16-pin DIP resistor
R2—2200 ohms, 10-pin SIP resistor
R3—1000 ohms, 10-pin SIP resistor

Capacitors
C1–C7—0.15 μF, 50 volts, monolythic or polystyrene
C8–C11, C20–C28—1500 pF, 63 volts, polystyrene
C12–C19—220 pF, 100 volts, ceramic disc

Semiconductors
IC1—74LS573D octal latch
IC2—74LS688D 8-bit magnitude comparator
IC3—74LS245D octal transceiver
IC4—74LS02D quad 2-input NOR gate
IC5, IC6—octal buffer
IC7—74LS08D quad 2-input AND gate

Other components
J1—16-pin male header
J2—18-pin male header
J3—Right-angle PC-mount male DB25 connector

Miscellaneous: 17 shorting blocks (for J1 and J2), solder, etc.

Note: The following items are available from TSW Electronics Corp., 2756 N. University Drive, Suite 168, Sunrise, FL 33322 (305) 748-3387:
- **I1000 kit—$65.00**
- **I1000 PC board only—$35.00**
- **I1000, assembled and tested—$77.00**
- **6-foot interface cable (DB-25-6)—$12.95**

Add $3.00 S&H for each order. Send check or money order only.

and handshake buffer restores the original fast rise and fall times of the signals.

Sending a byte

When describing software-related functions, we'll again use BASIC due its wide popularity and we'll assume the following initial conditions:

- The base address of the I1000 is 768 (hex 300).
- The front end of the peripheral has not been selected.
- The address of the peripheral is 4.

Refer to the front-end schematic in Fig. 8 and the following source code:

```
10 BAS = 768
20 OUT BAS + 31,4
30 OUT BAS + 2,170
```

Line 10 in that example assigns the address "768" to the variable "bas." Line 20 causes the $\overline{\text{SEND}}$ and $\overline{\text{CREN}}$ pulses at IC6 pins 8 and 9 to go low (refer to the timing diagrams in Figs. 2 and 3). If the shorting blocks have been installed at header J2, then the $\overline{\text{RD}}$, $\overline{\text{WR}}$, ADDRESS, $\overline{\text{SEND}}$, and $\overline{\text{CREN}}$ lines are all terminated. Line driver IC6 restores the original wave shape of any signals fed to it. The $\overline{\text{SEND}}$ and $\overline{\text{CREN}}$ pulses exit IC6 at pins 12 and 11. If the shorting blocks have been installed at J1, then the data lines D0–D7 are terminated. Either way, the data is fed to the input of latch IC1; IC3 is inactive at this time. At a time 750 nanoseconds later, the $\overline{\text{WR}}$ pulse enters IC5-a where it is reshaped. It is combined with the cleansed $\overline{\text{CREN}}$ pulse by IC4-d to produce the WR-CREN pulse.

The WR-CREN pulse latches the data (a binary 4) into IC1. The binary 4 appears at the output of IC1 and, subsequently, at the input of IC2, an 8-bit magnitude comparator. The magnitude comparator (IC2) compares the byte fed into it from IC1 with its hardwired address (see the IC2 address-configuration chart contained in Fig. 8). If the two bytes match, pin 19 of IC2 goes low ($\overline{\text{BEN}}$). $\overline{\text{BEN}}$ is then combined with $\overline{\text{SEND}}$ by IC4-b to produce the OUTPUT ENABLE control line signal ($\overline{\text{OE}}$) used by IC3, which transfers all the data to and from the peripheral.

When $\overline{\text{BEN}}$ is high, IC3 is inactive. The BEN line ($\overline{\text{BEN}}$'s compliment) is produced at IC4-c and enables or disables the chip-select section in the peripheral circuitry.

The $\overline{\text{BEN}}$ and BEN lines are the primary lines that determine whether a peripheral on the bus is active or dormant. The direction pin on IC3 (DIR) is controlled by the $\overline{\text{RD}}$ pulse. The $\overline{\text{RD}}$ pulse is high during a write op-

eration, allowing data to flow from the I1000 side of IC3 to the peripheral side of IC3.

Line 20 in the software example activates the peripheral by causing $\overline{BEN}$ to transition low. Line 30 in the software example will not affect IC1 or IC2. As explained earlier, only an "out" to bas+31 will activate $\overline{CREN}$. Line 30 will cause the following sequence of events: $\overline{SEND}$ will go low. The data (a decimal 170 in this case) will pass through IC3 to the peripheral circuitry. Address information (a decimal 2 in this case) will pass through IC6 to the peripheral circuitry. At a time 750 nanoseconds later, a 500-nanosecond $\overline{WR}$ pulse will pass through IC5 to the peripheral circuitry. The address is decoded by the chip-select circuit in the peripheral and the $\overline{WR}$ pulse is then routed to the addressed IC. Any "out" to an address between bas+0 and bas+30 will initiate the process commanded by line 30.

Termination

The termination sections are composed of J1, C12–C19, R2, J2, C20–C28, and R3. Those sections provide a termination impedance to ground as well as an R-C time constant. The termination impedance reduces the reflected signal caused by the inductive and resistive properties of the six-foot cable. The R-C time constant slows down the rise and fall times of the signal in the cable, thus reducing crosstalk. As stated earlier, the original transition times are subsequently restored.

Receiving a byte

As we describe how the front end end receives a byte from the I1000 interface, let's assume the following initial conditions:

- The base address of the I1000 is 768 (hex 300).
- The front end of the peripheral has been activated at an earlier time.

Next refer to the following source code:

```
40 A=INP(BAS+3)
50 A=INP(BAS+3)
60 PRINT A
```

Lines 10–30 are assumed to have been executed previously. Therefore, our theoretical peripheral has already been selected (activated). Line 40 produces a read function as described earlier. The $\overline{SEND}$ pulse goes low. The address lines (A0–A4) function as they did during the write function. At a time 500 nanoseconds later, a 1-μs $\overline{RD}$ pulse is received by the front end. It is reshaped by IC5-c and IC5-d. The $\overline{RD}$ pulse passes through IC7-d to IC3 pin 1. The peripheral side of IC3 becomes an octal input while the I1000 side of IC3 becomes an octal output.

The $\overline{RD}$ pulse arrives at the read chip-select section of the peripheral circuitry. The $\overline{RD}$ pulse, in conjunction with the address lines, cause the target IC to place its byte onto the bus. The transmitted byte passes through IC3 to the I1000 where it is latched. A data bus directional delay (DBDD) is provided by IC5-e–IC5-h in combination with IC7-a–IC7-d.

The DBDD provides a delay after the read cycle has finished before returning IC3 to its normal "output" configuration. That prevents IC3's peripheral side from going into its low-impedance state before the IC that was just read is able to de-activate. Line 50 causes the byte latched in the I1000 to be sent to the PC where it is stored under the variable "A." Line 60 prints the value contained in variable "A" on the screen.

As mentioned before, there's no separate front end PC board; each peripheral contains its own front end. Next month you'll see the front-end parts installed on the first peripheral board we'll work on: the T1001. That peripheral contains a 100-MHz frequency counter for digital signals, a period event meter, and a capacitance meter covering 1 picofarad to 10,000 microfarads. Other PC-based test instruments that we will build in future articles, include a logic-IC tester/identifier, and an A/D-D/A peripheral that can also be used as a low-frequency 8-channel digital storage oscilloscope. **R-E**

PC-BASED TEST BENCH

The first I1000 peripheral that we're going to build, the T1001, contains a frequency counter, an event/period meter, and a capacitance meter.

STEVE WOLFE

THIS MONTH WE CONTINUE our PC-based test equipment series by completing the first of several that are compatible with the I1000 interface we built last month. We also went over the Front-End circuitry that must be contained in each I1000 peripheral. This first peripheral, the T1001, contains a 100-MHz digital frequency counter, an event/period meter, and a precision capacitance meter accurate from 1 pF to 10,000 µF.

Capacitance measurement

The Circuit Control Latch section (CCL) is made up of 16 control lines that are individually routed to every block depicted in Fig. 1. The purpose of the CCL section is to enable, disable, reset, start, and stop the major processes of the T1001. The Capacitor Pulse section, when started by the CCL section, produces a negative-going pulse whose period is proportional to the capacitor under test.

The pulse produced in the Capacitor Pulse section enables and disables the 60-MHz clock. To determine the period of the pulse, the output of the clock is connected to the Cap/Event section which contains the least-significant eight bits (byte 1) of a 32-bit digital counter, as well as a latch used to read those eight bits. The Counter section provides the remaining 24 counter bits (bytes 2, 3, and 4) as well as three more 8-bit latches that are used to read the count back into the computer.

The complete sequence is as follows: Control data is sent to the address of the CCL. The Chip-Select (CS) section enables the CCL to store the control data. The control data disables the Frequency, Event, and Timebase sections, and resets the counter and Capacitor Pulse sections. Next, the CCL is sent a byte that causes a one-shot to fire in the Capacitor Pulse section. The resultant pulse enables the clock, which enables the counters. When the pulse has ended, the final counter values are read back into the computer. The four counter bytes are then combined into a single decimal value. The resultant value is proportional to the capacitance of the component under test.

Event/period measurement

Event or period measurement uses most of the same circuitry as the capacitance meter. In this case, the CCL is programmed to deactivate the Capacitor Pulse section and to activate the Event-Pulse section. The Event Pulse section contains a CCL-controlled inverter/buffer. The 60-MHz clock is enabled and disabled by a negative-going pulse. The inverter/buffer ensures that a pulse of any polarity fed into the Event Pulse section will be negative-going upon reaching the Clock section. That allows for measurement of either negative-going or positive-going pulses. As with capacitance measurement, the counters are clocked at a 60-MHz rate for the duration of the event pulse, and are then stopped. The counter bytes are read back into the computer and combined into a single decimal value. The resultant period in seconds is equal to the final count divided by 60 MHz.

Frequency measurement

For frequency measurement, the CCL is first instructed to disable the Capacitor Pulse and Event Pulse sections, reset all the counters, and select one of eight available timebases, which are derived from the 60-MHz clock. Next, a timing period begins, and the output of the Timebase section goes low. That allows the Frequency Input section to begin counting the frequency that is being measured. The first byte of the input frequency ripple carries into the Counter section (bytes 2, 3, and 4). When the timebase period ends, the output of the timebase section returns to a high condition, disabling the Frequency Input section. The final count bytes are then read back and are combined into a single decimal value. The resultant frequency is

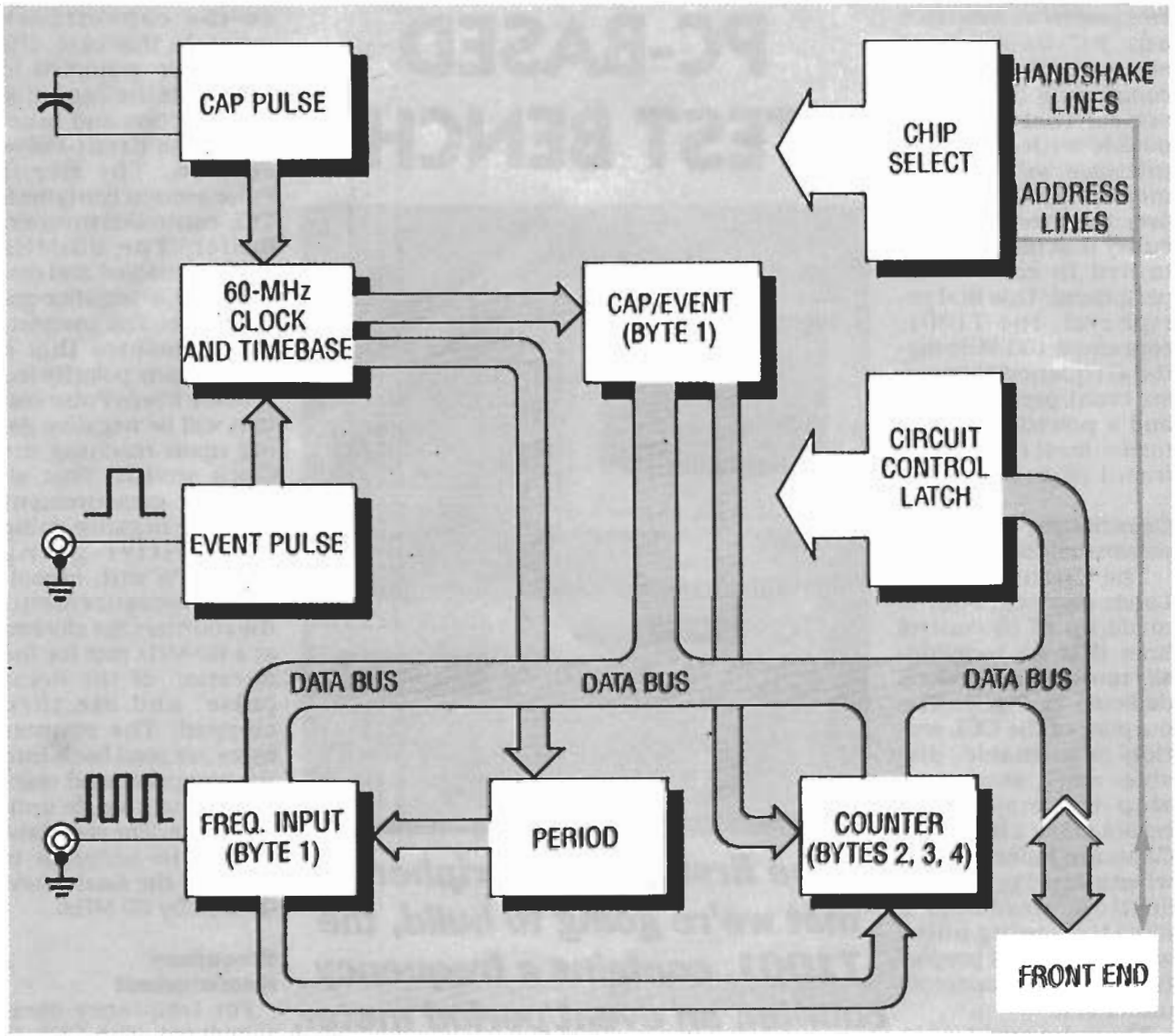


FIG. 1—T1001 BLOCK DIAGRAM. This peripheral contains a 100-MHz digital frequency counter, an event/period meter, and a precision capacitance meter.

equal to the final count divided by the timebase period in seconds.

Controlling the T1001

The first step in controlling any I1000 peripheral is to establish a base address and select the desired peripheral. The first bit of code will be:

bas = 768 : out bas + 31,1.

768 (hex 300) is the factory-preset base address of the I1000. Next we have an out to bas + 31. Recall that address bas + 31 is reserved for peripheral selection. The T1001 has a unit or peripheral address of "1." Consequently, if you send an out to bas + 31 with a data byte of "1," the T1001 will be readied for full I/O operation.

Take a look at the T1001 schematic in Fig. 2. (Note that the Front End circuitry is absent—you can find that, and a description of it, in the June 1992 issue.) A 74HCT138 3-to-8 line decoder (IC21) produces the read function chip selects within the T1001; it decodes three binary lines and produces a low on one of eight output lines. The low remains active as long as the handshake lines remain active. The handshake lines that come from the Front End are $\overline{\text{SEND}}$, $\overline{\text{RD}}$, and BEN. The address information present at pins 1–3 of IC21 corresponds to A0–A2 (A3 AND A4 are not used by the T1001).

The BEN pulse is high as a result of selecting the T1001. Executing "a = inp(bas + 3)" will cause SEND and A2 lines to go low, and A0 and A1 to go high. After 500 nanoseconds, the read pulse ($\overline{\text{RD}}$) will go low, activating IC21 pin 12 for the duration of the $\overline{\text{RD}}$ pulse (1 μs). If BEN were low, IC21 would not respond to read pulses. BEN is low in every peripheral except the one addressed with the bas + 31 function. The +0 through +4 designator on the outputs of IC21 correspond to bas + 0 through bas + 4 in the software. Using that notation, it is easy to visualize the software's effect on the hardware.

A byte latched into IC9 can be retrieved using the following:

a = inp(bas + 0):a = inp(bas + 0)

A read to bas + 0 will cause IC21

pin 15 to go low, which in turn brings IC9 pin 1 low. That causes IC9 to go active and place its data onto the bus. Similarly, a read to bas+1 will bring data held within IC19 onto the data bus. Reads issued to bas+2, +3, +4, and +7 retrieve bytes from IC27, IC28, IC30, and IC25, respectively. Another 74HCT138, IC22, produces the write function chip selects within the T1001. It functions in much the same way as IC21 except that it responds to the write pulse ($\overline{WR}$) instead of the read ($\overline{RD}$) pulse.

An "OUT bas+0,170" would cause IC22 pin 15 to go low and subsequently IC20 pin 8 to go high; IC20 pin 8 controls the latch input of IC23 pin 11. You may have noticed that chip-select read-function outputs are active low, while write function outputs are inverted, or active high. That's because the 74HCT573 latches need a low on pin 1 to output their byte, and a high on pin 11 to store a byte. Components IC23 and IC24 are used to clear, start, and stop all of the processes of the T1001. The labels on the output side of IC23 and IC24 match labels at the IC being controlled.

T1001 PARTS LIST

Resistors
R1—200,000 ohms, ¼-watt, 1%
R2—5110 ohms, ¼-watt, 1%
R3—2200 ohms, ¼-watt, 5%
R4—5600 ohms, ¼-watt, 5%

Capacitors
C1, C2, C7, C8, C10, C16, C17, C34, C41—10 µF, 35 volts, electrolytic
C3, C5, C6, C12–C15, C18, C20–C30—0.15 µF, 50 volts, monolythic
C4, C9, C11, C19, C31, C35, C36, C38, C39—not used
C32—105 pF, 100 volts, dipped mica
C33, C37, C40—100 µF, 25 volts, electrolytic

Semiconductors
IC1—74LS123D dual one-shot
IC2—74HCT86D quad 2-input XOR gate
IC3, IC11—74HCT32D quad 2-input OR gate
IC4—74HCT20D dual 4-input NAND gate
IC5—74HCT74D dual D flip-flop
IC6, IC16—74F86D quad 2-input XOR gate
IC7, IC10, IC17—74ACT74D dual D flip-flop
IC8, IC12–IC14, IC18, IC26, IC29—74HCT4040D 12-stage binary counter
IC9, IC19, IC23–IC25, IC27, IC28, IC30—74HCT573D octal latch
IC15—74HCT151D 8-channel multiplexer
IC20—74HCT04D hex inverter
IC21, IC22—74HCT138D 3-to-8 line decoder
IC31–IC33—LM340T 5-volt regulator, TO-220 case
IC34—LM340K 5-volt regulator, TO-3 case
D1—1N4148 diode

Other components
OSC1—60-MHz crystal oscillator
J1—panel-mount BNC connector
J2, J4—red binding post
J3—black binding post
J5–J7—spring jacks or other type of connector, see text
Miscellaneous: project case, PC board, software, three TO-220 heatsinks, one TO-3 heatsink, sheilded cable, stranded jumper wire, hardware, ribbon cable, solder, etc.

Powering the T1001

Peripherals attached to the I1000 are powered by the +12-volt DC power line of the host PC. The +12-volts DC is filtered and regulated to +5-volts DC within the peripheral. In the T1001, the +12-volts DC is converted into four different +5-volt supply lines. There are four different supply lines because the 60-MHz master oscillator produces energy that can radiate to other parts of the circuit. (In an early T1001 prototype, the 60-MHz clock radiated enough energy to completely disable the frequency-counter section.) Giving each high-frequency section its own power supply eliminates such problems.

Measuring capacitance

To measure capacitance, you must first disable any systems not involved in capacitance measurement. Therefore, IC23 and IC24 are used to disable IC17, IC18, IC10, IC2-d, and IC5-b. That disables the Frequency Counter and Event sections. Let's assume that you are going to measure a small capacitor (less than 1 µF). Now IC23 and IC24 clear IC1-a, IC1-b, IC7-a, IC7-b, IC8, IC26, and IC29, and another byte from IC23 and IC24 releases those chips from their reset modes.

You are now ready to start IC1-a by transitioning its start line at pin 2; that causes IC1-a pin 4 to go low and IC4-b pin 8 then goes high. Flip-flop IC7-a—a 74F74 high-speed flip-flop set up as a divide-by-two—contains the least-significant bit of the 32-bit counter. When IC6-d receives a low on pin 13, IC7-a is disabled; when IC6-d receives a high on pin 13, IC7-a is enabled. Therefore, during the time that IC1-a is producing a negative pulse, IC7-a is counting at a 60-MHz rate.

The rest of the 32-bit counter section is made up of IC7-b, IC8, IC26, and IC29. Each section ripple-carries to the next. Once the one-shot pulse has begun, IC25 continually reads back IC6 pin 13 to determine if the pulse has finished. When IC6 pin 13 is found to be low, the one-shot has finished and the contents of the counters are read back from IC9, IC27, IC28, and IC30. The four bytes are recombined by the software to yield one decimal number proportional to the capacitance.

One-shot circuits cannot produce pulses that increase with capacitance in a 1:1, or linear fashion. In fact, the graph can be a curve resembling the natural log of 2. To achieve better than one percent accuracy, matrices and determinants are used in the software to overlay a correction curve and thus cancel any nonlinear characteristic. That is achieved by plugging capacitors with known values into the capacitor checker during a calibration process, allowing the checker to learn what capacitance equals what count. Therefore, the T1001 capacitance meter is accurate from 1 picofarad to 10,000 microfarads. For optimal performance, the calibration process should be repeated every six to eight months.

Measuring an event

Period measurement is accomplished with most of the circuitry used for capacitance

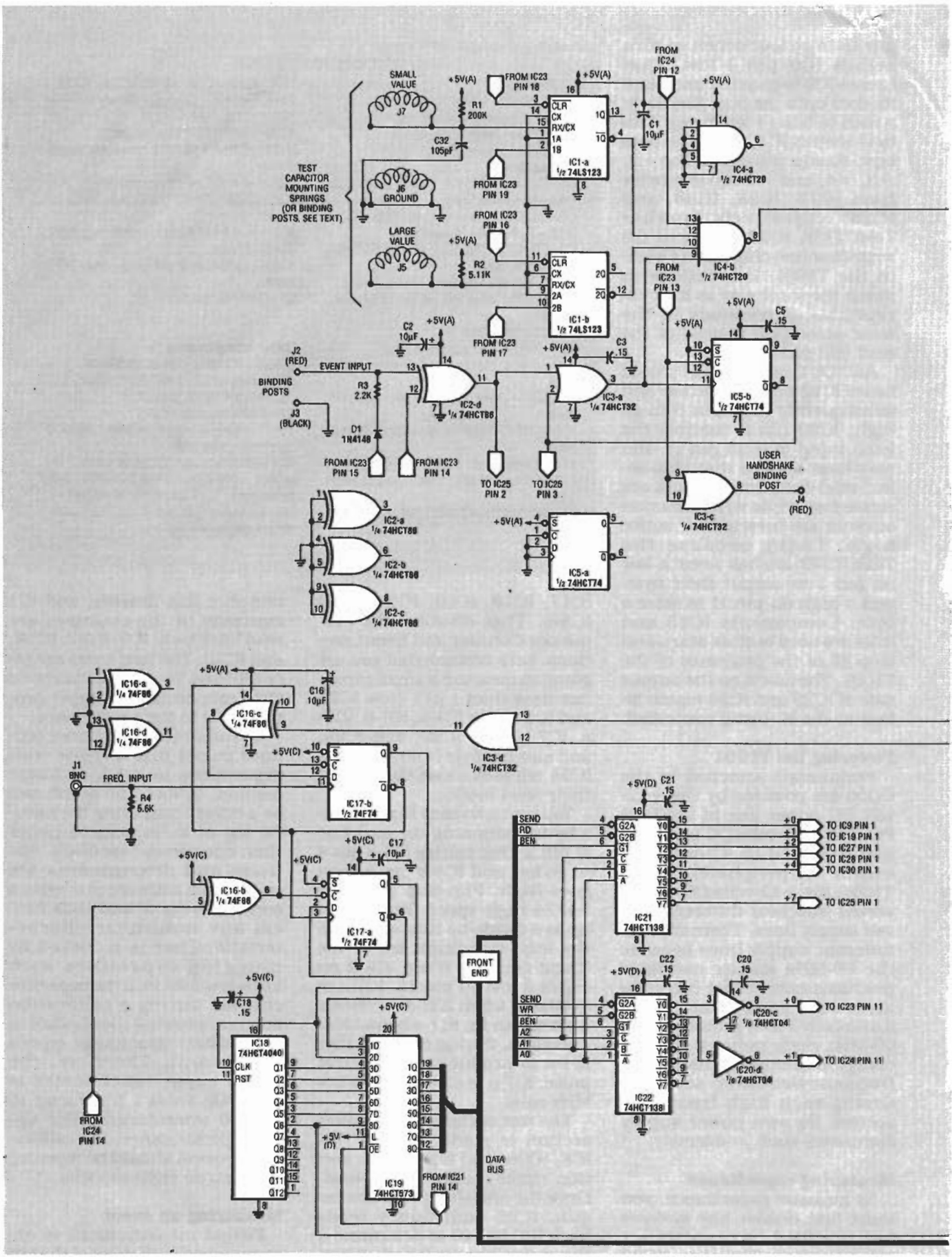
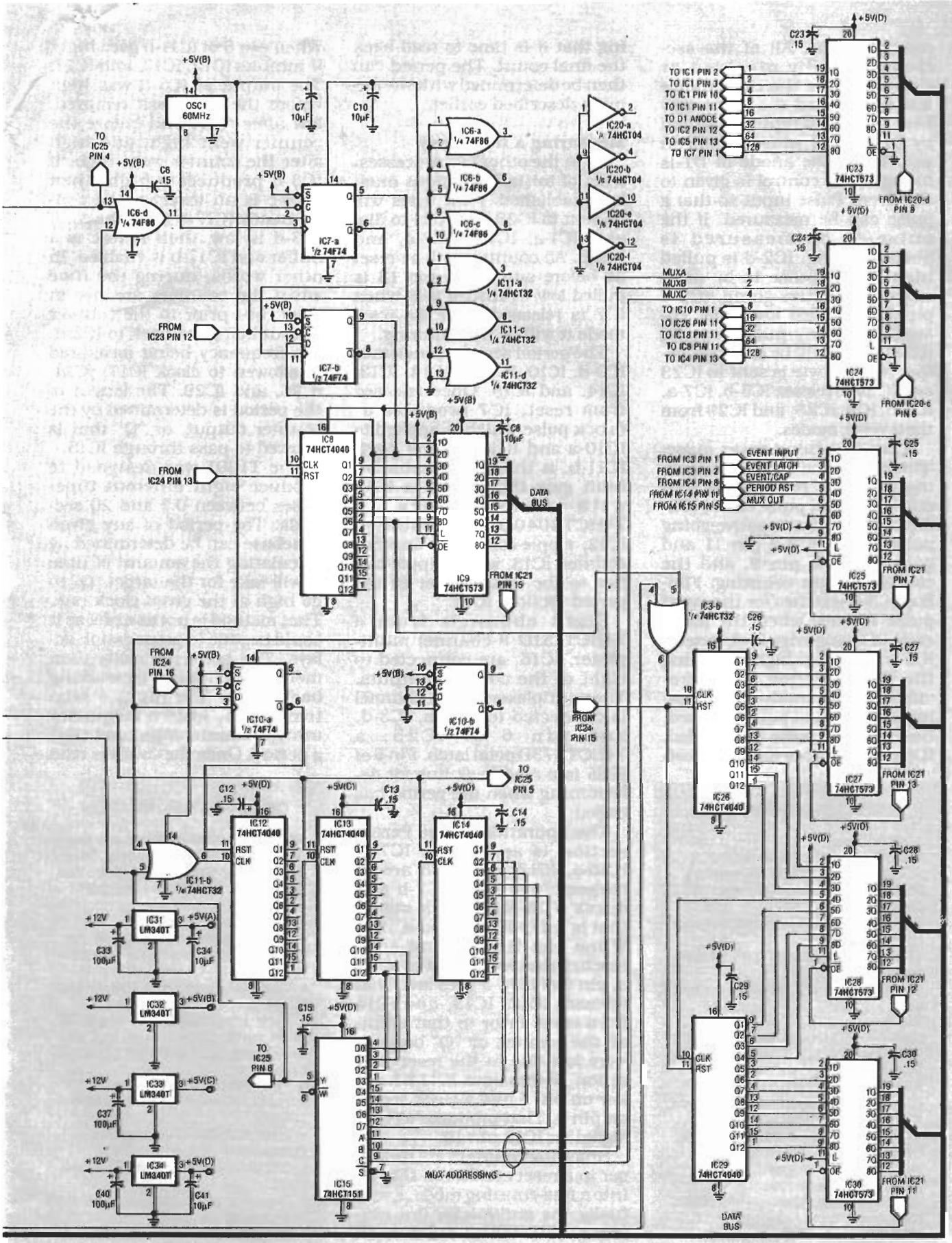


FIG. 2—T1001 SCHEMATIC. A 3-to-8 line decoder (IC21) produces the read function chip selects within the T1001 by decoding three binary lines and producing a low on one of eight output lines.


OSC1
60MHz
IC6-a
1/4 74F86
IC6-b
1/4 74F86
IC6-c
1/4 74F86
IC6-d
1/4 74F86
IC7-a
1/2 74F74
IC7-b
1/2 74F74
IC11-a
1/4 74HCT32
IC11-c
1/4 74HCT32
IC11-d
1/4 74HCT32
IC11-b
1/4 74HCT32
IC20-a
1/6 74HCT04
IC20-b
1/6 74HCT04
IC20-c
1/6 74HCT04
IC20-d
1/6 74HCT04
IC8
74HCT4040
IC9
74HCT573
IC10-a
1/2 74F74
IC10-b
1/2 74F74
IC12
74HCT4040
IC13
74HCT4040
IC14
74HCT4040
IC15
74HCT151
IC23
74HCT573
IC24
74HCT573
IC25
74HCT573
IC26
74HCT4040
IC27
74HCT573
IC28
74HCT573
IC29
74HCT4040
IC30
74HCT573
IC31
LM340T
IC32
LM340T
IC33
LM340T
IC34
LM340T
+5V(B)
+5V(D)
+5V(A)
+5V(B1)
+5V(C)
+12V
DATA BUS
MUX ADDRESSING
EVENT INPUT
EVENT LATCH
EVENT/CAP
PERIOD RST
MUX OUT
MUXA
MUXB
MUXC

measurement. All of the sections initially disabled or cleared during the capacitance test are treated the same way here. The event input is secured by D1 and R3 when it's not in use. When the anode of D1 is brought low, control is given to the Event Pulse input so that a pulse can be measured. If the pulse to be measured is positive-going, IC2-d is pulled high. If the pulse to be measured is negative-going, IC2-d pin 12 is pulled low. That ensures that any pulse leaving IC2-d pin 11 will be negative-going. Next, a byte is sent to IC23 and IC24 to release IC5-b, IC7-a, IC7-b, IC8, IC26, and IC29 from their reset modes.

A positive-going START pulse, which tells the circuit producing the event to begin, is sent out. The input pulse enters IC2-d pin 13, and a negative-going pulse leaves IC2-d pin 11 and goes to IC4-b pin 9, and the counters begin counting. Flip-flop IC5-b watches for the event pulse to end; when the pulse ends (a rising edge is detected), IC5-b pin 9 goes high, disabling the Event section. That provides noise immunity by passing only the first pulse received. Because the pulse has ended, IC6-d pin 13 goes high, indicating that it is time to read back the final count. The period can then be determined with the formula described earlier.

Measuring a frequency

As in the other two processes, a set of initial conditions must be established. First bytes will be sent to IC23 and IC24 to disable IC1-a, IC1-b, IC2-d, and IC5-b. All counters will be reset as before and IC4-b pin 13 is pulled low to ensure that when IC7 is released from the reset mode it will be free-running.

The period section consists of IC3-d, IC10, IC11-b, IC12, IC13, IC14, and IC15. Once released from reset, IC7 produces a CLOCK pulse which is applied to IC10-a and IC11-b. That part, IC11-b, is the clock enable/inhibit gate that supplies IC12 with clock pulses. A 74HCT4040D 12-bit counter, IC12, ripple-carries to another counter, IC13, which ripple-carries to the last counter in the period section, IC14.

Eight channels from a 74HCT151D 8-channel multiplexer, IC15, are connected to eight of the counter outputs. The multiplexer output channel is connected to IC11-b, IC3-d, and pin 6 of IC25, a 74HCT573D octal latch. Pin 6 of IC25 is a read-back line for determining when the period has ended.

The operation of the Period section is as follows: IC7-a, IC10-a, IC17, and IC18 are all released from reset. IC7-b produces a 15-MHz clock signal that is fed to IC10-a and IC11-b. When the first rising edge reaches the clock input of IC10-a, pin 6 of IC10-a goes low. That releases IC12, IC13, and IC14 from reset. Prior to that event, all the counter, or "Q" outputs were low due to the reset condition. At this time, IC11-b has a low on pin 5 and a clock signal on pin 4. That produces a clock signal on IC12 pin 10.

Since the counters are no longer in a reset condition, they go into a free-running mode. Eventually, the multiplexer line currently selected is fed a high condition. The high is fed to IC11-b, IC3-d, and IC25 pin 6. When pin 6 of IC11-b goes high, it inhibits IC12, IC13, and IC14. The output of IC3-d was high before the reset was removed, low after reset and before the counter went high, and high after the counter went high. If IC3-d produces a high, then IC16-c is an inverter and consequently IC17-b is inhibited. If IC3-d is low, then IC16-c is a buffer and IC17-b is enabled. In other words, during the time when the counters are not in reset, but prior to the counter output being fed back to IC3-d, the frequency being measured is allowed to clock IC17, IC18, IC26, and IC29. The length of the period is determined by the counter output, or "Q" that is allowed to pass through IC15.

The T1001 was designed to produce eight different timebases between 0.1 and 20 seconds. The period of any given timebase can be determined by calculating the amount of time it will take for the target "Q" to go high at the given clock rate. That method is not as exact as it could be, due to propagation delays. The preferred calibration method is obtained by working backwards. You input a relatively high, known frequency into the counter input and start a period. Once the count is read

FRONT-END PARTS LIST

Resistors
R1—33 ohms, 16-pin DIP resistor
R2—2200 ohms, 10-pin SIP resistor
R3—1000 ohms, 10-pin SIP resistor
Capacitors
C1–C7—0.15 μF, 50 volts, monolythic or polystyrene
C8–C11, C20–C28—1500 pF, 63 volts, polystyrene
C12–C19—220 pF, 100 volts, ceramic disc
Semiconductors
IC1—74LS573D octal latch
IC2—74LS688D 8-bit magnitude comparator
IC3—74LS245D octal transceiver
IC4—74LS02D quad 2-input NOR gate
IC5, IC6—octal buffer
IC7—74LS08D quad 2-input AND gate
Other components
J1—16-pin male header
J2—18-pin male header
J3—Right-angle PC-mount male DB25 connector
Miscellaneous: 17 shorting blocks (for J1 and J2), solder, etc.

ORDERING INFORMATION

Note: The following items are available from TSW Electronics Corp., 2756 N. University Drive, Suite 168, Sunrise, FL 33322 (305) 748-3387:

- **I1000 kit—$65.00**
- **I1000 PC board only—$35.00**
- **I1000, assembled and tested—$77.00**
- **6-foot interface cable (DB-25-6)—$12.95**
- **T1001 kit (includes PC board, all listed parts, project case, and pre-assembled front and rear panels—$149.00**
- **T1001 PC board only—$49.00**
- **T1001, assembled and tested—$179.00**
- **T1001 software (included free with T1001 order)—$10.00**
- **Capacitor kit (unmeasured)—$21.00**
- **Capacitor kit (measured to within 1%)—$26.00**

Add $5.00 S&H to any order. Check or money order only.

back, the period in seconds is equal to the count divided by the frequency. In that way you can determine the exact period, propagation delays included. Once you have mapped out the exact value of all eight periods, you can save them to disk and reverse the equation so that the frequency is equal to the count divided by the period.

Construction

To build the T1001 peripheral, a PC board is recommended. You can either buy a PC board from the source mentioned in the Parts List or make your own from the foil patterns we've provided. Note that the parts for the Front End are contained on the T1001 board shown with a dark line around them. There is also a separate Parts List for the Front End. Do not confuse the two lists of parts, or where they go on the board. Install parts on the board as shown in Fig. 3. Also, for many of the capacitors, notice that there are three holes on the board, with two of them electrically the same. The holes accommodate capacitors of different sizes. Use the pair of holes that best fits the capacitors you use.

The frequency-input BNC connector (J1) must be wired to the board as shown in Fig. 3 with shielded cable. Binding posts J2–J4 are connected to the board with insulated stranded wire. For testing capacitors, "spring jacks" (J5–J7) allow quick insertion and re-

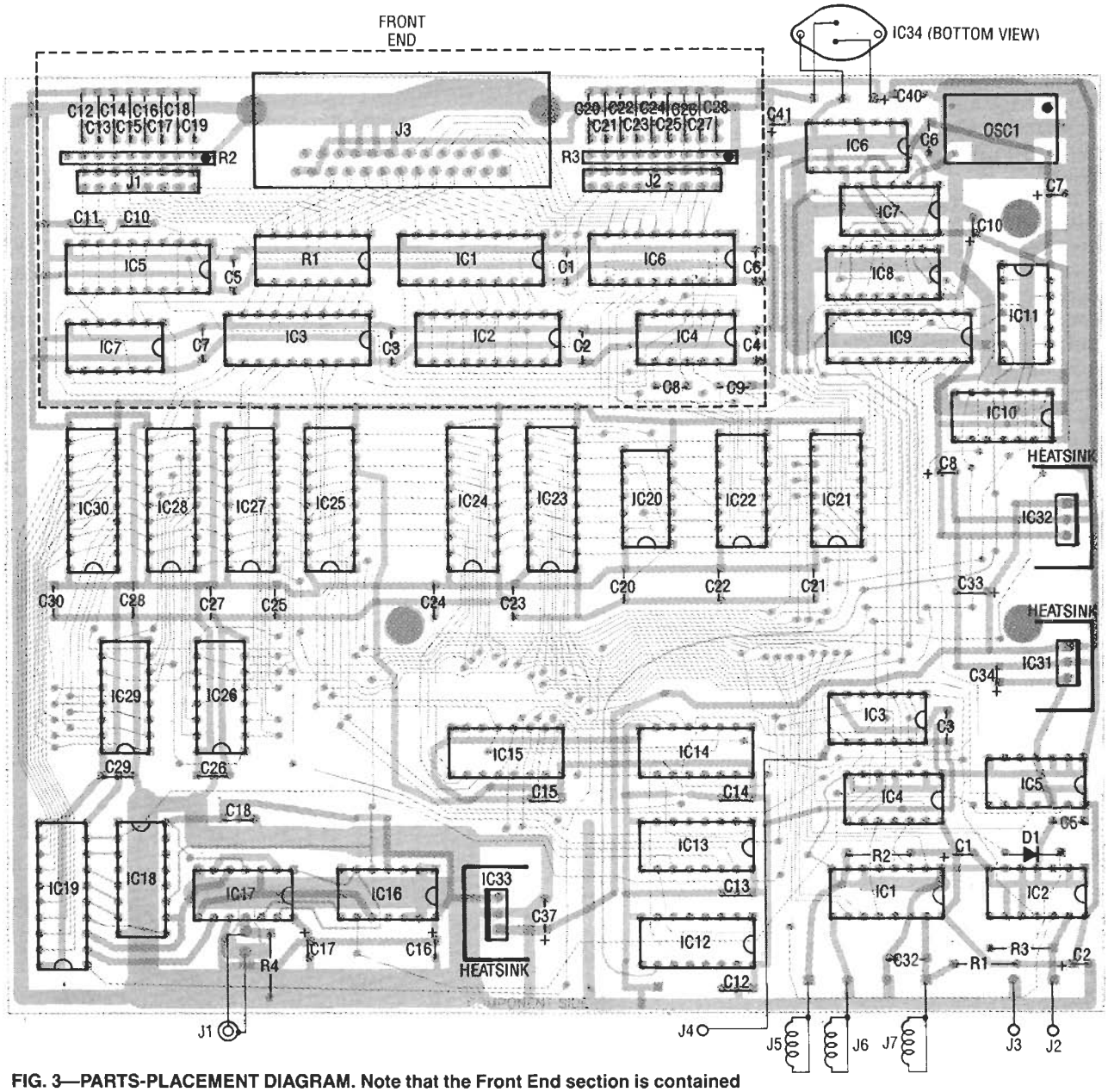


FIG. 3—PARTS-PLACEMENT DIAGRAM. Note that the Front End section is contained on the T1001 board shown with a dark line around it. There are separate Parts Lists for the sections, so be sure not to confuse them. (The extra holes where capacitors are mounted are for accommodating capacitors of different sizes.)

moval of test capacitors, as well as easy paralleling of capacitors to achieve any desired value. The spring jacks are simple springs bent in a semicircle, attached to the front panel with a screw at both ends, and connected to the PC board with insulated stranded wire. There is one spring jack for large-value capacitors (J5), one for small-values (J7), and a common one for ground (J6).

However, a problem with the spring jacks is that a spring is an inductor, and the measured capacitance would vary depending on how the capacitor is inserted into the springs. Therefore, a fine-gauge shunting wire must be "woven" around the back edge of each spring and soldered to the jumper wire that connects the spring jack to the board.

Making spring jacks can be difficult and tedious for the average do-it-yourselfer. Therefore, anyone who purchases a complete kit for the T1001 will receive a preassembled front panel—it's drilled, silkscreened, and all the jacks, including the three springs, are mounted on it. To save yourself a lot of hassle if you're not buying the kit, you can use any kind of capacitor test jacks such as binding posts or alligator clips.

Four voltage regulators are used in the T1001: IC31–IC34. Three of them (IC31–IC33) are LM340T's in a TO-220 case, and the proper heatsink should be attached to each of them. The fourth regulator (IC34) is an LM340K in a TO-3 case. That regulator must be mounted on the back panel of the T1001 case, also with an appropriate heatsink, and hardwired to the board. Figure 4 shows the completed T1001 board.

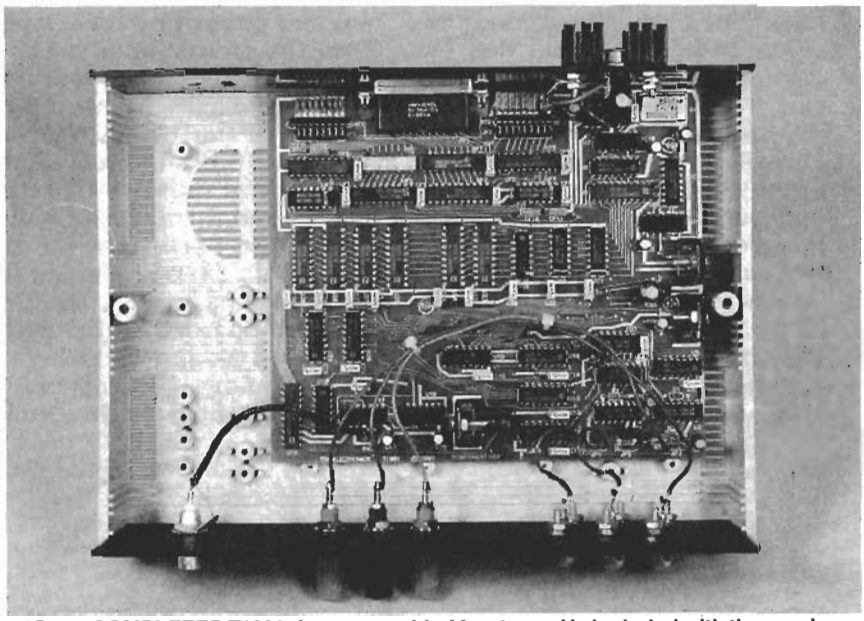


FIG. 4—COMPLETED T1001. A preassembled front panel is included with the purchase of a T1001 kit.

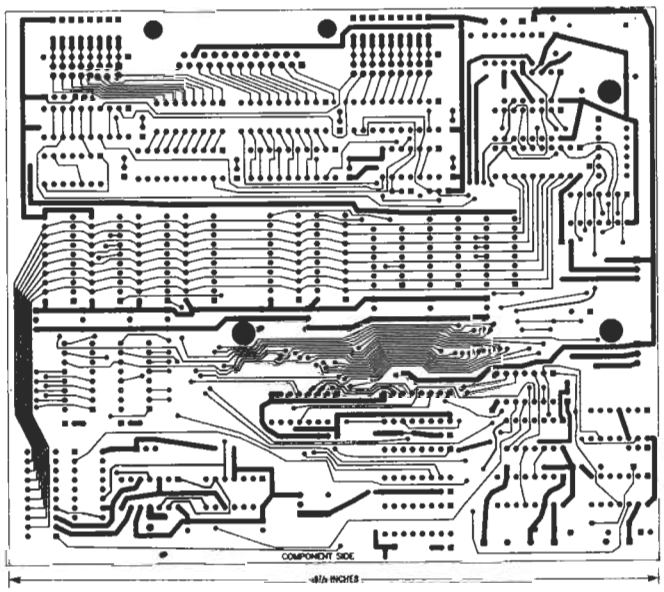
Software

Each peripheral, including the I1000 itself, has its own software program to control its own operation. All of the programs end up in one directory as you add more peripherals. Software for the I1000 and the entire series of peripherals, including the T1001, can be downloaded all at once from the RE-BBS (516-293-2283, 1200/2400, 8N1) as a self-unarchiving zip file called I1000.ZIP. Both compiled and uncompiled software is included. Software is included free with the purchase of any peripheral from the source mentioned in the Parts List. (Software can also be purchased from that source if you're not buying anything else from them and you have no way of downloading it from the RE-BBS.) Before you can do anything with the I1000 system, the software must be installed in your computer. To do that, type "install" and then hit Enter, and follow the instructions you are given.

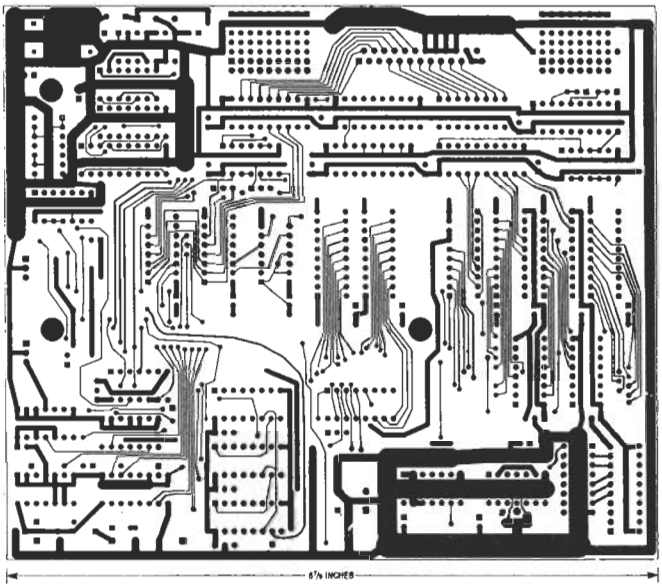
Operation and calibration

Before installing the I1000 card in your computer, the card must be calibrated. To calibrate the I1000, you'll need a dual-trace oscilloscope capable of measuring a 400-nanosecond pulse, two ×1 probes, and a non-metallic alignment tool. Set both oscilloscope channels to 2 volts/division, the timebase to 0.2 microseconds/division, the trigger slope to negative (−), and then set the sync source to channel 1.

Power down your computer,



COMPONENT SIDE of the T1001 board.



SOLDER SIDE of the T1001 board.

install the I1000 card, and connect the scope's ground lead to the I1000's metal mounting bracket. Attach the channel-1 probe to TP11 and channel 2 to TP5. Boot your computer and change directories to \TSW. Type "CALI1000" and press Enter. Press the space bar until the status line indicates "WRITING." Adjust the trigger level of your scope until you are in sync with channel 1. Adjust R12 until the waveform on channel 2 is centered within the waveform on channel 1. Move the channel-1 probe from TP5 to TP7. Press the space bar until the status line indicates "READING." Adjust R13 until the waveform on channel 2 is centered within the waveform on channel 1. Move the channel-2 probe from TP7 to TP9. Adjust R14 until the waveform on channel 2 is centered within the waveform on channel 1. Power down the computer and remove the probes; the I1000 is now fully calibrated.

All three functions of the T1001 peripheral must also be calibrated. When the system is up and running, the main, or "TSW" menu allows you to choose between the different functions of the peripheral. First choose the frequency-counter option, and you'll then be presented with the frequency-counter menu as shown in Table 1; pressing the keys shown on the right side will execute the functions shown on the left side.

TABLE 1—FREQUENCY

Function	Press
Units (Hz, etc.)	U
Quit	Q
Main menu	M
Direct	D
Timebase	↑ ↓
Calibrate	C

Connect the counter input to a known reference frequency, and make sure that frequency is displayed on the screen. Press "C," and answer "Y" to activate the calibration. After you are asked what frequency (in hertz) you are using for calibration, type it in and press Enter. The computer will take care of the rest.

The event/period menu is shown in Table 2. Again, pressing "C" activates the calibration mode. You will be asked to enter the number of nanoseconds needed to calibrate the period being displayed. The value you enter will be saved to disk and used in all subsequent readings. To remove the calibration offset, press "C" and enter a zero.

The capacitance-meter menu is shown in Table 3. Pressing "C" and answering "Y" from that menu activates the capacitance calibration process. You will then be asked to insert various known-value capacitors and press a key. The calibration capacitors required are shown in Table 4. The more precise the values of the calibration capacitors, the more precisely calibrated the T1001 will be. A package of the capacitor listed in Table 4 is available from the source mentioned in the Parts List.

TABLE 2—FREQUENCY

Function	Press
Units (μs, etc.)	U
Quit	Q
Main menu	M
Positive	P
Negative	N
Handshake toggle	H
Calibration	C

TABLE 3—CAPACITANCE

Function	Press
Units (uF, etc.)	U
Quit	Q
Main menu	M
Large cap test	L
Small cap test	S
Zero	Z
Direct	D
eXit zero or direct	X
Calibrate	C

TABLE 4—CAPACITORS

5 pF	.47 μF
10 pF	1.0 μF
47 pF	4.7 μF
100 pF	10 μF
470 pF	47 μF
1,000 pF	100 μF
4,700 pF	470 μF
.01 μF	1,000 μF
.047 μF	4,700 μF
.1 pF	10,000 μF

The I1000/T1001 pair should now be completely calibrated. With that and your computer, you're well on your way to having a versatile computer-controlled test bench. R-E

continued from page 6

parks. Several days before the broadcast, a portable Switched 56 "traveling case" is sent to the ballpark's technician. Somewhat larger than a briefcase, the case contains a modem, a codex, a digital service call-up unit, the power supply, and a power cord. The unit's AC power line and input and output connections are plugged in, and a MCI's phone number is dialed.

The equipment converts the analog voice signal to digital data for transmission to the CBS studios in New York where the broadcast is mixed and commercials are added. The finished product is than digitally transmitted (uplink) to a satellite for retransmission (downlink) to all CBS network and affiliate stations, which convert the digital data back to an analog broadcast signal. Because the equipment is full duplex, the Switched 56 also carries two-way communication between New York and the broadcast site.

CBS made use of the Switched 56 system at the NCAA Basketball Tournament, the Masters Golf Tournament, and for live news coverage of the New Hampshire presidential primary. CBS affiliate, KMOX in St. Louis, will broadcast half of its Cardinals games with the system.

Correcting soil contamination

According to Sandia National Laboratories, heavy-metal contamination of soil and ground water is a widespread problem for the nation. Sandia says the problem is particularly serious at the Department of Energy's weapons complex. The Albuquerque, NM, laboratories are studying electrokinetics as one possible technique for the direct removal of such contaminants from soil waters.

In the electrokinetic technique, electrodes are implanted in the soil, and a direct current is passed between the electrodes. This has two effects: First, ions in the soil-water solution begin to migrate toward the oppositely charged electrode—a process called electromigration. Second, and at the same time, soil-water begins to flow toward the cathode—a process called electro-osmosis.

The combination of those two effects can cause contaminant ions to move toward one electrode or the other, promising in-place removal of contaminants from the soil. The contaminants are actually removed by one of sseveral methods, including electroplating at the electrode. Thje other methods are precipitation or co-precipitation at the electrode, and pumping or ion-exchange of water near the electrode.

Both electrokinetics and electo-osmosis have been tried for increasing the density and solidifying slurries, and to to extract water from liquefied soils, paper mats, and concrete. More recently electro-osmosis has removed heavy metals and soluble organic contaminants from saturated clays in laboratory experiments.

Sandia is now trying to learn more about electrokinetic remediation and to evaluate the kinds of contaminants and soil conditions that are appropriate candidates for that remediation. The issues being evaluated are: the removal of heavy metals with complex redox chemistry, the effectiveness of the process in partially saturated soils, the effects of mixed soils on the process, and methods for scaling the process up to practical field applications.

FCC allocates radio-spectrum space for interactive TV

The Federal Communications Commission on January 16 voted unanimously to allocate a portion of the radio spectrum for interactive video and data services (IVDS) use, paving the way for a new wireless broadcast industry in interactive television, which will allow consumers to shop, bank, and pay bills directly through their television sets, without requiring a telephone line or computer. The action was a result of a petition filed in 1987 by TV Answer (**Radio-Electronics**, February 1992).

The FCC, which will allocate one megahertz in the 218–219-MHz band for use by companies providing IVDS services, is expected to issue the first IVDS licenses by the end of this year.

Updated area-code plan

Since area codes were first introduced in 1947, they've had "0" or "1" as the middle digit, indicating to the switch that a long-distance call is being made. With only two of the original 144 codes still available, we're in imminent danger of "running out" of area codes in the near future. A plan mapped out by Bellcore's North American Numbering Plan (NANP) Administration (Livingston, NJ) describes how new area codes can be distributed. The proposed two-part strategy is designed to meet telecommunications numbering needs at least through the first quarter of the 21st century by allowing the numbers "2" through "9" to be used as the middle digit.

The plan is the backbone of the NANP Administration's long-range "Proposal on the Future of Numbering in World Zone 1," which has been distributed to more than 3000 telephone companies, manufacturers, governments, and other interested parties in the World Zone 1—the United States, Canada, and 16 Caribbean countries—where Country Code 1 is the international-dialing designation. Under the plan, 300 new area codes will be assigned to specific geographic areas, tripling the number now available. Ninety more codes will be reserved for non-geographic uses: 80 for personal communications and 10 for special-purpose service access codes such as today's 800 or 900 codes. The remaining codes will be allocated for future growth and as-yet-unidentified future needs. The plan predicts that eventually all calls made in World Zone 1 will require ten digits.

Bellcore's NANP Administration, a small group that has the responsibility for administering the scarce telecommunications numbering resources for all countries in World Zone 1, works closely with local telephone companies that manage local telephone exchanges. After hearing industry comments, the NANP Administration will reissue the proposal by the end of the year. Once consensus has been reached, further study of the steps needed to achieve the plan's long-term goals will begin. **R-E**