CAPACITANCE ADAPTER FOR YOUR DMM

Here's a simple adapter circuit that lets your DMM measure capacitance up to 2.2 microfarads

BY JOHN CLARKE AND GREG SWAIN

WHEN WAS THE LAST TIME YOU HAD TROUBLE DEciphering a capacitor label? The fact is that it's easy to misinterpret capacitor markings. And that's something that no one can afford when building projects.

A capacitance meter easily solves that problem by allowing you to simply plug the unknown capacitor into the test terminals and read the value in picofarads (pF) or microfarads (μF) directly from the digital display. You can also use a capacitance meter to check suspected bad or unmarked capacitors, as well as select critical capacitor values.

If you are one of the fortunate few hobbyists who have purchased one of the modern digital multimeters, you may already have a capacitance meter. Many of them now come with built-in capacitance ranges that are typically capable of measuring up to about 20μF.

On the other hand, if you are like most of us who use digital multimeters that don't have capacitance-reading capabilities, then perhaps this simple *Capacitance Adapter** is for you.

The Adapter is designed to plug directly into the test terminals of a DMM, and allow you to measure capacitance values of up to 2.2 μF in two ranges: 0-2200pF (.0022μF) and 0-2.2 μF. Don't be put off by the rather low upper limit of the circuit—capacitors with values greater than 2.2 μF are usually clearly marked and seldom require testing.

On the down side, the Adapter is only suitable for use with digital multimeters, which usually have fixed input impedances of 10 megohms, because analog meters (with their comparatively low input impedances) would load down the circuit, causing inaccurate readings.

*This story first appeared in *Silicon Chip*, Australia (November, 1987); reprinted with permission.

About the Circuit

Figure 1 shows the schematic diagram of the Capacitance Adapter, which is basically a capacitance-to-voltage converter. The circuit consist of only two active devices: a 74HC132 quad, two-input NAND Schmitt trigger (U1) and 7805 5-volt regulator (U2). One gate in the U1 package (U1-a) forms a free-running oscillator, while R1 allows for frequency adjustments. The squarewave output of the oscillator is fed to two inverters, U1-b and U1-c.

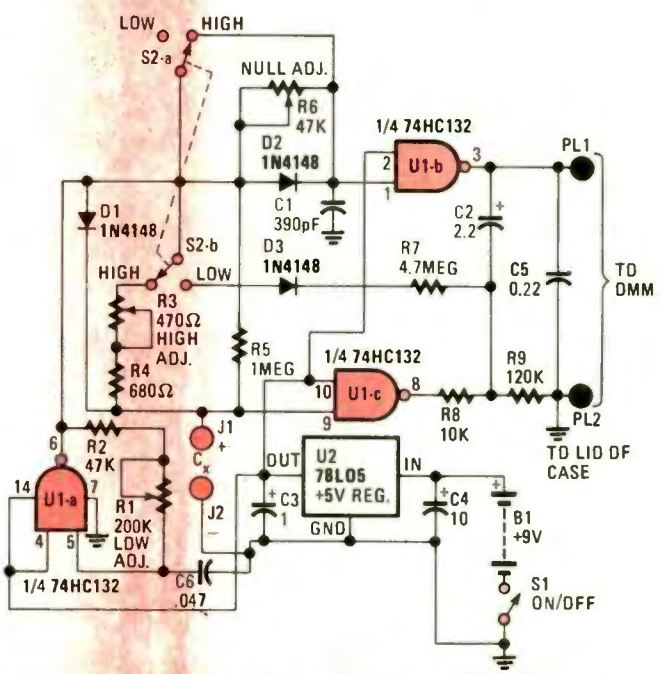

Fig. 1—The circuit is built around a single 74HC132 quad NAND Schmitt trigger. It produces a voltage that is directly proportional to the unknown capacitance, C_x.

When the capacitor in question (which we'll refer to as C_x) is connected to the J1/J2 input terminals, the circuit produces a voltage—one millivolt per picofarad on the lower range and one volt per microfarad on the upper range—that is directly proportional to the capacitance. And it is that voltage that's shown on the DMM display and interpreted as a capacitance value.

Capacitor C_x (when connected across J1/J2) charges via D1 during the positive half-cycle of the oscillator output and discharges on negative half-cycle via resistor R5 (in the LOW range) or via the series-parallel network formed by R3/R4 and R5 (in the HIGH range).

When the circuit is set to the HIGH range, the output of U1-a is fed directly to the pin 1 input of U1-b. So the output of U1-b is simply an inverted reproduction of its input signal. And with no capacitor connected across the J1/J2 input terminals, the output of U1-c is virtually identical to that of U1-b. If we were to measure the voltage difference between the U1-b/U1-c outputs, the result would be zero.

Now consider what happens when a capacitor is connected across the J1/J2 terminals. Capacitor C_x charges quickly via D1 and discharges slowly via R3/R4 and R5. That causes pin 9 of U1-c to stay high for longer than it stays low (the time duration on the size of the capacitor). So the output waveform from C_x is a series of pulses at the same frequency as U1-a, but with the pulse length being inversely proportional to the size of C_x.

Refer to Fig. 2. Waveforms A, B, and C correspond to the outputs of the three gates, respectively. If C_x is relatively large, the positive pulses fed to pin 8 of U1-c will be very short (as shown in waveform C). If the averaged voltage difference between the waveforms B and C is measured, it would be proportional to the capacitance of C_x.

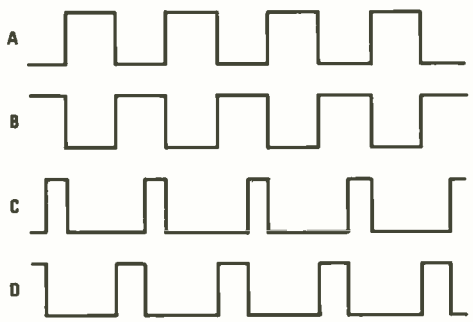

Fig. 2—This collection of waveforms shows the relationship between the three NAND Schmitt triggers when the circuit is set to the HIGH range.

The pulses are filtered by a dual RC filter (consisting of R8/C2 and R9/C5) to give a smooth DC voltage. That voltage is then measured by the DMM to give a direct readout of the capacitor value.

Sadly, things become more complicated when the circuit is switched to the LOW range due to stray capacitance across the J1/J2 terminals. Without some correction for stray capacitance, reading low-value capacitors would result in serious errors. That's where the null circuit comes into play.

When S2 is set to the LOW range, the output of U1-a is fed to pin 1 of U1-b via diode D2, charging the 390-pF capacitor, C1. Capacitor C1 charges quickly via D2 and discharges slowly via R6. So the input to pin 1 stays high for a short period, each time pin 6 of U1-a switches low. The result is that the positive pulses output by U1-b are slightly shorter than they otherwise would be; compare the waveforms shown in A and B of Fig 3. Look closely, as the difference may not be apparent at first glance.

The C wavform in Fig. 3 shows the output of U1-c with only stray capacitance at the J1/J2 input (in other words, no test capacitor is connected). The stray capacitance is charged via D1 and discharges via R8, so the positive output pulses of U1-c are also slightly shorter than they otherwise would be (if there was no stray capacitance).

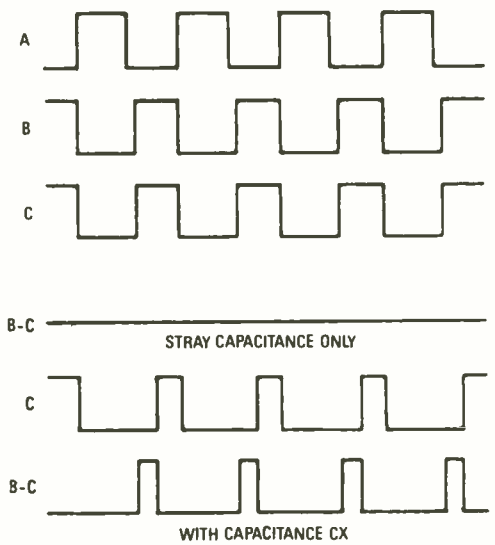

Fig. 3—Shown here are the waveform timing diagrams for the LOW range. Note that the positive pulses at B and C are shorter than those at A, due to capacitor C1 and the stray capacitance at the J1/J2 input.

Potentiometer R6 is the null adjustment, which should be set so that the positive-going edge of the B waveform in Fig. 3 coincides with the positive-going edge of waveform C (making the delay times equal). If measured, the voltage difference between waveform B and C would be zero, because the two waveforms are identical. In other words, the effects of stray capacitance are canceled out.

Offset Voltage

When the circuit is set to the LOW range, D3 and R7 are switched into the circuit. Diode D3 feeds the squarewave output of U1-c to a voltage divider consisting of R7 and R8 (which is tied to pin 8 of U1-c). Actually, D3 is forward biased only when the output of U1-b exceeds 3.1 volts, and is reverse biased when the output drops below that value.

As a result, a fixed 5-mV offset appears on the negative output terminal (jacking up the negative terminal by 5 mV). To null the circuit, the voltage on the positive terminal must also be increased by 5 mV. That's achieved by adjusting R6 so that U1-b goes high before U1-c triggers.

The offset voltage overcomes a tendency for U1-b and U1-c to lock together when their respective trigger points are close. By adding the 5-mV offset, the circuit is nulled with U1-b set to trigger well before U1-c, eliminating the locking problem.

On the HIGH range, stray capacitance is insignificant compared to the value of C_x, so the nulling circuit is disabled (via S2). Similarly, the offset-voltage circuit is no longer required and D3 is also disconnected via S2.

Power for the circuit is derived from a 9-volt transistor-radio battery. A 78L05 3-terminal regulator provides a regulated 5-volt source so that the oscillator and nulling circuits remain in calibration over the life of the battery.

The circuit demands that U1 be a high-speed CMOS NAND gate (74HC132) because that type of IC has shorter propagation times than do standard CMOS. And that's particularly important when measuring low-capacitance values on each range.

Construction

The Capacitance Adapter was built on a small printed-circuit board, and housed in a small plastic enclosure, measuring about 3½ × 2¼ × 1¼ inches—although any suitably-sized enclosure will do. The project (with banana plugs PL1 and PL2 protruding through the rear of the enclosure) is designed to be plugged directly into the DMM test terminals. The two banana jacks, J1 and J2, are mounted on the front panel of the enclosure, along with the range and power switches.

Begin construction by first etching a printed-circuit board, using the full-size foil pattern shown in Fig. 4 as a template.

PARTS LIST FOR THE CAPACITANCE ADAPTER

SEMICONDUCTORS
U1—74HC132 quad two-input NAND Schmitt trigger, integrated circuit
U2—78L05 low-power 5-volt regulator, integrated circuit
D1–D3—1N914 or 1N4148 small signal diode

RESISTORS
(All resistors are ¼-watt, 5% units, unless otherwise noted.)
R1—200,000-ohm miniature, vertical PC-mount trimmer potentiometer
R2—47,000-ohm
R3—470-ohm miniature vertical, PC-mount trimmer potentiometer
R4—680-ohm
R5—1-megohm
R6—47,000-ohm miniature vertical, PC-mount trimmer potentiometer
R7—4.7-megohm
R8—10,000-ohm
R9—120,000-ohm

CAPACITORS
C1—390-pF polystyrene
C2—2.2-µF 16-WVDC electrolytic
C3—1-µF 16-WVDC electrolytic
C4—10-µF 16-WVDC electrolytic
C5—0.22-µF metalized polyester
C6—0.047-µF metalized polyester

ADDITIONAL PARTS AND MATERIALS
B1—9-volt transistor-radio battery
J1, J2—banana panel jacks (1 red, 1 black)
PL1, PL2—banana plugs
S2—Double-pole, double-throw toggle switch
S1—Single-pole, double-throw toggle switch
Printed circuit or perfboard materials, enclosure, IC sockets, battery connector, alligator clips, wire, solder, hardware, etc.

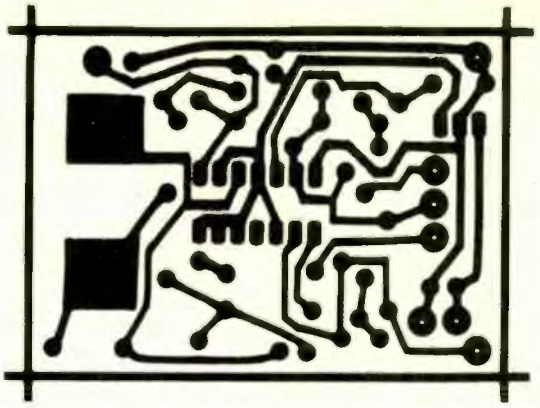

Fig. 4—Shown here is a full-scale template of the Capacitance Adapter's printed-circuit artwork.

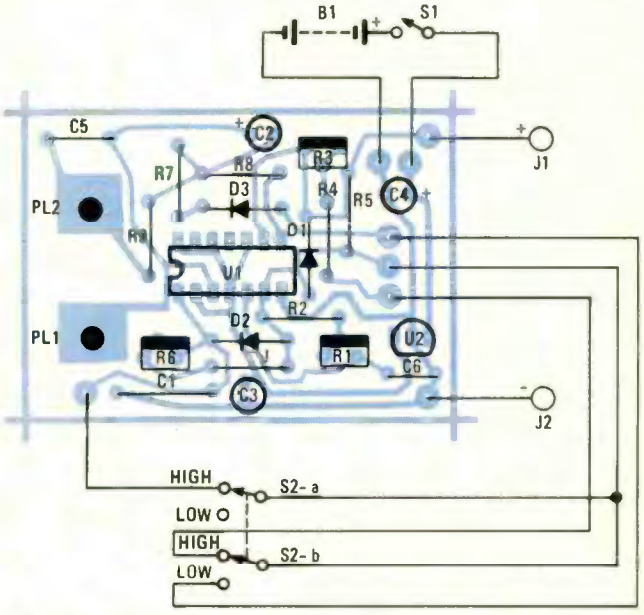

Fig. 5—This parts-placement diagram of the Adapter shows both location and orientation of the board-mounted components, as well as indicating the off-board wiring connections.

Once etched, begin installing the components given in the Parts List using Fig. 5 as a guide. Install the resistors, capacitors, and trimmer potentiometers; followed by U1 and U2. And don't forget to install the jumper (marked with a J). Make sure that all polarized parts (ICs, diodes, and electrolytic capacitors) are correctly oriented.

The banana plugs are soldered to the foil side of the board (see photos) and further secured using the screw-on insulated moldings. It will be necessary to cut the moldings down to about ¼-inch, so that the battery fits into the case. The switch and input-terminal positions can then be labeled using dry-transfer (rub-on) lettering, and the finished panel sprayed with a clear lacquer to keep the lettering from rubbing off.

Next mount the switches and test terminals to the finished front panel of the enclosure, and connect the off-board components to the circuit board as shown in Fig. 5.

The case can now be drilled to accept the printed-circuit board assembly. Two 0.32-inch holes are drilled in the rear panel to provide clearance for the banana plugs, while another three holes are drilled in the sides of the case to allow screwdriver access to the trimmer potentiometers.

The assembly goes together with the battery sandwiched

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between the board and the front panel of the enclosure (see photo). A strip of electrical tape can be used to prevent shorts between the battery case and the trimmer potentiometers.

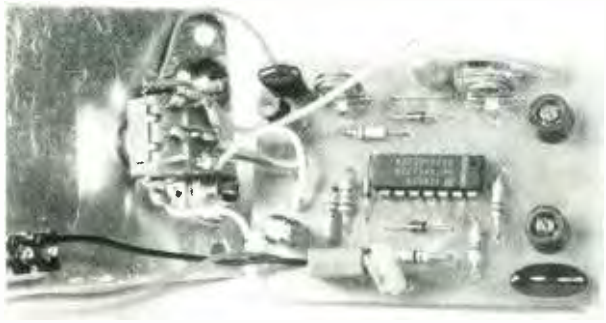
Calibration

Calibrating the circuit involves first setting the NULL adjustment (R6), then adjusting R1 and R3 so that the DMM displays the correct reading for a capacitor of known value on the LOW and HIGH ranges, respectively.

To set the NULL control, set the DMM to the millivolt range, S2 to LOW, and adjust R6 for a reading of 0 mV. In practice, it is difficult to set R6 so that the meter reads exactly zero, so a reading that is slightly negative is considered satisfactory.

Now connect a capacitor of known value, say between 1000 and 2200-pF, across J1 and J2. Adjust R1 so that the meter displays 1 mV per picofarad. In other words, if the capacitor value is 1000 pF, adjust the meter to read 1 volt).

Finally, set the Adapter to the HIGH range and connect a 0.1 to 1-μF capacitor across J1 and J2. Adjust R3 so that the meter displays 1-volt per microfarad (or 0.1 volt for a 0.1-μF capacitor and 1 volt for a 1-μF capacitor). ■



The Capacitance Adapter is designed to be plugged directly into the jacks of your DMM. Banana plugs PL1 and PL2 are soldered directly to the underside of board, and protrude the enclosure of the project.

Shown here is the Adapter's printed-circuit board prior to being sealed in its enclosure. Note that the battery is sandwiched between the printed-circuit board and the front panel of the enclosure.