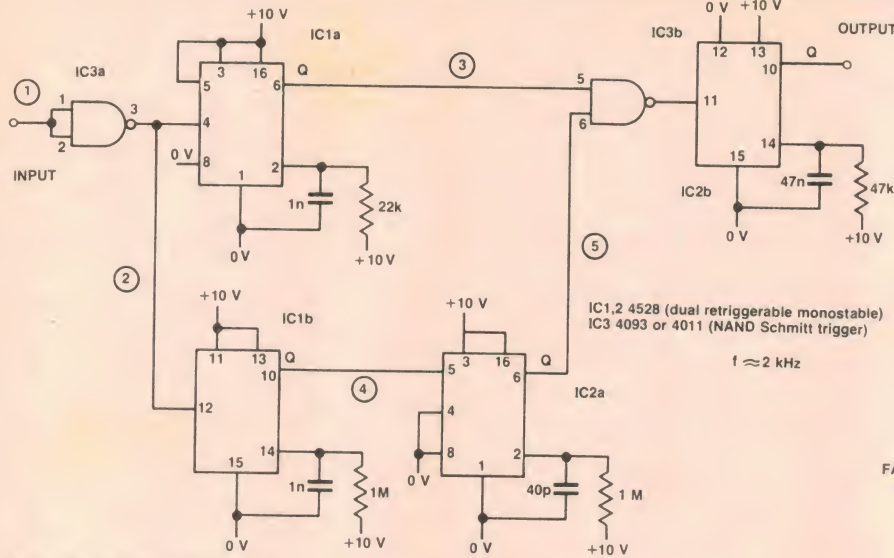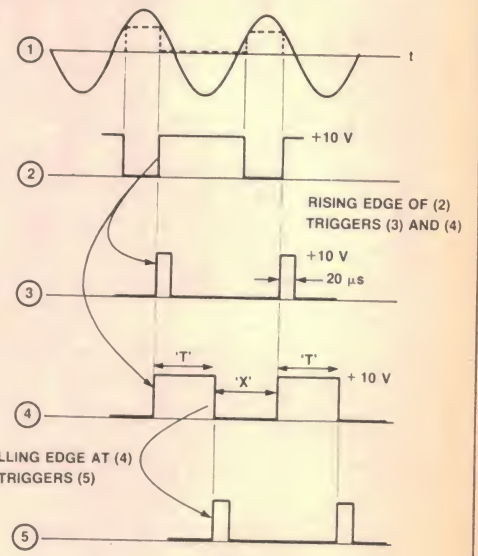# IDEA OF THE MONTH

Audio frequency switch. Sine wave input (peak value equal to supply voltage) applied to input will cause output to go high within a certain narrow range of frequency. Response outside this range is zero.

IC1,2 4528 (dual retriggerable monostable)
IC3 4093 or 4011 (NAND Schmitt trigger)

f ≈ 2 kHz

RISING EDGE OF (2) TRIGGERS (3) AND (4)

FALLING EDGE AT (4) TRIGGERS (5)

T=RC

NO OUTPUT

Case 1. Input frequency is below the acceptor frequency.

'X' ALMOST DIMINISHED TO ZERO

OVERLAY ZONE FOR (3) AND (5)

PULSES (3) AND (5) APPEAR SIMULTANEOUSLY AT GATE, HENCE THE OUTPUT TO TRIGGER IC2b

Case 2. Input frequency is within the acceptor range.

Case 3. Input frequency is higher than the acceptor frequency. IC1b is retriggered before its timed interval has elapsed. Its output is permanently high and the waveform (5) disappears. Hence no triggering of IC2b is possible.

Tone operated switch ☆ ★ ☆

Ian Johnston, Mt Eliza Victoria

This is a new approach to the idea of operating a switch by means of a tone, such as a whistled note. It avoids the problems of acceptor filters formed by twin-T networks in the feedback paths of op-amps. They either oscillate or fail to discriminate against loud noises pitched just outside the acceptor frequency.

Gate IC3a squares up the input waveform and triggers IC1a and IC1b on the rising edge of its pulse. IC1a produces a short pulse (approximately 20 μs) which is applied to gate IC3b.

IC1b is set to a time delay that equals the period of the accepted frequency. It forms a reference which measures the period of every cycle of the incoming signal.

IC2a is triggered on its negative edge by the output pulse of IC1b. At the desired frequency the pulse from IC2a (which is short — about 20 μs) will appear at the gate almost simultaneously with the pulse from IC1a. These two pulses overlap, causing an output pulse at the gate.

The output pulses appear at intervals of T (period of the acceptor frequency) and since IC2b is timed longer than T, it is repeatedly retriggered and its output remains high for the duration of the signal.

(Note diagrams of waveforms). When the incoming signal is too low in frequency, pulses do not coincide at gate IC3b.

When the incoming signal is too high in frequency, IC1b is prematurely retriggered, remaining permanently high at pin 10 (Q), causing elimination of any pulse output from IC2a.

(1) Ideally, C in IC1a and IC1b should be the same value to equalise start up delay upon triggering, but with small values of C this delay is negligible.

(2) Frequency of acceptance is controlled by R and C on IC1b. Bandwidth of acceptance is controlled by R and C on IC2a.

(3) A 4011 can be used in place of the 4093 for IC3, but the latter is probably preferable.
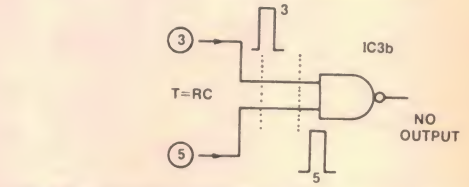
(4) ICs 1 and 2 are 4528 dual retriggerable monostables.

(5) IC2b can be connected to be positive or negative edge-triggered; it does not matter which. IC2a, however, *must* be negative-edge triggered.
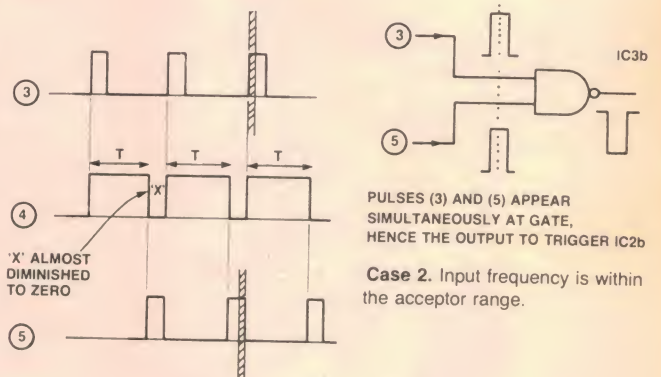
(6) The input signal should rise to a peak which is about equal to the supply voltage to ensure reliable triggering.

(7) The circuit will not trigger at one half or one quarter of the acceptor frequency.

I intend to use the circuit in a 'hands-free' whistle-switched intercom in my workshop (where I frequently have dirty hands).
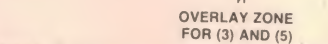
In a breadboard assembly using two complete circuits, the values of C and R must be chosen for IC1b: low note — 1n, 1M5; high note — 1n, 1M. Cheap greencap capacitors were used. The frequencies of acceptance measured were 900 Hz and 2 kHz respectively.

This arrangement can be made to switch on to a few whistled bars of 'I did it my way', and switch off to a few bars of 'Colonel Bogie'. Needless to say, the circuit will also find use in less frivolous applications.

When a sine wave (peak value equal to supply voltage) is applied to the input and output will go high within a certain narrow range of frequencies. Outside this range the response will be zero.

The frequency at which the circuit responds is a function of the time constant set by the capacitor and resistor on IC1b. The 'breadth' of the response range depends on the time constant set by the capacitor and resistor on IC2a.