Technical Article

Introduction to the Class E Power Amplifier

September 25, 2024 by Dr. Steve Arar

Learn how Class E amplifiers improve on the efficiency of Class D amplifiers at RF frequencies.

For a Class D amplifier to provide high efficiency, it needs switches that are quite fast relative to the frequency of operation. This becomes increasingly challenging as we move to higher and higher frequencies. In a Class D RF amplifier, switching intervals can take up a considerable portion of the operating cycle. Losses from parasitic capacitances also increase with frequency, presenting a further problem.

Class E power amplifiers effectively overcome these challenges. Like their Class D counterparts, these are switching-mode amplifiers. However, their load networks are specifically designed to minimize switching losses and channel the energy from shunt (transistor output) capacitances to the load. In this article, we'll discuss how the design of the Class E amplifier avoids the pitfalls of Class D operation at high frequencies.

Contrasting the Class D and Class E Circuits

Consider the complementary voltage-switching Class D amplifier shown in Figure 1.

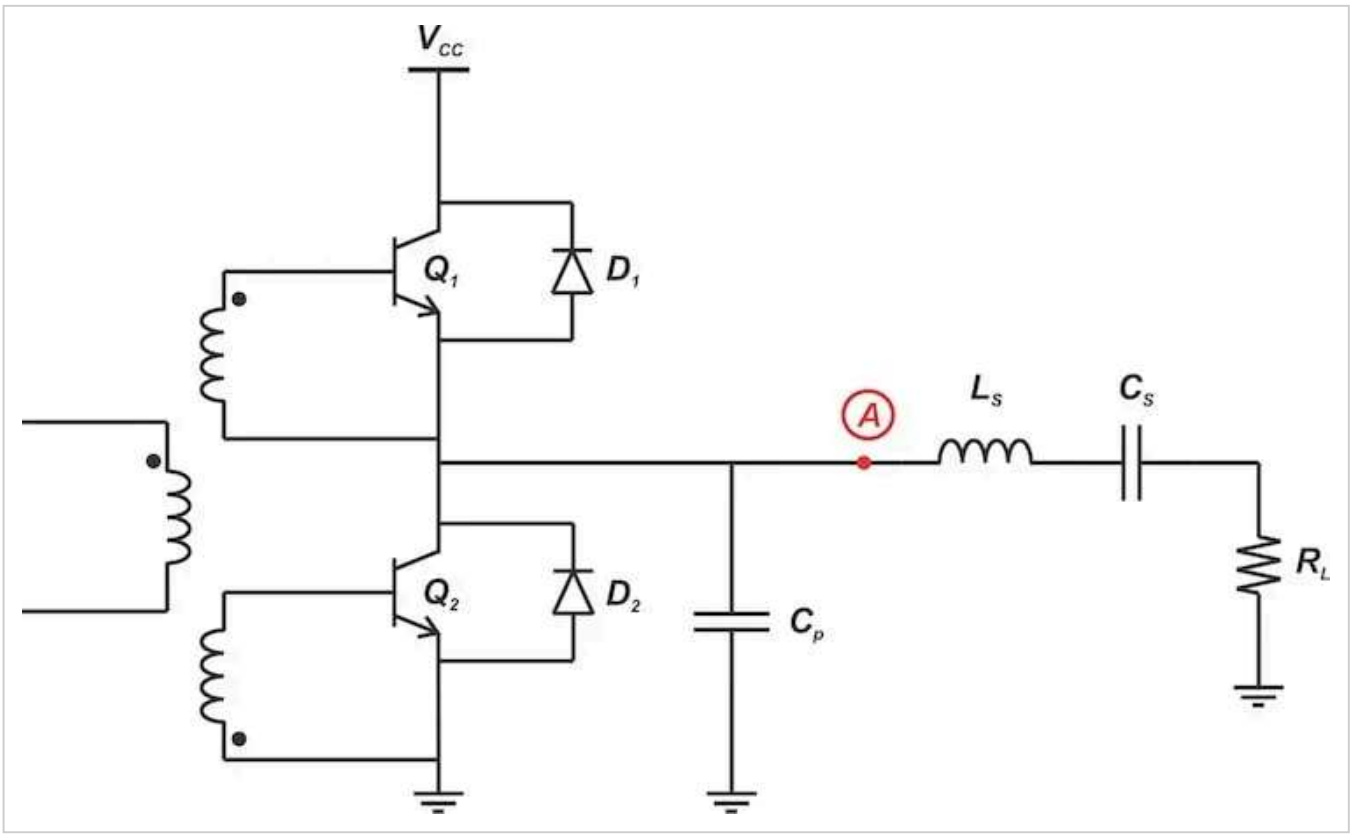

Figure 1. Complementary voltage switching configuration with the parasitic capacitances of node A modeled by C_p.

In the above figure, C_p models the parasitic output capacitances of the transistors. The transistors turn ON and OFF on alternating half-cycles, causing the voltage at node A to switch between V_{CC} and ground. Whenever a transition occurs, the charging and discharging of C_p leads to some energy being dissipated as heat in the on-resistances of the switches.

For example, for a transition from V_{CC} to ground, transistor Q_2 turns ON and discharges the charge that was initially stored in C_p. This dissipates some energy in the on-resistance of Q_2. The total power lost due to the charging and discharging of C_p is:

$$P_{dissipated} = C_p V_{CC}^2 f$$

Equation 1.

where f is the amplifier's switching frequency.

The operation of the Class D amplifier involves charging and discharging C_p, but the energy stored in the capacitance isn't delivered to the load. In fact, the value of C_p doesn't influence the output RF power at all—the power it draws from the supply is lost to heat.

By contrast, Figure 2 shows the circuit schematic of the simplest possible Class E amplifier.

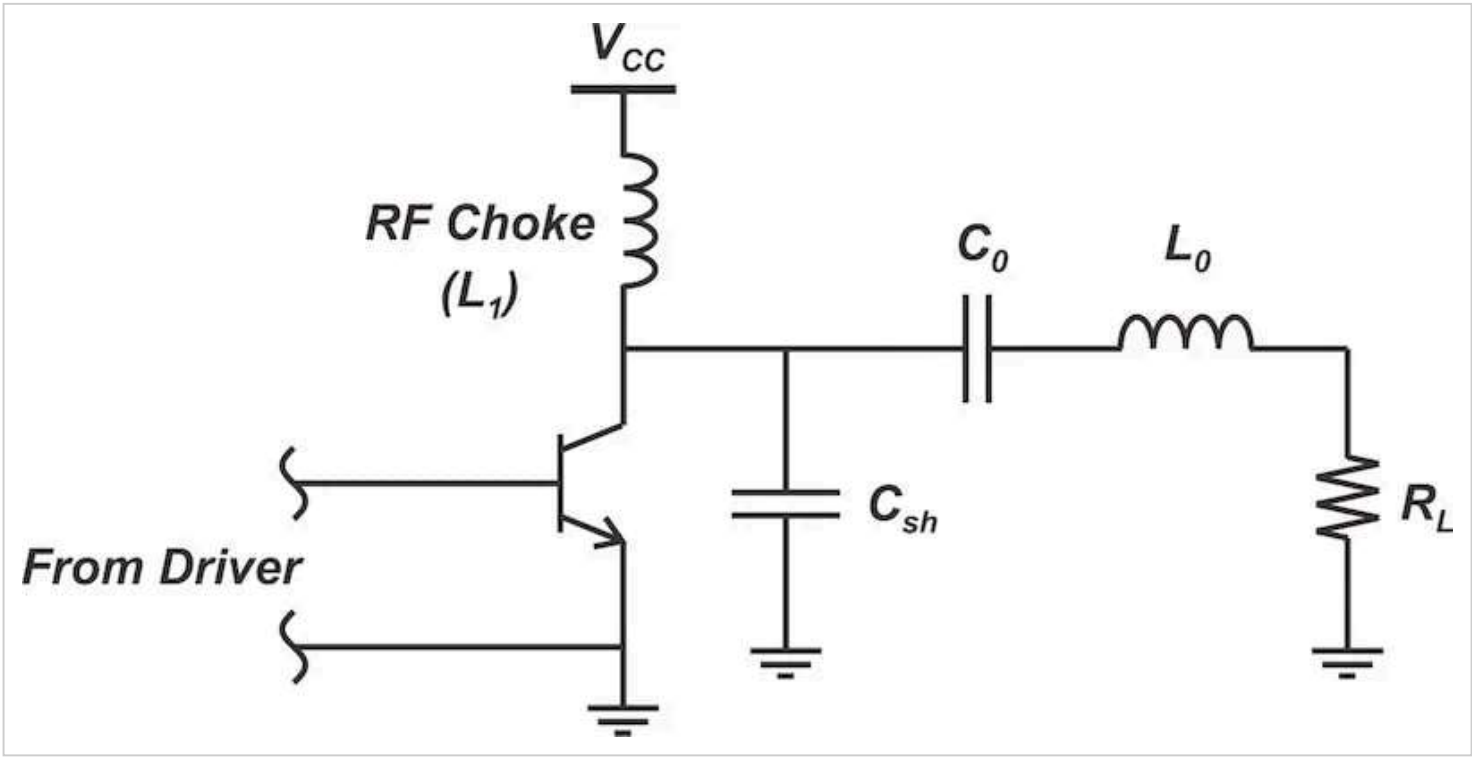

Figure 2. Schematic of a low-order Class E amplifier.

The transistor in this circuit is driven to act as a switch. The RF choke (L_1) provides a DC path to the supply and approximates an open circuit at RF. L_0 and C_0 form a series tuned circuit that connects the load to the collector of the transistor.

Between the transistor and C_0 is the shunt capacitance (C_{sh}). The shunt capacitance includes both a capacitor added at the output and the device output parasitic capacitance. Unlike in the Class D amplifier, the energy stored in this capacitance isn't dissipated as heat—instead, it's channeled to the load.

As we'll see later on in this article, C_{sh} plays a key role in the Class E amplifier's operation. Before we get to that, however, we need to understand the problem of finite switching speed. Only then will we be ready to discuss how the Class E power amplifier deals with that problem.

The Impact of Slow Rise and Fall Times on Switch-Mode Operation

When the drive signals of the switches are ideal, they approximate a rectangular waveform with sharp edges. To more accurately reflect practical conditions, we should instead assume that the switch current and voltage waveforms are trapezoidal instead of rectangular. This is illustrated in Figure 3.

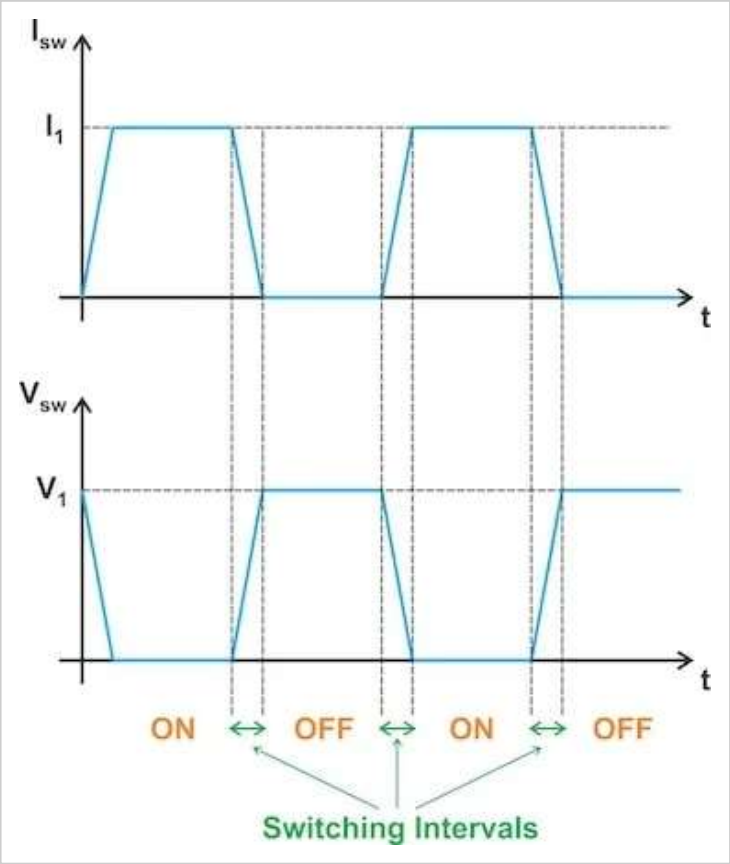

Figure 3. The current (top) and voltage (bottom) waveforms of practical switches exhibit non-zero transition intervals.

To understand the waveforms in Figure 3, recall the basic idea behind switching-mode power amplifiers—namely, that operating the transistors as switches rather than current sources leads to a higher efficiency. An ideal switch dissipates no power because the product of its voltage and current is zero at all times. With the switch ON, it has no voltage drop; with the switch OFF, it has no current flow. Since the transistor dissipates no power, the theoretical efficiency of a switch-mode power amplifier can approach 100%.

In practice, however, transistors don't change state instantaneously. During the switching intervals, both the voltage across the switch and the current through it are appreciable. With a non-zero *IV* product, power is dissipated in the transistors, reducing the amplifier's efficiency.

Class E amplifiers prevent this situation by strategically time-displacing the voltage and current switching transitions from each other. Ideally, this leads to zero power dissipation in the transistors even when the switching transitions make up a substantial portion of the RF period. The timing offset is achieved through careful design of the load network, including the shunt capacitance at the device output (C_{sh} in Figure 2). In the coming sections, we'll examine how this design eliminates switching losses during both turn-OFF and turn-ON transitions.

Eliminating Switch Turn-OFF Losses

A circuit with a purely resistive load will have the switch voltage and current waveforms shown in Figure 3, where a change in the switch current translates to an instantaneous and proportional change in the switch voltage. However, if we add a shunt capacitor to the load network, we can expect some delay between the edges of the switch voltage and current waveforms. This is because the voltage change across a capacitor (ΔV_c) is inversely proportional to the capacitance, as we see in Equation 2:

$$\Delta V_c = \frac{I \Delta t}{C}$$

Equation 2.

For a given current (I), an additional capacitance (C) reduces ΔV_c over a given time interval (Δt). We can therefore produce the required timing offset by choosing a sufficiently large shunt capacitor.

Figure 4 shows how adding a time delay affects the waveforms from Figure 3.

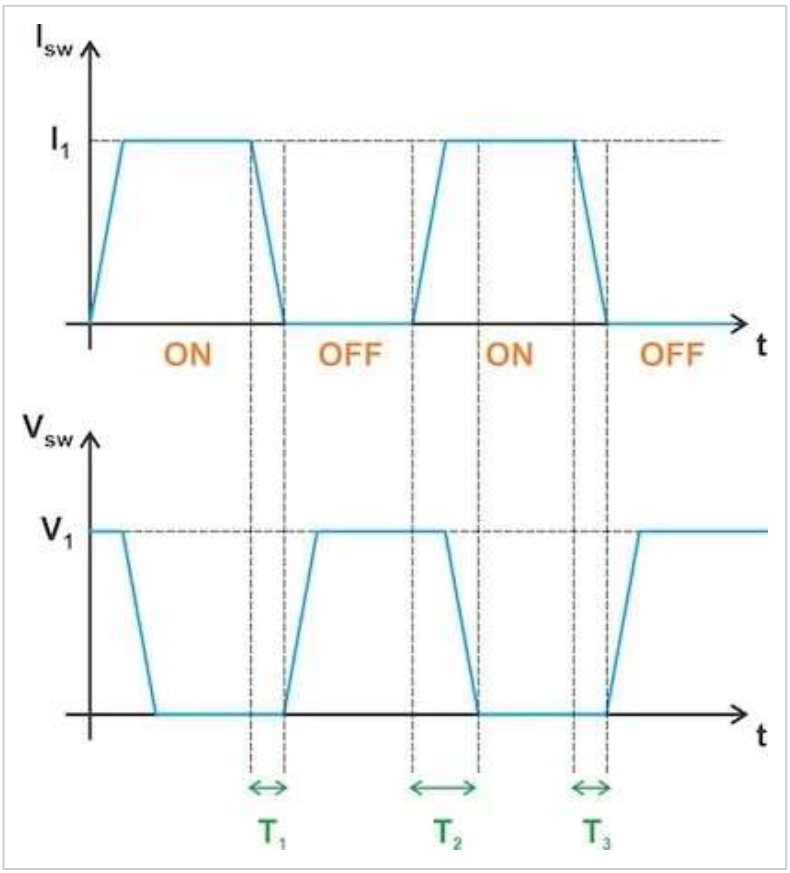

Figure 4. Waveforms produced by delaying the rise of the collector voltage until after the switch current reduces to zero.

In Figure 4, the non-zero portions of the voltage and current waveforms don't overlap during the ON-to-OFF transitions of the switch (the T_1 and T_3 intervals). We therefore have $IV = 0$ during the turn-OFF transitions, leading to zero power loss. However, the overlap around the T_2 interval—the OFF-to-ON transition—actually increases.

It's clear that merely introducing a delay isn't enough to eliminate switching losses during both sets of transitions. To understand how the Class E amplifier eliminates switch power losses during OFF-to-ON transitions, we need to examine the circuit when the switch is in the OFF state.

Eliminating Switch Turn-ON Losses

Figure 5 shows the Class E amplifier's load network when the switch is OFF.

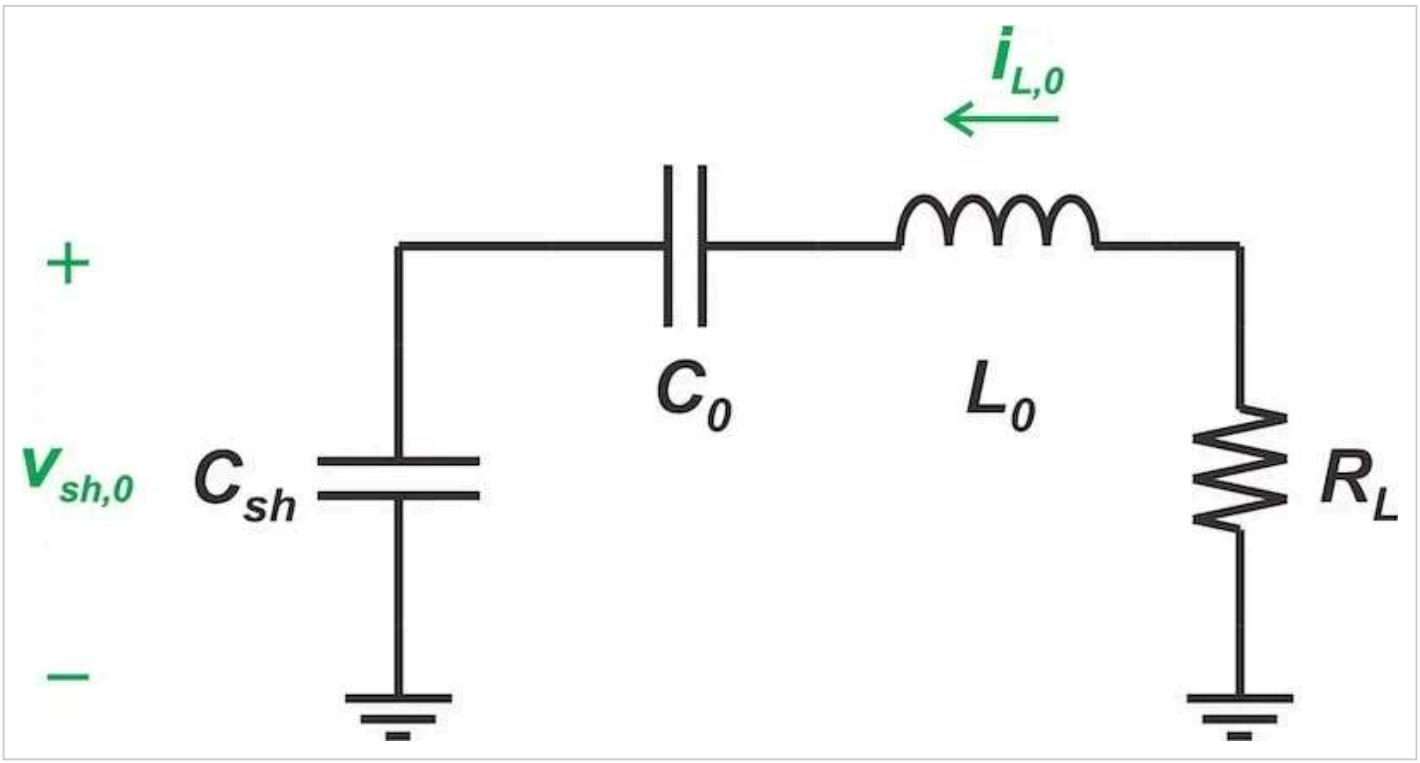

Figure 5. The load network of the Class E amplifier when the switch is OFF.

After the switch turns OFF, the load network of a Class E amplifier operates as a damped second-order system with some initial energy stored in its inductor (L_0) and capacitors (C_0 and C_{sh}). Though no input is applied to the load network in this half-cycle, the initial energy stored in the system causes a transient response. The transient response eventually dies out due to R_L dissipating energy.

To gain insight into the response of the load network, let's use the LTspice schematic in Figure 6. Note that both the initial conditions and component values for this circuit were chosen arbitrarily.

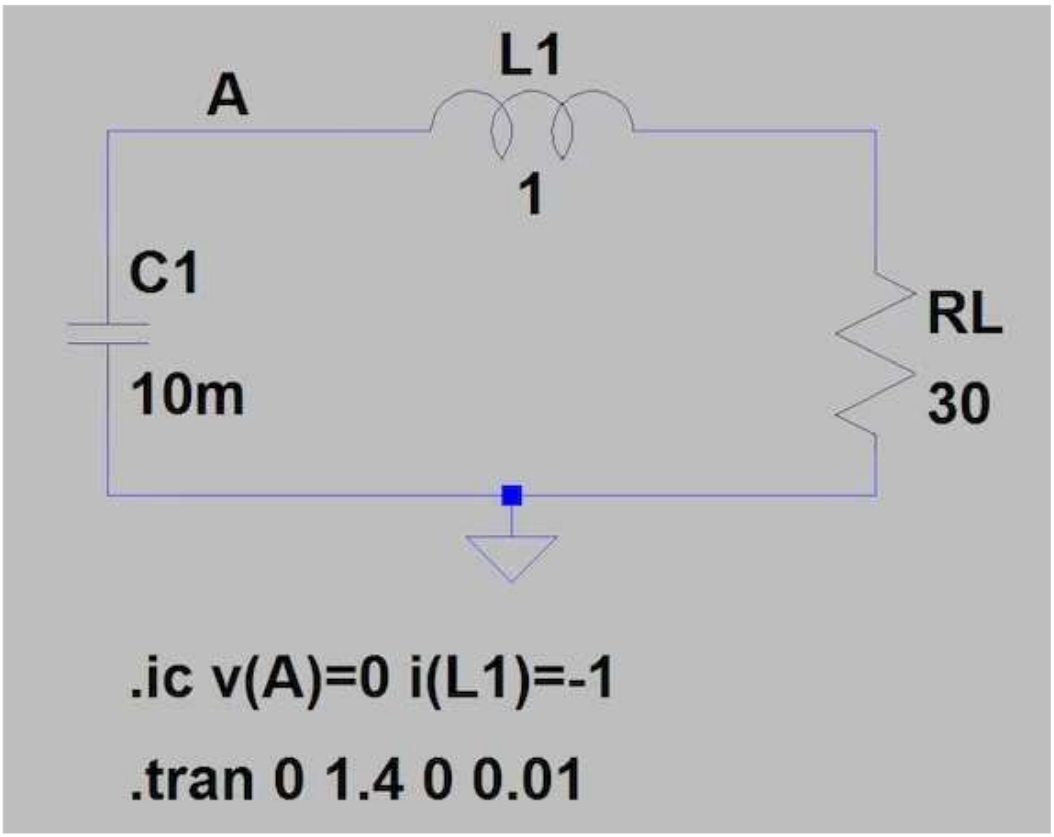

Figure 6. LTspice schematic for examining the response of a series RLC circuit with some initial conditions.

From our circuit theory courses, we know that the value of the components can result in three distinct types of transient responses:

- Overdamped.
- Critically damped.
- Underdamped.

Figure 7 shows the time response of the voltage across the capacitor (C_1) for three different values of R_L, allowing us to examine all three levels of damping.

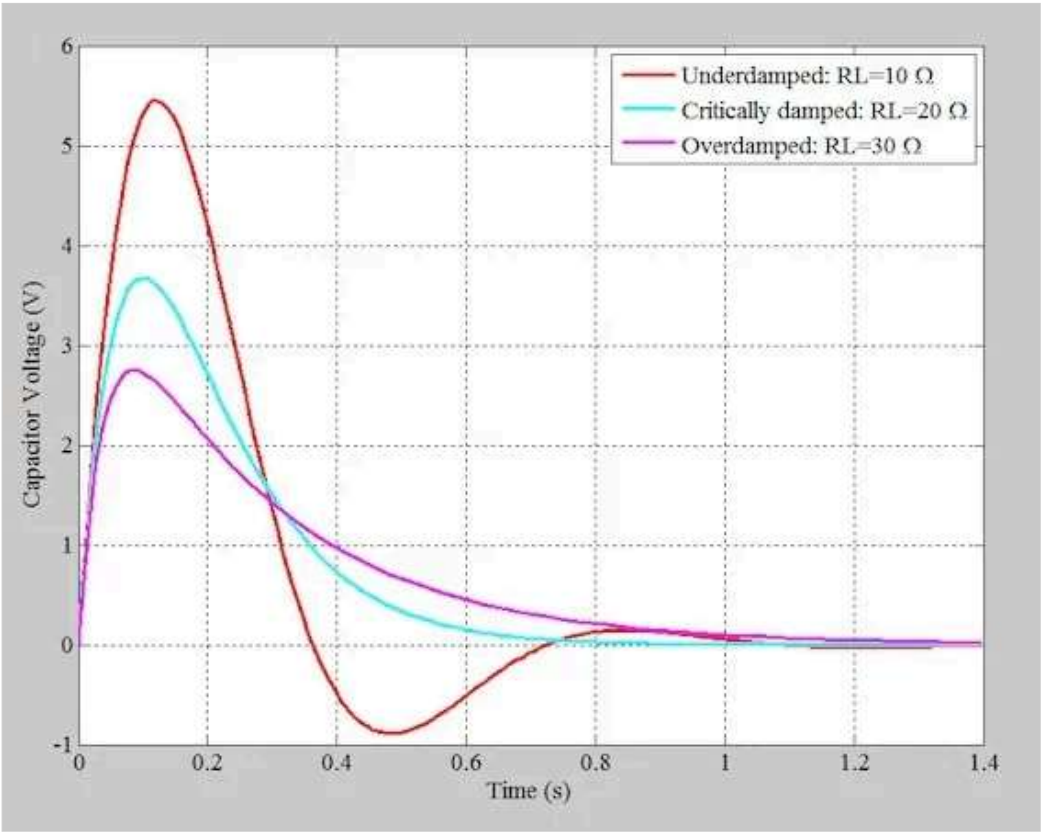

Figure 7. The response of the series RLC circuit for $\mathbf{R_L}$ ***= 10 Ω, 20 Ω, and 30 Ω.***

Although the shape of the response depends on the component values, the presence of R_L ensures that the final capacitor voltage is zero. If the OFF half-cycle of the switch in our power amplifier is long enough, the capacitor voltage will actually reduce to 0 V when the switch turns ON. Unlike the hypothetical situation illustrated in Figure 4, this automatically eliminates the overlap between the switch current and voltage waveforms during the OFF-to-ON transition.

Figure 8 shows typical—though not ideal—switch waveforms for the Class E amplifier.

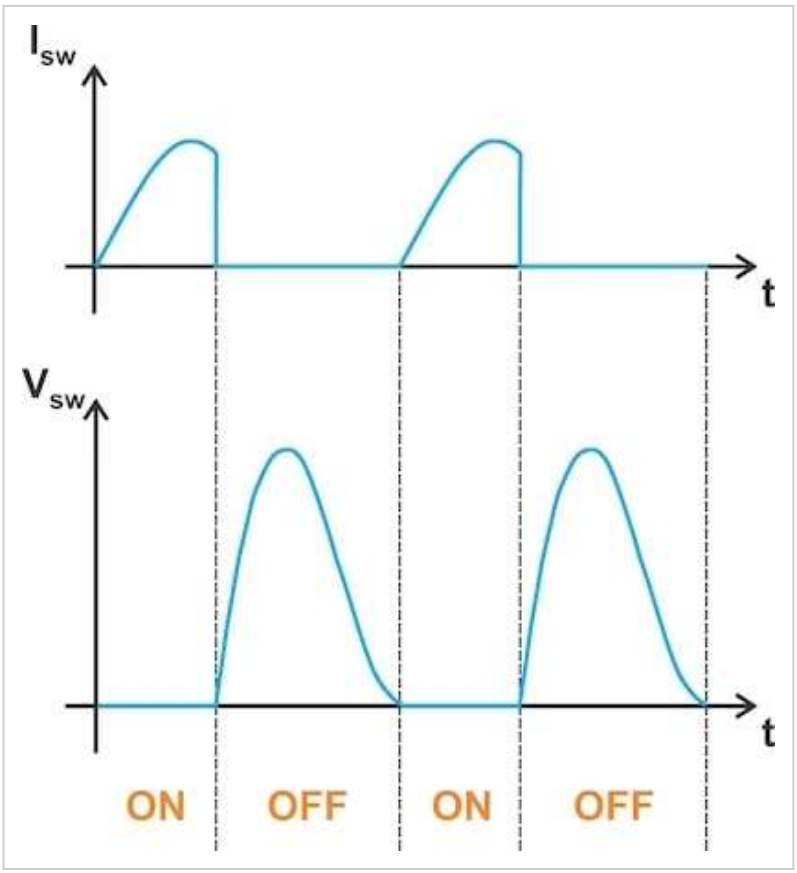

Figure 8. Typical switch current (top) and voltage (bottom) waveforms for a Class E amplifier.

Wrapping Up

For optimum performance, the load network in a Class E amplifier should be designed to produce a critically-damped response. We'll discuss the reason for this in a future article. Before that, however, we'll investigate the ideal switch voltage and current waveforms for Class E power amplifier design. We'll also discuss the practical constraints on generating these waveforms.

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