Simple Prescaler **for Transmitters**

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Most phase-locked loop (PLL) based transmitters use a prescaler chip at the heart of their oscillator. A single-chip prescaler like SAB6456 is a divide-by-64 or divide-by-256 switchable prescaler. It offers high sensitivity and ease of use. But electronics hobbyists, particularly in India, have a tough time finding these chips in the market.

The circuit presented here solves this problem by using three low-cost, readily-available integrated circuits (ICs) and offering three common divider rates of 64, 128 and 256. It works well from 1MHz to 150MHz and is suitable for use in PLL FM transmitters and other frequency

synthesisers for HAM band including 2-metre amateur radio band (144MHz-148MHz).

Test Points

Test point	Details
TP0	GND
TP1	12V DC
TP2	5V
TP3	RF input frequency /4
TP4	RF input frequency /16
TP5	RF input frequency /32
TP6	RF input frequency /64
TP7	RF input frequency /128
TP8	RF input frequency /256

PARTS LIST

Semiconductors:
IC1   - 7805, 5V voltage regulator
IC2, IC3   - 74AC74 dual D flip-flop
IC4   - CD4040 ripple counter
T1, T2   - 2N2222 npn transistor
LED1   - 5mm LED
Resistors (all 1/4-watt, ±5% carbon):
R1, R2, R5, R7 - 10-kilo-ohm
R3, R4   - 220-kilo-ohm
R6   - 3.3-kilo-ohm
Capacitors:
C1   - 100μF, 25V electrolytic
C2, C4, C5   - 0.1μF ceramic disk
C3   - 10pF ceramic disk
Miscellaneous:
CON1   - 2-pin connector terminal
CON2   - 4-pin connector
JACK1   - RF jack interface connector
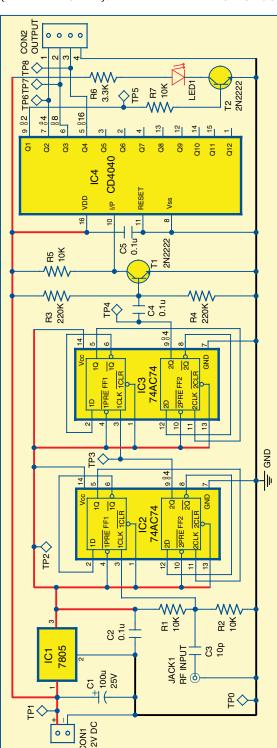   - 2-pin connector

Fig. 1: Circuit diagram of the simple prescaler for transmitters

Circuit and working

Circuit diagram of the simple prescaler for transmitters is shown in Fig 1. It is built around voltage regulator 7805 (IC1), dual D-type positive-edge-triggered flip-flop 74AC74 (IC2 and IC3), ripple-carry binary counter CD4040 (IC4) and a few other components.

The four cascaded flip-flops in IC2 and IC3 have been configured to divide the input signal by a factor of 16. Radio frequency (RF) input (at JACK1) from the oscillator is applied to pin 3 of IC2 via capacitor C3. Signal from IC2 pin 9 is fed to pin 3 of IC3. Transistor T1 converts TTL output of IC3 to CMOS logic levels to drive clock input to pin 10 of binary counter IC4.

Output divider rates of 64, 128 and 256 are available at pins 1, 2 and 3 of CON2, respectively. The circuit can directly drive a CMOS divider chip like CD4059 (not shown here). LED1 indicates that the prescaler is working normally. In the absence of RF input, LED1 remains off.

Construction and testing

An actual-size, single-side PCB pattern of the simple prescaler for transmitters is shown in Fig. 2 and its component layout in Fig. 3.

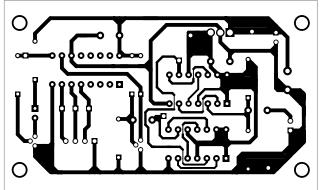*Fig. 2: Actual-size PCB pattern of the circuit of the simple prescaler for transmitters*

Fig. 3: Component layout of the PCB

power supply is recommended.

During testing, the prescaler performed well with an input frequency of 150MHz. Verify that test points in the circuit are as per the table before using the circuit.

To test the circuit, ensure there is 12V at test point TP1 and 5V at test point TP2 with respect to TP0, to verify the correct power supply. Now, give the RF signal using a function generator and measure the frequencies at different test points using an oscilloscope.

EFY Note. The circuit was tested successfully up to 10MHz RF frequency with around 1Vrms to 7Vrms. ●
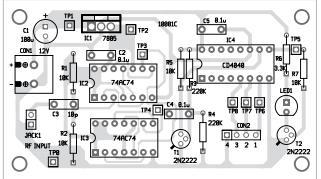
Assemble the prescaler on the PCB shown above or on a general-purpose PCB and enclose it in a suitable case. Use a shielded cable or a thin coax for input and output connections. Mount input (CON1), output (CON2) and RF jack (JACK1) on the panel. Keep all component leads as short as possible. A 12V regulated

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