Digital demodulator for phase-shift-keyed data

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Exclusive-OR gates and a repeat-modulation scheme can be combined to produce a digital phase-shift-keyed (PSK) demodulator that allows accurate recovery of the reference-carrier pulse train. The demodulation of binary PSK data usually involves two major problems: recovering the reference carrier, and differentiating between the logic 0 and the logic 1 data pulses. This latter problem is resolved easily with differential coding, assigning a logic 1 when the change in carrier phase is 180° and a logic 0 when there is no change.

The first problem, however, cannot be resolved as simply. Usually, the input PSK-modulated carrier frequency is multiplied by 2 to cancel out the phase changes. But this technique, unfortunately, generally results in a degradation of demodulator performance.

A better method is to remodulate the demodulator's local oscillator with the received data so that the phase changes due to input modulation are cancelled out. This produces a virtually unmodulated reference carrier that is equal in phase to one of the two possible input PSK phase states. The ambiguity between the two phase conditions can be resolved by differential encoding.

The circuit shown employs this improved demodulation technique. A quad exclusive-OR IC is used to perform both the demodulation and remodulation functions. Here the exclusive-OR gates are operated as controlled inverters. In the phase-detector portion of the circuit, the PSK input carrier and the remodulated voltage-controlled-oscillator (VCO) signal are normally at quadrature with each other when the system is in lock. This results in a pulse train having a 50% duty cycle at the output of gate G_1. The pulse train is then integrated by the low-pass filter into a dc error signal.

As the phase difference between the input PSK signal and the input VCO signal deviates from its normal 90° shift, the pulse train at gate G_1's output becomes width-modulated. The average dc error voltage then changes, correcting VCO phase and frequency in the direction that reduces demodulation error.

In the circuit's data-demodulator section, the input signal and the VCO output are either mostly in phase or mostly out of phase with each other, depending on the modulation status of the input PSK signal. Therefore, the output of gate G_2 is either logic 0 or logic 1, according to the status of the PSK data.

A second low-pass filter then integrates G_2's gate output signal, which is subsequently squared by the comparator to produce the demodulated output data. This final output signal is also used to modulate the VCO by means of gates G_1 and G_3. □

BIBLIOGRAPHY
C.A. Herbst, "Digital Phase-Locked-Loop with Loss-of-Lock Monitor," EDN/EEE, October 15, 1971.

Unscrambling a binary line. Demodulator for phase-shift-keyed inputs operates exclusive-OR gates as controlled inverters to decode the input data and recover the reference carrier. Input data is remodulated with an error-corrected output from the voltage-controlled oscillator, cancelling out any phase changes from the input modulation. This permits a nearly unmodulated reference carrier to be recovered.