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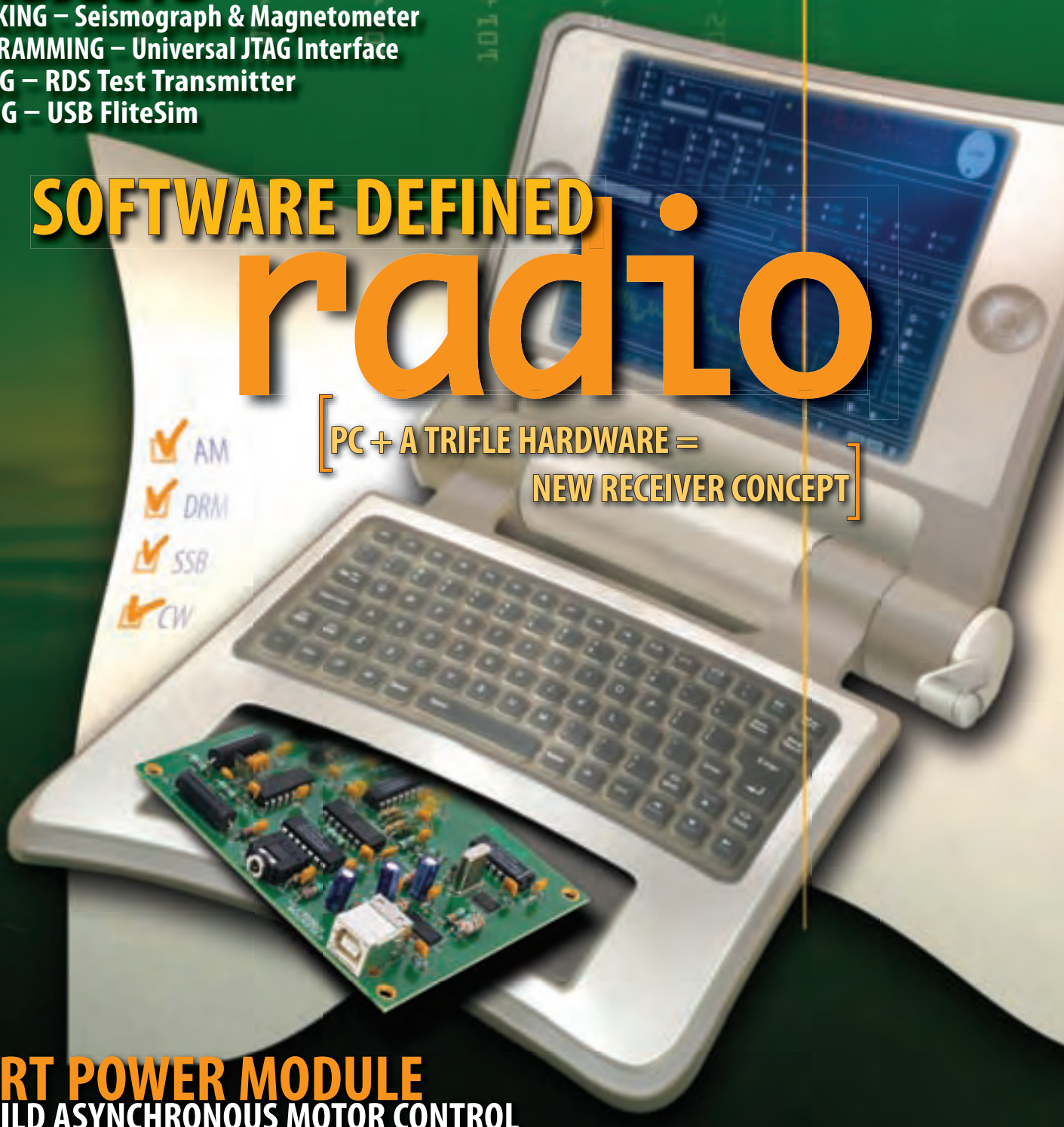
PROJECTS

- SHOCKING – Seismograph & Magnetometer
- PROGRAMMING – Universal JTAG Interface
- TX-ING – RDS Test Transmitter
- FLYING – USB FliteSim

SOFTWARE DEFINED radio

[PC + A TRIFLE HARDWARE = NEW RECEIVER CONCEPT]



SMART POWER MODULE
FAIRCHILD ASYNCHRONOUS MOTOR CONTROL

E•L•F RECEPTION
MOTHER EARTH ON THE RADIO

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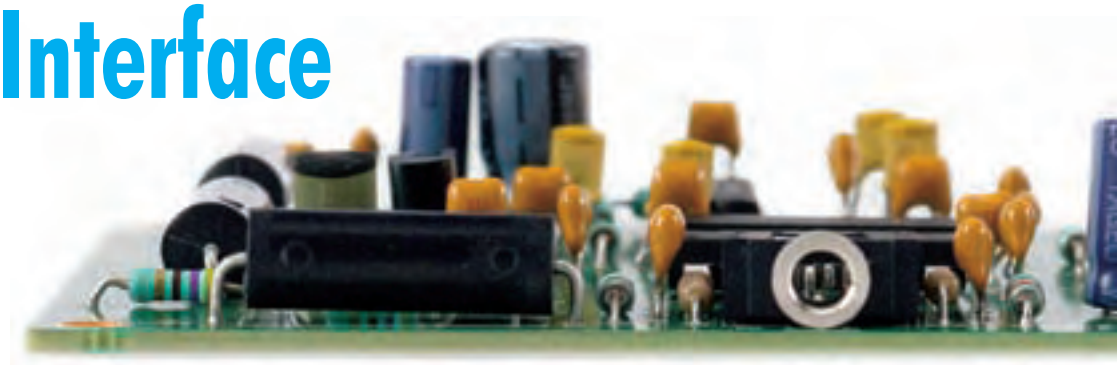
Software Defined

With USB Interface



Burkhard Kainka

SD (software-defined) radio receivers use a bare minimum of hardware, relying instead on their software capabilities. This SDR project demonstrates what's achievable, in this case a multi-purpose receiver covering all bands from 150 kHz to 30 MHz. It's been optimised for receiving DRM and AM broadcasts but is also suitable for listening in to the world of amateur transmissions.

The designer's aim for this project was to create a receiver displaying high linearity and phase accuracy. Development was focussed on the characteristics that were most important for a top-notch DRM receiver and the end result is a receiver with remarkable interference rejection characteristics. Reception of DRM stations using DREAM software produced signal-to-noise ratio (S/NR) values of well over 30 dB. The design principle of the receiver guarantees an extremely flat filter-curve response. This works out rather well not only for DRM but also for the audio quality of AM broadcasts, which sound almost as good as VHF FM. It's worth noting too that some transmitters that do not conform to the normal bandwidths laid down for medium wave (9 kHz) and shortwave (10 kHz) as rigidly as perhaps they should. Whilst these stations produce no observable sound improvement for listeners using normal receivers (since their IF filters limit the bandwidth and in the process the frequency response too), this is not the case with SDR, where it's no problem to select a wider bandwidth at will. It gets even better: in software receivers the fine-tuning capabilities of PC decoder programs give you the capability of determining the desired bandwidth with notch filters to the automatic level control (ALC) settings along with selecting all the usual receive modes from AM by way of DRM and SSB to CW.

Further refinements can be added for SWL (shortwave listening) applications. If for instance you wish to increase the sensitivity on the upper amateur bands this is easily arranged by using two switchable antenna inputs and providing an optimised preselector circuit or preamplifier in one of them. The receiver's printed circuit board itself provides a pretty basic RF front end, which is nevertheless perfectly adequate for broadcast reception. A long wire antenna of adequate length will lift the strength of signals above atmospheric noise level to ensure you miss virtually nothing.

Hardware requirements

Most SDR programs [1] require the Windows XP platform to operate satisfactorily. The most important hardware necessary then is an SDR-capable sound card. We have developed a small circuit for testing sound cards, described elsewhere in this issue under the heading 'Developer Tips'. Without performing this test first it's utterly pointless starting to make the SDR receiver!

All about USB

The receiver is controlled over a USB connection and powered with +5 V in the same way (no additional mains power supply needed). For the USB interface in the receiver circuit (Figure 1) we selected the FT232R from our Scottish friends at FTDI. This modern USB-to-serial converter works without the need for a quartz crystal, as it is equipped with an internal R-C oscillator of adequate stability. The module (IC4) is used here in its 'bit-bang' mode along the lines of a fast parallel port. Eight data lines are available for use and these can be driven in whichever way we choose. Two of the lines are used as an I²C Bus and control the frequency of the receiver. Three wires connect the input multiplexer to one of up to eight antenna inputs with and without filtering. Two additional inputs serve to control the IF amplification of the receiver. In this way the receiver operates entirely under remote control. Kiss good-bye to all those knobs and controls of bygone radio days…

Please pay particular attention to decoupling the power supply. One reason for this is because the USB chip

Radio

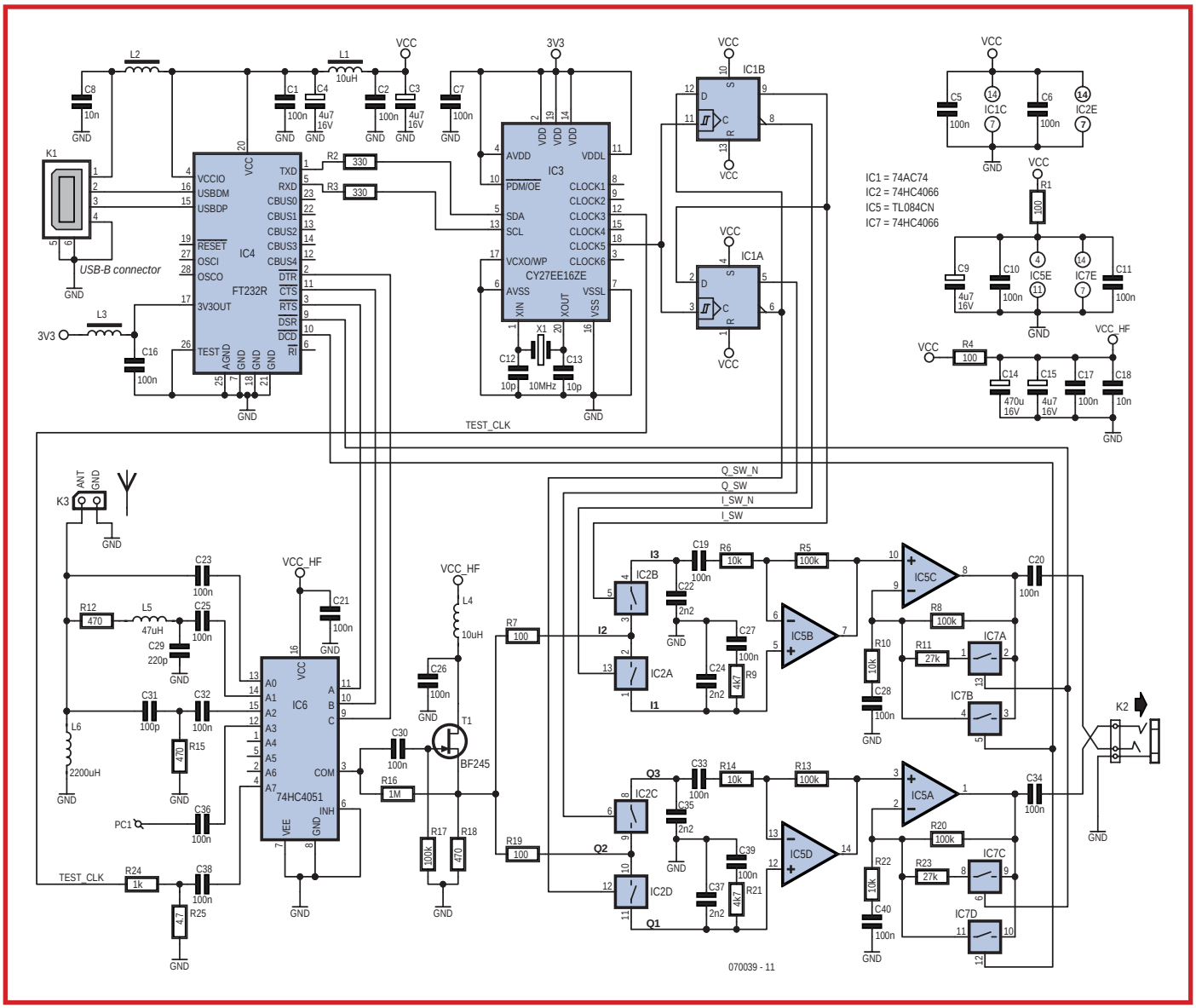


Figure 1. Diagram of the receiver circuit, which in fact comprises just a tuning oscillator and a mixer.

FT232R operates internally at the same frequency range that we are receiving through the antenna downlead and we don't want any of this RF to leak across from one stage to another. That said, the decoupling within the chip itself is remarkably good and the residual RF on the control port lines is barely detectible. Consequently we can control the HC4051 RF input multiplexer direct from the control port lines, without traces of the processor clock appearing in the wanted signal region.
Using its built-in 3.3 V voltage regulator, the FT232R provides the operating supply for the programmable clock generator CY27EE16ZE, avoiding the need for an additional voltage regulator. The rest of the circuit (**Figure 1**) operates exclusively on 5 V. Several different smoothed and filtered voltages are produced, to guarantee good RF decoupling on one hand and to ensure suppression of audio frequency interference on the other. This is particularly crucial at the RF input stage of the receiver, from which the signal is fed via the mixer to the IF circuitry. For this reason a large electrolytic is provided at this point (VCC_HF) to ensure proper 'peace and quiet'.

Programmable VFO

The SDR calls for an oscillator frequency running four times higher than that of the signal received, in order that the necessary phase filtering can be divided by four. If we are aiming to receive signals up to 30 MHz, then the oscillator needs to run right up to 120 MHz. DDS oscillators are very popular in HF projects today but at 120 MHz a DDS is dearer, more power-thirsty and far less controllable. Accordingly we shall look away from DDS oscillators and use a programmable clock oscillator with internal PLL here. Many Elektor Electronics readers will remember the CY-27EE16ZE back from the February 2005 issue. This clock oscillator, developed specially for digital applications, performs equally well in RF circuitry. The frequency resolution does not quite match that of a DDS but the phase accuracy of the output signal achieves comparable results. Restricting power consumption to a relatively modest amount is important with this project, since we must not draw too much current from the USB port.
The chip is programmed over the I²C-Bus using lines SCL and SDA. The internal VCO operates in the frequency range 100 to 400 MHz, stabilised by means of the 10-MHz crystal and a PLL. Its output signal then goes via counters to the desired outputs. Here we select the clock output Clock5, where a VFO signal between 600 kHz and 120 MHz is available for further processing in the 74AC74 counter.
The principle of the I-Q mixer has been described already in Elektor Electronics 12/2006. A two-stage mixer is created here from a total of four analogue switches inside an HC4066 IC. This is controlled by two phase-shifted oscillator signals, which themselves are produced with a 74HC74 counter. Supposing the programmable clock oscillator produces 24 MHz, then the mixer would need a drive of 6 MHz. The receiver would in this case operate in a region of around ±24 kHz either side of the centre frequency of 6 MHz.
Vital here is a phase shift of exactly 90 degrees between the two oscillator signals. Any deviation will lead to reduced suppression of the image frequencies. A 74HC4053 or 74HC4052 integrated changeover switch device would not make a good choice for the analogue switch because the signal transit delays in the internal decoders would then cause different phase errors to appear in every frequency range. Our chosen solution using the rather more basic switches of an HC4066 retains all four phases in sync. Since the 74AC74 counter is configured as a synchronous counter we would not expect to find any phase errors here either. In fact the receiver displays image frequency suppression of around 40 dB up to 15 MHz or so, although this value decreases beyond about 20 MHz (which we can tolerate given that these frequencies are not so heavily occupied).

Signal processing

The receiver is provided with several inputs, selected by the 74HC4051 input multiplexer (IC6). The antenna input ANT is fed by way of filters to the first three inputs. The first switch setting (wideband) uses only one input choke (L6), which shunts any audio frequency signals at the input to ground. In the second position (Medium Wave) there is a low-pass filter with a boundary frequency of 1.6 MHz, using resistor R12 to attenuate excessive resonance. This filter suppresses interference to medium wave reception from overtone mixing with stations in the short wave range. The third position makes use of a simple R-C high-pass filter to attenuate strong medium wave signals.
An additional input (PC1) can be selected if you wish to connect external tuned input circuits or preamplifiers. Finally three more inputs are provided for future developments. The input filters on the printed circuit board are good to be getting on with and are certainly adequate for most applications. You can of course introduce steep low-pass filtering ahead of the filters provided if you want to be certain of blocking out overtone mixing in every possible situation. Or you might choose to fit different resonant circuits, selected by input switching.
The particular input that is active at any given time is connected to the common output COM (pin 3). Coupling capacitors are provided either side of the switch. A bias voltage of about 2.5 V is provided to the switch from the source connection of the BF245 via a 1-megohm resistor. This eliminates any distortion from large input signals that might arise when signals are limited by the protection diodes on the analogue inputs to the ICs.
Input A7 delivers a calibration signal from Output 3 (Test-Clk) of the programmable crystal oscillator. The oscillator produces a square-wave signal of 3.3 V peak-to-peak at 5 MHz. A signal voltage of around 5 mV at 5 MHz is produced at the voltage divider, corresponding to a signal strength of S9 + 40 dB. This enables the field strength meter created in software to be calibrated without any further expenditure.
JFET BF245 on the output of the input multiplexer serves as an impedance transformer. This provides a relatively high impedance termination of 100 kΩ for the RF signal, enabling for instance a high-Q resonant circuit to be connected even to input In2. At the low-impedance output of the source follower we arrange to have a voltage of circa 2.5 V, fed via the mixer and the following op-amp all the way to the output. It is important that no audio frequency signal remnants appear at the source connection and for this reason the 'critical' supply Vcc_HF is also filtered very thoroughly. The FET itself provides additional decoupling of the supply voltage, but we don't want any signal escaping from the Gate either that might fall in the IF region below 24 kHz. This is why an RF choke is connected directly to the antenna input, to shunt for instance any 50 Hz mains hum signal.
Leading off from the Source connection are two 100-Ω resistors that go to the two mixers for the I and the Q signals.

COMPONENTS LIST

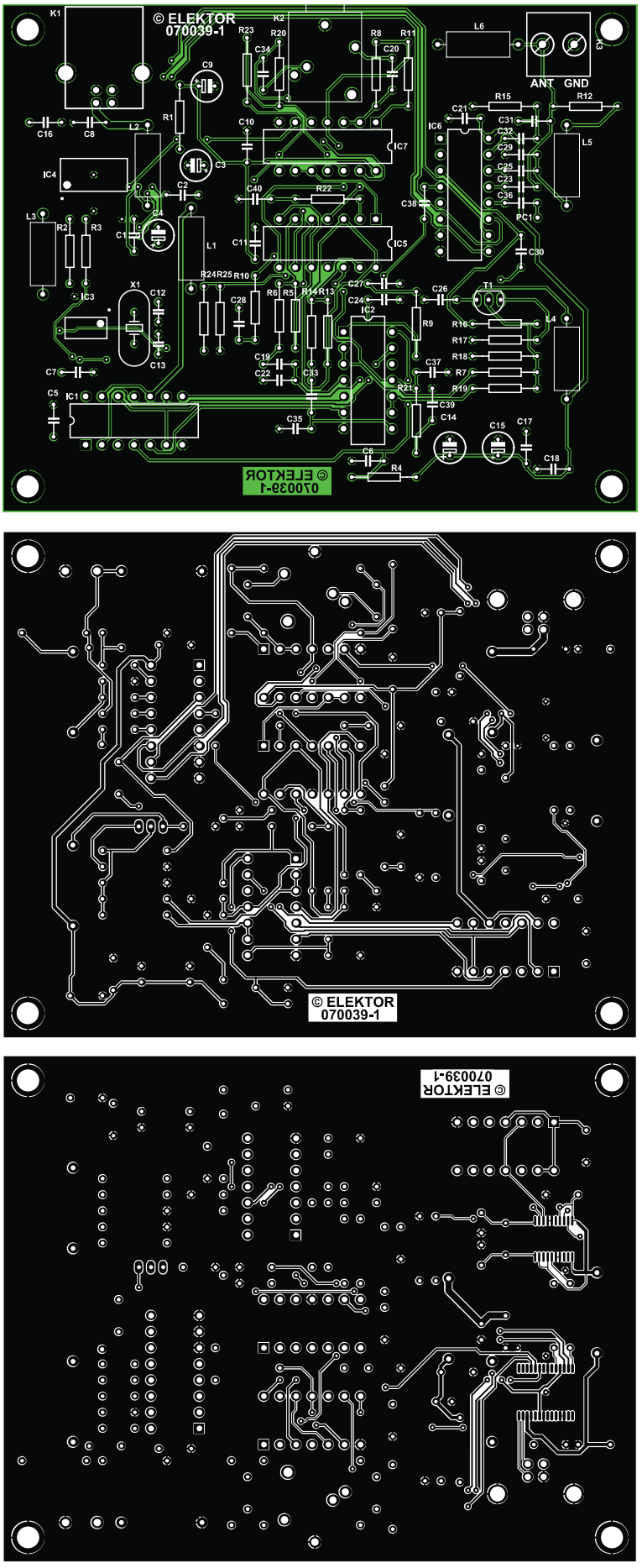
Resistors
R1,R7,R19 = 100Ω
R2,R3 = 330Ω
R4 = 100Ω
R5,R8,R13,R17,R20 = 100kΩ
R6,R10,R14,R22 = 10kΩ
R9,R21 = 4kΩ7
R11,R23 = 27kΩ
R12,R15,R18 = 470Ω
R16 = 1MΩ
R24 = 1kΩ
R25 = 4Ω7

Capacitors
C1,C2,C5,C6,C7,C10,C11,C16,C17,C19,C20,C21,C25-C28,C30,C32,C33,C34,C36,C38,C39,C40 = 100nF
C3,C4,C9,C15 = 4μF7 16V radial
C8,C18 = 10nF
C12,C13 = 10pF
C14 = 470μF 16V radial
C22,C24,C35,C37 = 2nF2
C29 = 220pF
C31 = 100pF

Semiconductors
IC1 = 74AC74
IC2,IC7 = 74HC4066
IC3 = CY27EE16 (Cypress)
IC4 = FT232R (FTDI)
IC5 = TL084CN with socket (see text)
IC6 = 74HC4051
T1 = BF245

Inductors
L1-L4 = 10μH
L5 = 47μH
L6 = 2.2mH

Miscellaneous
K1 = USB-B socket, PCB mount
K2 = stereo jack socket, 3.5mm, PCB mount
K3 = 2-way PCB terminal block, lead pitch 5mm
PC1 = solder pin
X1 = 10MHz quartz crystal
Ready-populated and tested PCB, order code 070039-91
Project software, free download 070039-11
Supplementary document, free download
PCB, bare, ref. 070039-1 from www.thepcbshop.com



They improve the symmetry of the mixers, the 'on' resistances of which let through a certain amount of leakage. The mixers themselves are HC4066 analogue switch ICs ganged as changeover switches. The voltage of these too is set around 2.5 V, allowing them to be controlled without overdriving up to about 5 V peak-to-peak.
The IF amplifier consists of two exact-

Figure 2. The SDR receiver board.

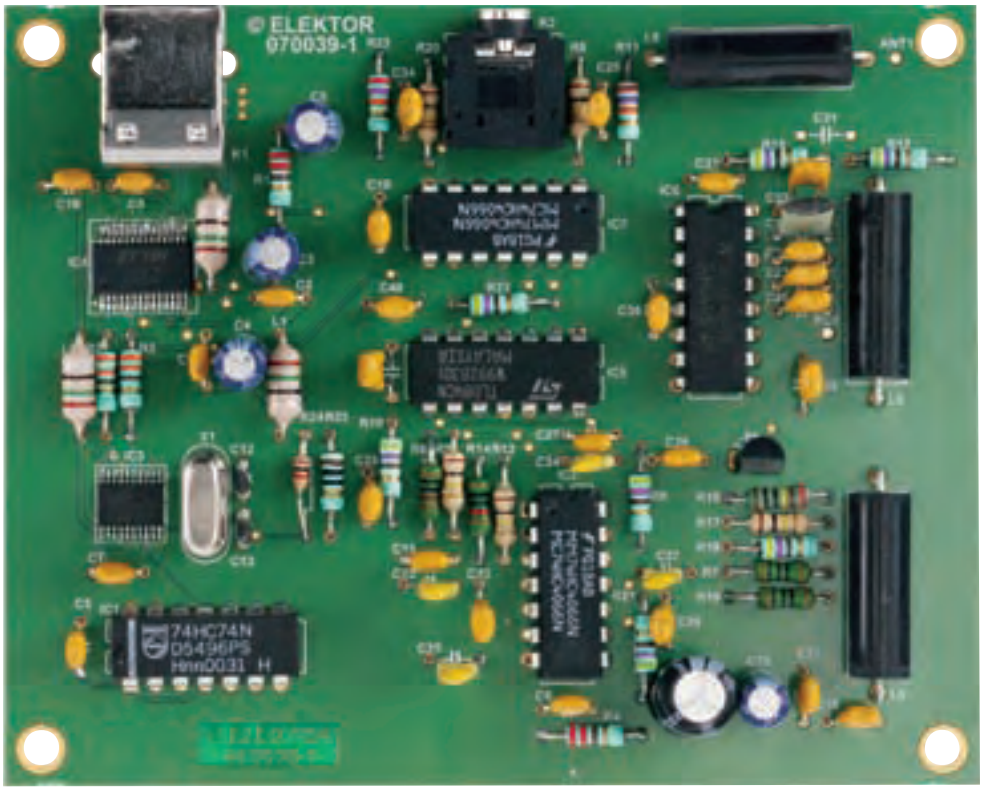


Figure 3. This lab sample board is not quite equivalent to the production version supplied through the Elektor SHOP.

ly equal branches that together produce an attenuation of up to 40 dB at all times. When you are using 5 V supplies, the gain bandwidth (GBW) of the selected op-amp is important, in order to achieve tenfold amplification without phase errors for signals around 20 kHz. In the author's test samples a TL084 turned out to be adequate. If you provide a socket for IC5 you will be able to try other, faster op-amps.

The input stage works as a differential amplifier. In dimensioning the resistors what we are looking for is not the best common-mode suppression but rather an input resistance that's as equal as possible across the inverting and non-inverting inputs. Tests show that good phase accuracy (and consequently high image-frequency suppression) depend on equal impedance existing on all four phases of the mixer. The input impedance amounts to around 5 kΩ at all of the inputs. Note the load resistance of 4.7 kΩ on the non-inverting input as opposed to 10 kΩ on the inverting one. This is correct, since signal transit on this input gets dispersed in exact antiphase by inverse feedback, halving the input resistance to 5 kΩ. In this way both inputs offer the same input resistance as close as matters.

The 2.2 nF capacitors together with the mixer's internal resistance and the 100 Ω series resistors form simple low-pass filters with a limiting frequency of over 100 kHz, so as to keep remnants of RF well away from the audio frequency stages. The limiting frequency lies far above the transfer frequency range, meaning that capacitor tolerances do not produce any discernible phase errors. You can use even ceramic disc capacitors here. Tolerances between 10 and 20 % are not a problem with any of the capacitors in the signal path acting as high-pass elements with a limiting frequency of around 300 Hz.

The final stage has a tenfold gain (20 dB), which can, however, be reduced to unity gain by the analogue switches. A total of three attenuation steps are provided: 0 dB, –10 dB und –20 dB. To avoid it being driven too hard, the gain can be reduced in software. As the receiver's input displays high resistance to being overdriven the attenuator is placed in the final stage, so as to prevent overdriving of the output. This corresponds to gain control in an IF amplifier.

Construction

The printed circuit board shown in **Figure 2** uses standard wire-ended components as far as possible, with the exception of the LSI (large scale integration) chips FT232RL and CY27EE16, which unfortunately are available only in SSOP case format with a pin spacing of 0.65 mm. **Figure 3** shows the laboratory prototype PCB with components fitted.

The best way to begin is by soldering the two surface-mount device (SMD) chips in place. It pays to start first at the four corners, before soldering all the other pins generously. Superfluous solder can be removed with desolder braid, followed by thorough checking with a magnifying glass to avoid unwelcome surprises later on.

The components with wire leads will present no difficulty. The circuit does not call for any special RF components or test points. Capacitors C12 and C13 should not be fitted initially. The CY27EE16 has presettable internal capacitors that should enable you to achieve a frequency of exactly 10 MHz without difficulty. C12 and C13 will be needed only if the crystal used requires greater loading capacity.

Once all construction is complete you need to make a quick round-up with a multimeter checking for any short circuits around the USB connections, as you certainly don't want to damage the PC.

Hook-up and alignment

Before connecting the receiver to the computer's USB port for the first time you will need to install the driver software for the FT232R. You can find this on the manufacturer's website (www.ftdichip.com/FTDrivers.htm) or alternatively in the software download for this article. Installation using CDM_Setup.exe automatically removes any traces of older FTDI drivers on your computer. After this has been done Windows will find the correct driver automatically as soon as the receiver is connected. The same process provides the PC automatically with an additional virtual COM-port interface. For this you do not even need to know which COM number is allocated to the device, as it effectively sets up its own direct connection to the FT232R. FTD2XX.dll controls the eight data lines of the chip as for a parallel port, eliminating at the same time all timing problems. To save time the multiple level changes involved in controlling the I2C bus are loaded conveniently into a buffer and then fed out to the data lines in short order. The program ElektorSDR.exe enables you to control all functions of the receiver (**Figure 4**) and can be found in the download archive as an executable file together with the Delphi source code. Also available for download is a supplementary .pdf document that describes initialisation and commissioning.

Decoder software

Nearly all significant characteristics of the receiver are determined by settings in the decoder software on your PC. As the survey in [1] indicates, there are a number of different programs to choose from. You could perform your first test with SDRadio [2] for example. After this you will discover additional possibilities in DREAM [3] or G8JCFSDR [4]. Whichever program you select, it's vital to set up the sound card correctly (this is described in the supplementary document). Information on the programs can be found on the relevant Web pages and in the Elektor Electronics articles listed below. Further advice may be found on the author's homepage (www.b-kainka.de) and will appear also in due course on the project page at www.elektor-electronics.co.uk and, if necessary, in the Forum on the same website.

(070039-1)

Figure 4. Elektor Electronics SDR Tuning control program.

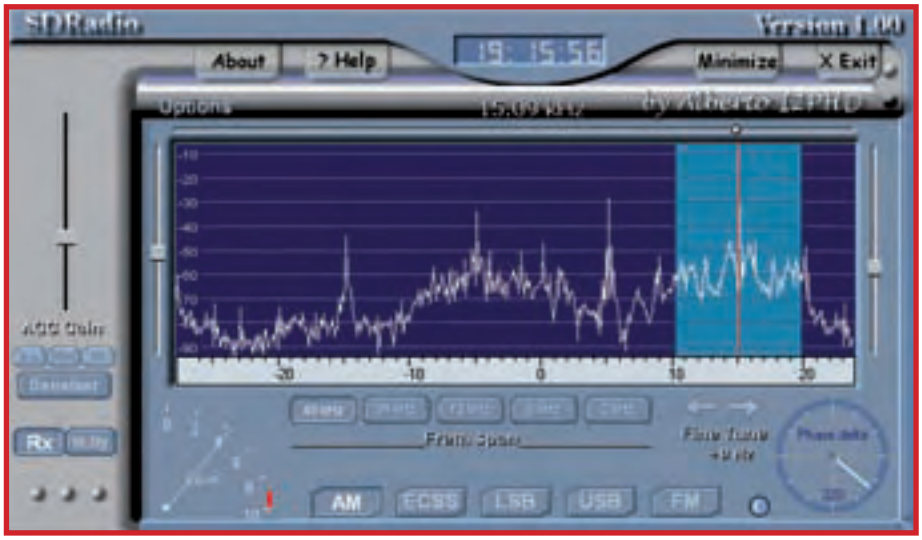


Figure 5. Four AM stations in tuning range spectrum, as displayed by the SDRadio program.

Web links:

[1] www.nti-online.de/diraboxsdr.htm

[2] www.sdradio.org/

[3] http://sourceforge.net/projects/drm

[4] www.g8jcf.dyndns.org/

Literature:

Burkhard Kainka: DREAM Team –Software for DRM reception, Elektor Electronics 4/2004, pp. 20 ff.

Wolfgang Hartmann and Burkhard Kainka: 'Radio listening with Matlab—Diorama software DRM receiver', Elektor Electronics 4/2006, pp. 76 ff.

Burkhard Kainka: I-Q: a highly intelligent approach to quality radio, Elektor Electronics 12/2006, pp. 38 ff.