

PLL forms simple MSK demodulator

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n minimum-shift-keying (MSK) signaling, two frequencies that differ by the bit rate represent a one bit and a zero bit. Normally, the frequency shift occurs at the peak of a cycle, so that neither the amplitude nor the slope of the waveform shows a discontinuity. We needed to transmit 300baud ASCII text using ultrasonic transducers. These devices have a very narrow bandwidth around their 25-kHz resonant frequency, making MSK the obvious choice for modulation. A zero bit becomes

84 cycles of 25.2 kHz, and a one bit

is 83 cycles of 24.9 kHz. It is easy to generate this signal with a PIC μ C and an 8-bit DAC. However, a traditional MSK demodulator circuit uses a center-frequency VCO and several mixers and filters. This design needs something simpler: to wit, the circuit in **Figure 1**.

Because the transmitter sends 25.2 kHz between characters, the design phase-locks a 74HCT4046 PLL chip to this frequency. The chip has three phase detectors, each with different characteristics. By choosing the correct two, you can demodulate the MSK input without losing phase lock on the zero-bit carrier. Phase Detector 3 on the PLL chip has a 360° linear range. That is, its mean output varies from 0 to 5V and then switches back to 0V as the phase passes through 360°. Adjust the frequency of the PLL chip so that it locks to 25.2 kHz

with a 180° phase error and an output of 2.5V. If the oscillator frequency remains fixed, then you can recognize a one bit by its phase error, which swings from 0 to 360° during the bit.

Because the initial lock is at the 180° point, a one bit results in a phase error that goes from 180° down to 0°. It then jumps



The ASCII input character for the letter "g" (a) produces a frequency-varying MSK signal (b). The phase error as seen by the loop (c) produces the phase-error signal at TP (d) that drives the output.



A PLL makes MSK demodulation inexpensive and easy.



to 360° and continues back down to 180°. The net result is a ramp that goes down to 0V, a jump to 5V, and then another downgoing ramp. The mean voltage is 2.5V. Because the loop bandwidth is approximately 15 Hz, the instantaneous effect on the VCO is small, and the net frequency change is zero. Rather than detect the ramp-jump-ramp waveform, use Phase Detector 1 as the data output. Because this block is a simple exclusive-OR gate, each one bit appears as a spike going from 5 to 0V and back. A comparator can change it into a return-to-zero version of the input signal. Alternatively, the output can go to a retriggerable monostable with a 3.5-msec

period to generate a good approximation of a nonreturn-to-zero output. **Figure 2** shows the circuit waveforms that occur for the letter "g." (DI #2284).

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