DACs are Optimized for Communication *Transmit* Path

High-speed CMOS TxDAC™ 8-to-14-bit family with clock rates up to 125 MSPS

by Doug Mercer and Joe DiPilato

The pin-compatible AD976x family of 8-, 10-, 12-, and 14-bit TxDAC™ low-distortion DACs offers excellent spurious-free dynamic range (SFDR) specs at clock rates of up to 125 MSPS with the low price and power levels typical of CMOS devices.

The rapidly expanding consumer-oriented wireless and wireline communications markets have fostered an insatiable demand for high-speed analog-to-digital and digital-to-analog converters having good dynamic (frequency-domain) performance at low cost and with low power dissipation. The most visible manifestation has been the feast of new CMOS ADC offerings developed to meet the needs of the *receive* path; but there's been a lack of choice of low-cost CMOS DAC products with dynamic performance suitable for many *transmit* signal-path applications.

Traditional time-domain and dc linearity characteristics, such as integral nonlinearity (INL), differential nonlinearity (DNL), glitch impulse, and settling time are not adequate indicators of response and distortion in the frequency domain. Most existing high-speed CMOS DACs, developed primarily for video applications, tend to have poor spurious-free dynamic range (SFDR) and harmonic distortion (THD). Bipolar and BiCMOS devices can provide the required dynamic performance, but they are usually too costly, require dual supplies, and use too much power to be suitable for tomorrow's high-volume communications applications.

The low-power requirement is driven by communications-platform changes. They are either getting physically smaller and require higher component packaging density (e.g., micro and pico basestations packaged in small boxes that hang off telephone poles and sides of buildings); or are portable and battery-operated (for example, telephones, pagers, meter-reading terminals, etc.); or are powered by telephone lines (wireless local loop); or require battery back-ups (telephony over cable, life-line services). These requirements all dictate low power for extended battery life, minimized heat dissipation, and ability to operate with limited power available. In this regard, single-supply components avoid the cost and inefficiency of additional supplies. 3-V single-supply devices are becoming very popular to achieve even lower power dissipation and compatibility with high density digital circuits.

These requirements for low cost and low power with good dynamic performance have led to the development of a new class of high-speed CMOS DACs for transmit applications. This new low-cost TxDAC™ family, specified to operate at update rates of up to 125 MHz, represents a major break-through for high-speed transmit-path CMOS DACs. They offer SFDR performance that, until now, was simply unobtainable with high-speed CMOS DACs.

The first five members of the TxDAC family include the *8-bit, 50-MSPS* AD9708AR; the *10-bit, 50-MSPS* AD9760AR-50; the *10-bit, 125-MSPS* AD9760AR; the *12-bit, 125-MSPS* AD9762AR; and the *14-bit, 125MSPS* AD9764AR. All five models are offered in pin-compatible 28-pin SOIC packages, allowing designers to make easy price/performance trade-offs during the evaluation stages of the design cycle. Figure 1 shows a functional block diagram of the 12-bit AD9762 and the pin-out of the 10-bit AD9760. The MSB (DB *N*–1) is always pin-1 in this family, irrespective of the resolution; lower-resolution devices can be directly connected to circuits wired for higher-resolution devices. This permits a uniform design footprint and the direct swapping of different-resolution models for comparison, upgrading, and downpricing.

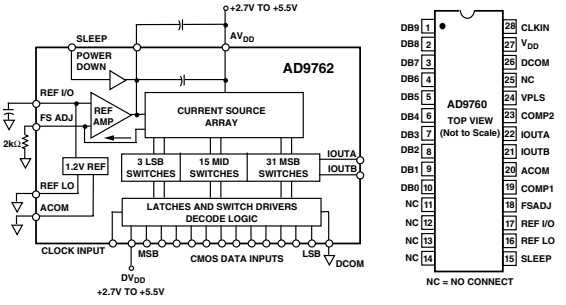

Figure 1. AD9762 block diagram and AD9760 pinout.

These devices are fabricated on a low-cost sub-micron single-polysilicon double-metal CMOS process. Each DAC's analog and digital circuitry can operate from single +2.7 V to +5.5 V supplies (providing full 3-V, single-supply operation). Each DAC includes a temperature-compensated 1.2-V band-gap reference and provides differential current outputs up to 20 mA full-scale (compliance voltage = 1.25 V), regulated by an on-chip reference amplifier, and settable anywhere from 2 mA to 20 mA, using an external resistor. The DAC outputs settle to within 0.25% of final value within 35 ns. Rise and fall times from 10% to 90% of full scale are specified at 2.5 ns, and output propagation delay is only 1 ns.

DESIGN FEATURES

To eliminate amplitude-dependent distortion associated with traditional R-2R ladder architectures, and for superior ac and dc performance, the TxDACs employ segmented current sources. For example, at the core of the 12-bit AD9762 are 49 current sources (Figure 1). The 5-most-significant-bits' contribution to the output is formed by summing up to 31 equal current sources, each having a weight of 2^{-5} FS. The contribution of the next four bits is provided by summing up to 15 current sources with 1/16th the weight of the first set (i.e., 2^{-9} FS each). The 3 LSBs are formed by a more-or-less conventional 3-bit binary DAC switching currents with weights of 1/2, 1/4, and 1/8 of the second set. This segmentation architecture is the key to the AD9762's achieving its ±0.5 LSB 12-bit DNL performance and its low 5 pV-s output glitch-impulse spec, as well as its excellent SFDR in multi-tone applications, where the output of the DAC is normally operating at 1/2 or 1/4 full-scale. Figure 2 shows AD9762's single-tone SFDR vs. output level at various rates.

For use in the *transmit* path of communications applications, the segmented current-source architecture was by itself insufficient to achieve the required SFDRs. To reduce the inherent causes of ac distortion, especially even harmonics, intense design effort was focused on improving output switch timing. The resulting innovative proprietary latch and switch circuitry has produced an SFDR increase of approximately 20 dB over traditional CMOS "video" DAC offerings. What's more, the TxDAC family's SFDR performance is comparable to that of the best bipolar and BiCMOS IC devices, but at a fraction of the power and price.

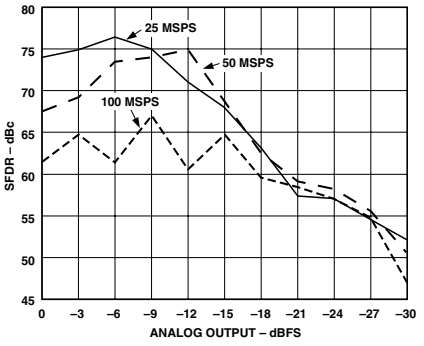

Figure 2. SFDR vs. output amplitude at various sampling rates.

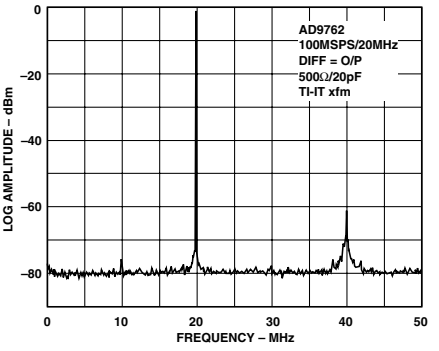

Figure 3. 19.96-MHz sine wave sampled at 100 MSPS; differential output, 50 Ω, 20 pF, SFDR = 60.8 dB.

SPURIOUS-FREE DYNAMIC RANGE

Why is SFDR important in communications? Usually, the information being transferred shares the frequency spectrum/bandwidth with other communication channels and applications (for example, different television channels being broadcast or transmitted by a common cable, different callers in a cellular system, different FM radio stations, etc.) If a transmitter sends spurious signals into other frequency bands, they can corrupt, interrupt, or obliterate the neighboring signal(s). This is considered to be bad practice, is counter to the regulations of the FCC (and other regulatory bodies), and can lead to legal action.

The TxDAC family has SFDRs over the Nyquist band upwards from 57 dB, when clocked at 100 MSPS and producing a 40-MHz output signal (10-bit AD9760), to 78 dB, when clocked at 20 MSPS and producing a 2-MHz output (14-bit AD9764). Table 1 shows typical SFDR and THD specifications for the AD9760, AD9762, and AD9764 at various clock rates and output frequencies. Though the 12- and 14-bit devices offer similar SFDR for full-scale sine waves, the higher-resolution devices have better SFDR for signals with high peak-to-average ratios and significant low-level content. Figure 3 demonstrates a typical spectral plot over the Nyquist range of the 12-bit AD9762 with an output consisting of a single 20-MHz signal at a 100-MSPS clock rate; shown is a –60.8-dB second harmonic, with the remaining spurs <–75 dB. In most narrow-band applications, the harmonics are filtered out, and the SFDR within "a window" or "without harmonics" is what matters. In this case, the TxDAC family offers performance in the 80-dB range, even for the 10-bit AD9760, for outputs in the 5-MHz range clocked at 100 MSPS.

In wideband applications, where the DAC will be producing several signals at its output, two-tone or multi-tone performance is of especial interest. A salient application is where two or more data/voice/video channels are simultaneously sent down a cable. Wideband cellular basestations is another, and beyond that there are applications like ADSL (Asymmetric Digital Subscriber Line), which utilize discrete multi-tone based modulation schemes and depend on good multi-tone performance.

Table 1. Typical SFDR and THD specifications

SFDR	**AD9760**	**AD9762**	**AD9764**
F_c=50 MHz; F_{out}=5.05 MHz to Nyquist	67 dBc	70 dBc	70 dBc
F_c=50 MHz; F_{out}=20.2 MHz to Nyquist	64 dBc	67 dBc	67 dBc
F_c=100 MHz; F_{out}=5.05 MHz to Nyquist	61 dBc	64 dBc	64 dBc
F_c=100 MHz; F_{out}=40.4 MHz to Nyquist	57 dBc	60 dBc	60 dBc
F_c=50 MHz; F_{out}=5.05 MHz; 2 MHz Span	84 dBc	84 dBc	84 dBc
F_c=100 MHz; F_{out}=5.05 MHz; 2 MHz Span	84 dBc	84 dBc	84 dBc
THD			
F_c=50 MHz; F_{out}=5.05 MHz	–61 dBc	–64 dBc	–64 dBc
F_c=100 MHz; F_{out}=5.05 MHz	–57 dBc	–60 dBc	–60 dBc

In most multi-tone applications, the output of the transmit-path DAC is normally operated at a fraction of the full-scale range (e.g., 1/2 or 1/4 FS), to ensure that the DAC output doesn't clip with all channels near full-scale (the harmonics produced by clipped transmit waveforms can result in illegal "splatter"). Figures 4 and 5 show spectral plots of an 8-tone waveform at full scale and half-scale, respectively, for the AD9764; both indicate SFDRs > 70 dBc—an important result of the innovative converter architecture. Various models of the TxDAC family have been measured against BiCMOS DACs performing comparably in single-tone tests; the TxDACs achieve repeatably better performance in multi-tone applications. This can be linked to timing skew attributed to the widely used R-2R ladder-network architecture—skews which the TxDACs' proprietary current-switching architecture has been optimized to minimize.

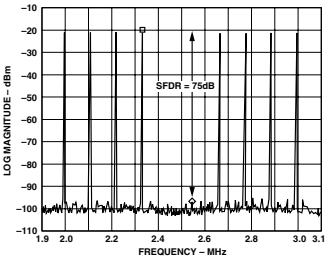

Figure 4. AD9764 8-tone FFT plot, at full-scale output.

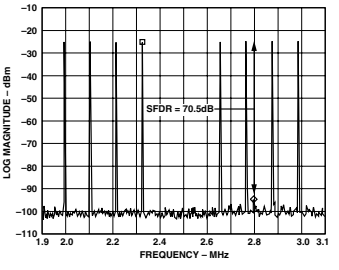

Figure 5. AD9764 8-tone FFT plot, at 1/2-scale output.

The switching circuitry used in the TxDAC core provides true differential outputs, for improved performance when the devices are used differentially. Even though the TxDAC families' single-ended performance is outstanding in its own right, the best possible harmonic performance is achieved when the outputs are driven differentially through a transformer. Table 2 demonstrates the improvement in differential performance over single-ended for the 12-bit AD9762, especially at higher frequencies.

Table 2. AD9762 Spurious-Free Dynamic Range, Fs = 125 MSPS

One Tone	**Single-Ended**	**Differential**
1 MHz	70 dBc	72 dBc
5 MHz	63 dBc	70 dBc
10 MHz	58 dBc	65 dBc
39 MHz	46 dBc	54 dBc

Each DAC consumes 150 mW when powered from a single +5-V supply and clocked at 100 MSPS, while configured for a 20-mA full-scale current output. The dissipation is reduced to a very low 35 mW when clocked at 40 MSPS, operating from a single +3-V

supply, and configured for 2-mA full-scale output. Each device supports a *sleep* mode, reducing power consumption to < 30 mW (from +5 V) when the DAC is not in operation.

In many cases, the figure of merit in a digital communications system is its bit-error rate (BER). The BER is usually dictated by the appropriate standard/specification, and is affected by a combination of analog component performance, transmission medium, modulation scheme, data rate, and available equalization and error-correction circuitry. The variety of different wireless and wireline applications (including wireless base stations and terminals for cellular, PCS, pager, wireless local loop and satellite services, and wireline modems for Internet access, interactive video set-top box, and digital subscriber lines such as ADSL, HDSL, VDSL, etc.) use many different modulation schemes, accommodate different data rates, and require differing system-level performance.

In these circumstances, the lack of a unique relationship to DAC performance makes it difficult for a communications system designer to establish the converter's required resolution/dynamic range. Fortunately, the TxDACs' pin-compatible footprint permits price-performance trade-offs at any stage of the development cycle, and provides an upgrade path to future higher-performance systems. The system designer has the flexibility to trade off BER performance for system cost. The choice permits the designer to accommodate a certain margin of error, compensating for equalization and error-correction methods and performance. Also, since data rate for a given modulation scheme is proportional to bandwidth and dynamic range, a designer can provide for increased data rates on higher-end devices.

Two basic transmit architectures are shown in Figures 6 and 7. In quadrature-based modulation schemes, such as QPSK and QAM, mixers are deployed to mix the in-phase (I) and quadrature (Q—90 degree out of phase) signals into a composite single-sideband signal for transmission. Figure 6 demonstrates a baseband transmit architecture that performs an *analog* mix of the I and Q signal. In this example, two DACs are required per transmit channel. Even at the low output frequencies used in many baseband applications, the TxDAC family are the best choice because all family members combine (1) high SFDR at low output frequencies; (2) low power consumption, single supply and 3-V operation to enhance system power efficiency; (3) competitive pricing (overall cost can be further reduced by oversampling the signal (interpolation) to reduce the DACs' in-band aliased images, thus easing the job of the low-pass filter); and (4) the variety of resolutions offered in the same pin-out allows ultimate cost/performance trade-offs. For example, in many of the TxDAC beta-site applications, users started with one resolution model and later designed-in either a higher- or lower-resolution device based on actual system performance.

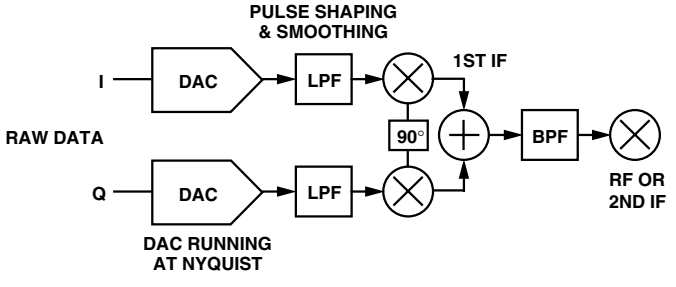

Figure 6. Baseband transmit architecture with analog quadrature mixing.

The system architecture in Figure 7 uses *digital* mixing of I and Q signals and inputs the modulated signal directly to a single DAC. In this case, the bandwidth requirements of the DAC are more stringent. With digital modulation, intermediate frequencies (IFs) in the range of 40 MHz can be generated via TxDAC chips. This is adequate for directly transmitting data in high-speed modems and upstream information in interactive set-top boxes. In other applications, it could eliminate an up-converter stage. Here, too, high SFDR, low price, low power, and family pin-compatibility are desirable (required) attributes. If multiple digital I&Q modulators were fed into the single DAC depicted in Figure 7, the system would correspond to a wideband transmit architecture, for which the superior multi-tone performance of the TxDAC family of products is a major performance attribute.

The 10-bit AD9760s are finding their way into high-speed Internet data modems and interactive set-top boxes where the SFDR requirements are in the 50 dB range, at 40 MHz output frequencies, clocking at rates of up to 120 MSPS. They are also being used in wireless local loop and high speed wireless trunking basestations. The 12-bit devices are being designed into cellular and personal communication service (PCS) basestations, cable head-end equipment, and hybrid fiber coax modems, where SFDRs of up to 70 dB are required at various clock and sample rates. The 14-bit AD9764 is finding a home in ADSL modems and next-generation PCS basestations where > 70 dB is desired for 1-MHz to 6-MHz signals at clock rates of < 15 MSPS.

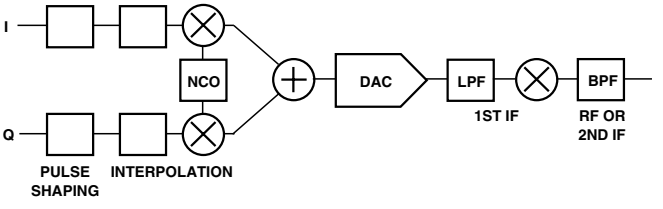

Figure 7. Transmit architecture with digital modulation.

A major benefit of chip design for plain-vanilla CMOS fabrication is digital integration compatibility. The TxDAC core, optimized on a *CMOS* process, enables efficient integration with digital-signal-processing (DSP) circuitry for additional board and cost savings, with enhanced performance capabilities and reliability. By integrating digital processing with the DAC core, higher-speed digital switching can be accomplished than ever before possible.

For example, in traditional two-chip direct digital synthesis (DDS) systems, using a digital DDS engine and a high-performance (bipolar) DAC, speed and resolution are limited by the speed and power required to clock the digital data out of the DDS chip into the DAC (TTL logic is limited to about 100 MSPS). By integrating the DDS circuitry with the DAC, internal data rates > 200 MSPS will be usable and economical. Besides single-chip high-performance DDS (see page 12), future on-chip digital circuitry will include digital modulators and interpolation filters.

The TxDAC family* products are packaged in 28-pin SOICs and are specified for –40 to +85°C. Evaluation boards are available. Prices (1000s) start at $7.84 for the AD9760AR-50, $12.54 for AD9760, $18.85 for AD9762, and $22.62 for AD9764. Evaluation boards for all models are priced at $150.

The TxDACs were designed by Analog Devices Fellow Doug Mercer at our facility in Wilmington, MA. A

*For technical data, consult our Web site, **http://www.analog.com, or circle 1**