Locate stations quickly & accurately

Digital readout for shortwave receivers

Want to add digital frequency readout to an AM radio or shortwave communications receiver that uses an old-fashioned analog dial? This unit features a bright four-digit LED display, 1kHz resolution, and a 0.2s update time that's fast enough to follow the tuning knob.

by JOHN CLARKE and GREG SWAIN

With today's crowded radio bands, a digital frequency readout is virtually a necessity. A digital readout not only provides an accurate indication of the tuned frequency, but also enables the operator to quickly locate stations of a known frequency.

In addition, the reading provided by a digital display is totally unambiguous, an important factor when listing to a multi-band shortwave receiver. The plethora of scales often found on analog dials can easily lead to an erroneous frequency reading, particularly when one's attention is concentrated on reception.

The "Digital Tuner Readout" to be described here can be used to update existing AM superhet receivers, or can provide a modern display for a home-built receiver. Two versions can be built: a 30MHz version suitable for use with communications receivers; and a 9.999MHz version for use with broadcast-band AM tuners. Only two connections are required to the receiver, one to the local oscillator and the other to ground.

Regardless of the version built, the Tuner Digital Readout has little effect on receiver performance. In fact, the only noticeable effect is due to the small loading on the local oscillator, causing it to shift frequency slightly. This will cause the tuning dial on the receiver to be slightly off scale but, since we are now using the digital readout, this will be of little consequence.

Resolution of the four-digit display is 1kHz over the full range of frequencies to 30MHz. For frequencies above 10MHz, the unit overranges and the most significant digit is not displayed when the range switch is set to the divide by one position. The most significant digit can be displayed simply by switching to the divide by 10 position, which gives a resolution of 10kHz.

Decimal point switching is employed in the design so that the display always indicates the tuned frequency in MHz. This facility is unnecessary if the unit is to be used only with a broadcast-band tuner.

By now, some readers will be wondering why our design appears to be so complicated. After all, why use 19 integrated circuits when an LSI chip (such as the AY-3-8112 as used in the Playmaster AM-FM Tuner-Clock) is

The Tuner Digital Readout can be used with broadcast-band AM tuners and communications receivers.

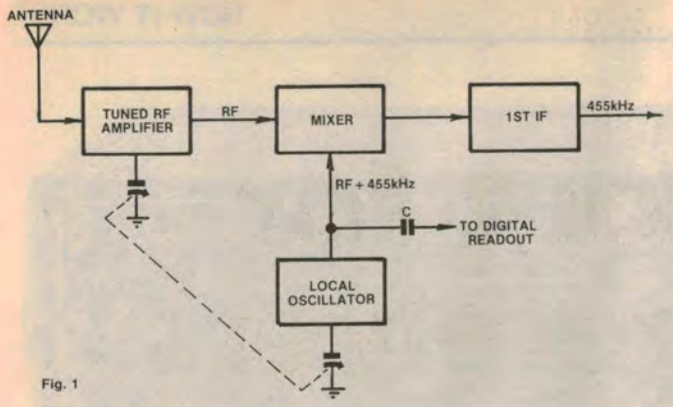


Fig. 1

Basic scheme for a superhet receiver front end. The local oscillator frequency is always 455kHz higher than the tuned signal frequency.

SPECIFICATIONS

RANGES (FULL SCALE)	0-10MHz and 10-30MHz (optional).
DISPLAY	Four digit.
RESOLUTION	1kHz with division switch set to divide by one; 10kHz with division switch set to divide by 10.
SENSITIVITY	Less than 100mV from 500kHz to 30MHz.
OFFSET FREQUENCY	Prototype set to 455kHz, but any offset frequency can be programmed.

available to do the job? The answer is that we have deliberately opted not to multiplex the LED displays, since this can cause noise problems within low signal circuitry of the accompanying tuner.

In short, the advantages of multiplexing have been rejected in favour of tuner performance. And while 19 ICs may sound a lot, the devices used are all low in cost and readily available.

Other advantages of our new design include selectable IF offset, which means that it is adaptable to almost any superheterodyne receiver. By comparison, the AY-3-8112 does not have adjustable IF offset and can only display the tuned frequency in 10kHz steps (later versions possibly have the necessary 9kHz resolution now required by the broadcast band).

At this stage, we should warn readers that the unit is not suitable for use with Wadley loop receivers or the "Electronics Australia" Deltahet receivers. Since the incoming frequency source is derived from the local oscillator, a conventional superheterodyne receiver must be used. This will include virtually all broadcast-band tuners and most general communications receivers.

Superheterodyne tuners

Before discussing the circuit operation, let's first examine the basic principle of a superheterodyne receiver.

Fig. 1 shows the general block diagram of a superhet receiver front end. The antenna feeds signal frequencies to a tuned RF stage, which selectively amplifies the particular tuned frequency. Tuning is commonly achieved by adjusting one gang of the dual-ganged capacitor, the second gang being used to control the local oscillator frequency. Both gangs work in unison, such that the local oscillator frequency is always 455kHz (the most common figure) higher than the tuned signal frequency.

Signals from the tuned RF amplifier and the local oscillator are mixed together in the mixer, the output of which consists of the original frequencies plus sum and difference frequencies. Virtually all superhet receivers reject the sum frequency and filter the 455kHz difference frequency at the first intermediate frequency (IF) stage.

It is important to realise that the tuned RF signal is not a single sine wave but consists of a range of signals centred about the tuned frequency. This range, in combination with various other factors, determines the maximum possible audio bandwidth of the receiver.

The local oscillator provides the only pure sine wave signal and it is this that is used to drive the digital readout, as shown in Fig. 1. However, the digital readout is unusual in that it is not set to zero at the beginning of a count sequence. Instead, it is "offset" (or preloaded), the amount of offset being equal to the intermediate frequency of the receiver being measured.

In other words, the circuit is basically a specialised type of frequency meter which measures the receiver's local oscillator frequency and subtracts the IF to display the actual frequency to which the receiver is tuned.

Block diagram

Fig. 2 shows the general arrangement of the Tuner Digital Readout. Essentially, it can be broken into three parts: input amplifier and divider chain to process the local oscillator signal; a crystal-controlled timebase; and a counter section.

As shown, the local oscillator input frequency is amplified and then divided by either 100 or 1000, depending upon the position of the division switch. A 4MHz crystal-controlled oscillator forms the timebase, which is divided by 80,000 to obtain a 50Hz clock signal. This 50Hz clock signal is then fed to a timing circuit to derive a 5Hz gating signal plus control signals for the counter, latch and preload circuitry.

When the division switch is in the divide by one position, the counter is preloaded with 9545, which is the appropriate offset for a 455kHz IF. Why

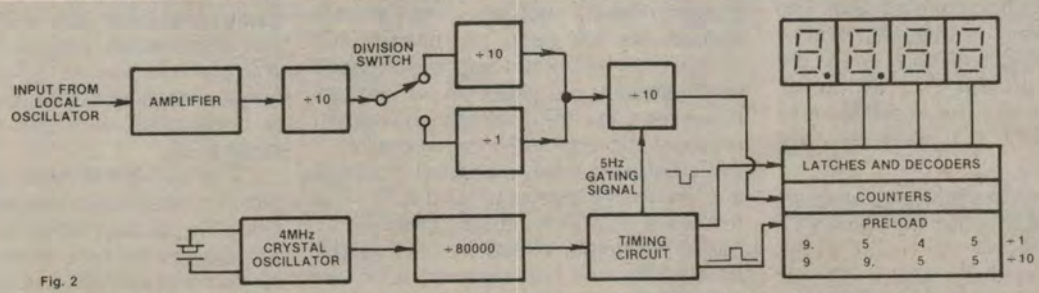


Fig. 2

The circuit is basically a DFM that is offset by an amount equal to the intermediate frequency of the receiver being measured.

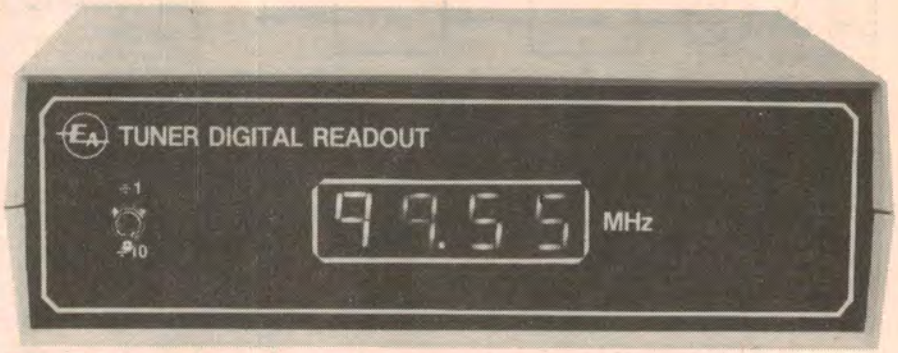
9545? The answer is that if we add 9545 and 455 we obtain 10,000 and, since the counter overranges, the display will read 0000.

By thus adding the IF to the counter preload, the counter is effectively zeroed.

Similarly, when the division switch is set to divide by 10, the counter is preloaded to 9955. This number is arrived at by rounding off the theoretical preload number of 99545 to the four most significant digits. Since counter resolution is only 10kHz in the divide by 10 position, this has no effect on the accuracy of the display.

After preloading, the gating signal allows the local oscillator signal to be counted. When counting stops, after 100ms, the latches store the BCD count and subsequently decode it to drive the seven-segment LED displays.

An example will serve to illustrate how preloading works. Let's assume that the division switch is set to divide by one and that the receiver is tuned to Sydney station 2SM on 1269kHz. The local oscillator will thus be on 1724kHz (or 1.724MHz). This frequency is fed to the counter, which counts up from 9545, on through zero and up to 1269.



This view shows the prototype displaying the divide by 10 preload value.

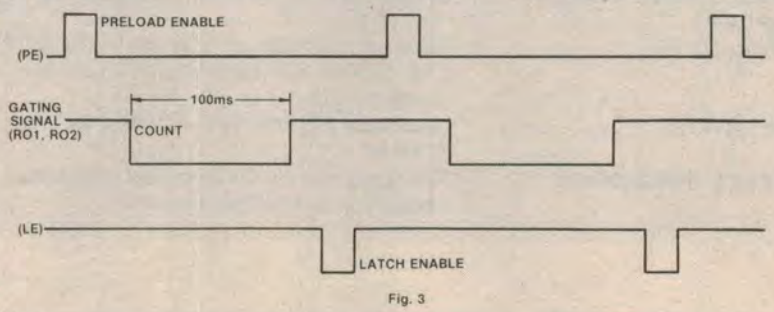


Fig. 3

These waveforms control the timing and counting operations of the circuit (see text). A full cycle takes 200ms, giving an update time of 0.2s.

Circuit details

A FET preamplifier stage and an emitter-coupled-logic (ECL) IC form the front end of the design, while low power Schottky (LS) TTL ICs are used as dividers. CMOS devices are used for the counters and decoders, however, since decoders with latching are not available in TTL.

Two separate FET preamplifiers are shown on the circuit diagram. The circuit enclosed within the dotted lines is recommended if the display is to be used with shortwave receivers, or if the leads to the local oscillator are relatively long (greater than 200mm). It is built on a separate small (38 × 24mm) PCB designed to mount inside the receiver, close to the local oscillator.

In this remote buffer stage, input signals from the local oscillator are coupled in via a 15pF capacitor to the gate of a 2N5485 N-channel FET arranged in common source configuration. The 1kΩ source resistor is bypassed with a .0047μF capacitor and this gives the stage a gain of around unity at the frequencies of interest. This is sufficient to drive the following ECL amplifier stage into clipping.

The alternative preamplifier, consisting of FET Q1, is built onto the main PCB along with the rest of the circuit. In this case, Q1 is arranged as a source follower with the gate connected to ground via a 1MΩ resistor and self-biased by a 1kΩ source load. This arrangement should work satisfactorily with broadcast band tuners, provided the leads to the local oscillator are kept short, but note that the input coupling capacitor must be increased to 47pF to compensate for the lower gain of the circuit.

The FET output is AC-coupled to cascaded ECL line receivers IC1c, IC1b and IC1a, which comprise an MC10116 triple differential line receiver IC. If this part of the circuit appears familiar, that's because an identical arrangement was used in the front end of the EA 500MHz DFM in the December 1981 issue!

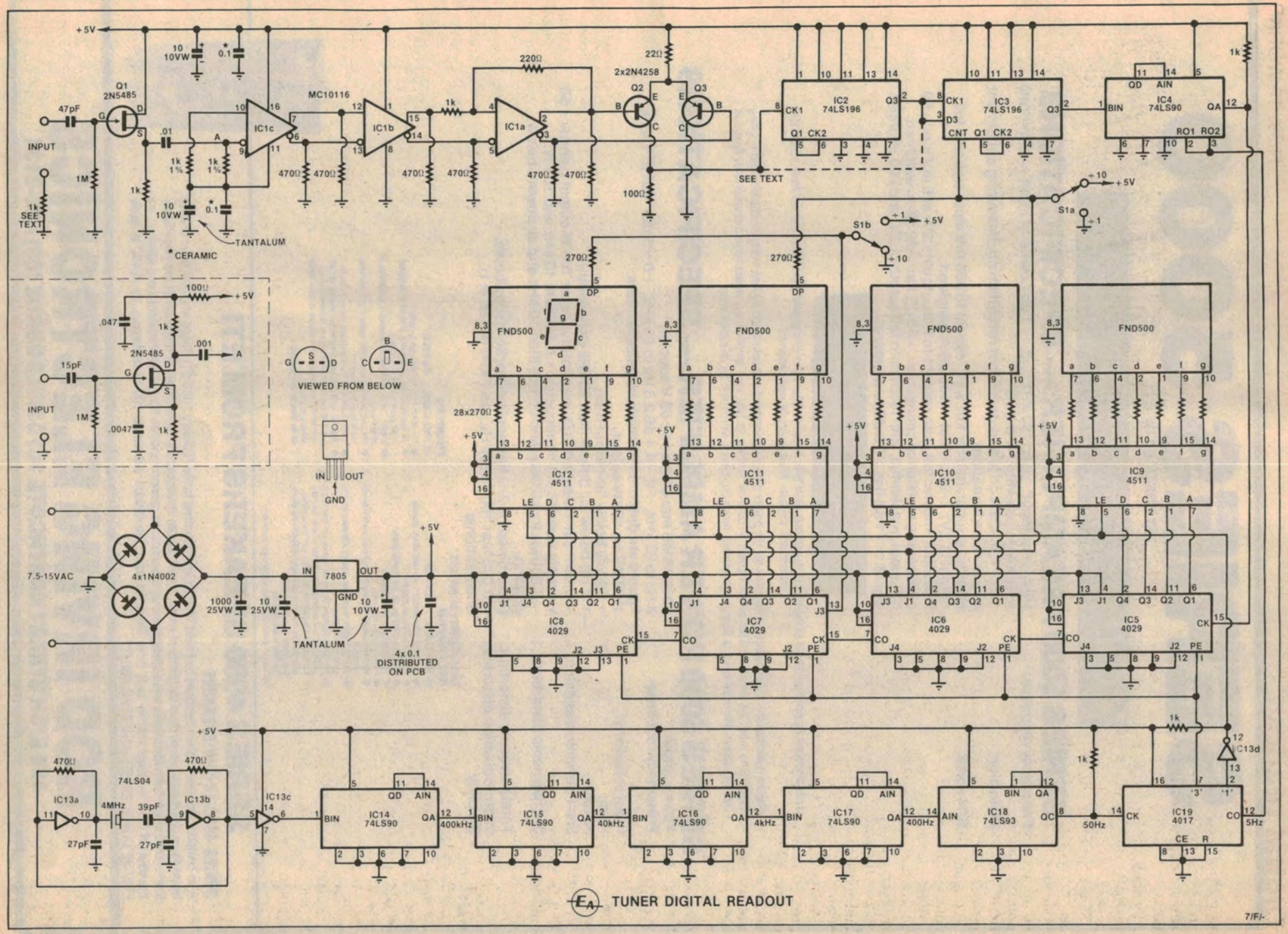
Essentially, each ECL line driver receiver consists of an NPN differential pair with a constant current source in the "tail" and resistor collector loads. The collector of each transistor is buffered by an emitter follower, which provides complementary outputs. The emitter outputs are left open, so that the ECL outputs can be ORed together to reduce the number of gates in a design. However, in this design pull-down resistors are required on each output.

ECL outputs usually swing ±0.2V about a reference voltage of around 3.7V. This reference voltage is actually provided by the 10116 on pin 11 and we have used it to bias the first line receiver, IC1c, via two 1kΩ resistors. A 0.1μF capacitor and a 10μF tantalum capacitor provide decoupling of the reference voltage.

The stage following IC1b is IC1a which operates as a Schmitt trigger by virtue of the positive feedback network consisting of the 220Ω and 1kΩ resistors. Input signals to this Schmitt trigger must exceed its two hysteresis trigger levels before the output of the trigger will change, so this stage provides a good deal of noise immunity as well as squaring up the waveform.

The ECL outputs of IC1a are converted to TTL levels by transistors Q2 and Q3, both 2N4258 high speed switching transistors. Since the ECL outputs from pins two and three swing ±0.2V about 3.7V, then either Q2 or Q3 will be on. Thus, when pin two goes low Q2 turns on and when pin three goes low Q3 turns on. Since one transister is always on, the current through the 22Ω resistor remains virtually constant at around 35mA. The output of this stage is taken from the 100Ω collector resistor of Q2 and will swing between 0.1V and 3.2V, making it directly compatible with the following TTL stage (IC2).

IC2 is a 74LS196 high speed counter which contains two separate divider circuits. The section consisting of CK1 and Q1 divides by two, while the CK2/Q3 section provides division by five. By connecting the Q1 output to CK2 the counter divides by ten and, in this configuration, will operate up to 40MHz.



EA TUNER DIGITAL READOUT

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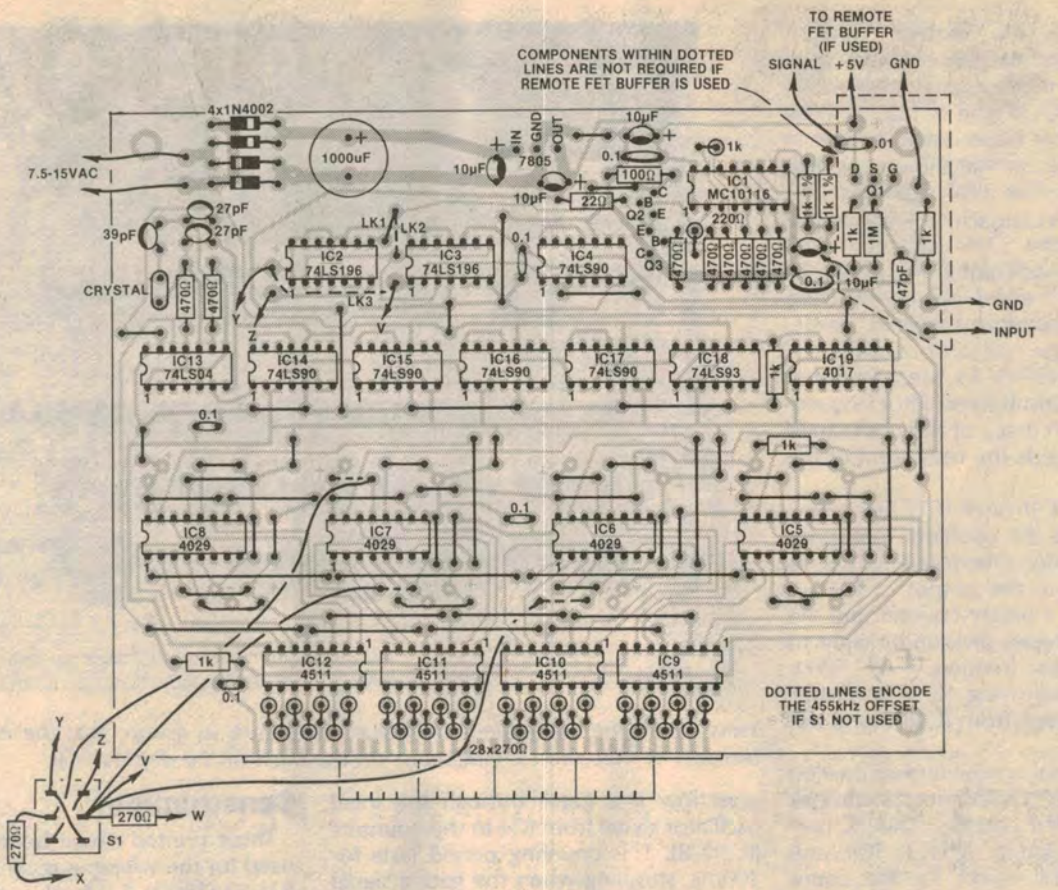


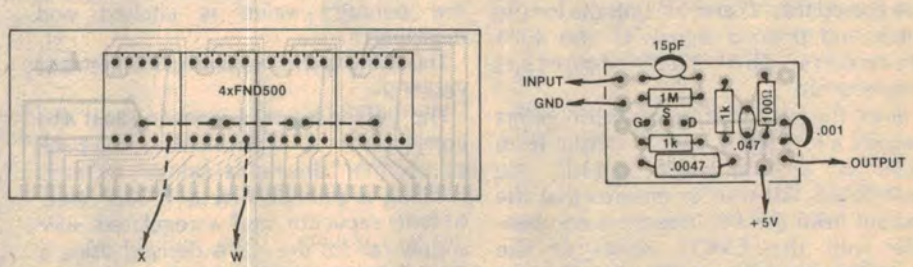
Parts layout diagram for the main PCB (30MHz version). The links shown dotted are used only in the 10MHz version.

Note that IC2 is used only for the 30MHz version. For broadcast band applications, IC2 is left out of circuit and the signal from Q2's collector applied direct to the input (pin 8) of IC3.

IC3 can be set to either divide by ten or to follow the input signal (divide by one). If IC2 is not used, then IC3 is permanently set to divide by ten. In the 30MHz version, switch S1a is used to select the division by switching the "count" input (pin 1) of IC3 either high or low. When pin 1 is held high the IC divides by ten in exactly the same manner as IC2. When the "count" is held low, the clock is disabled and the Q3 output follows the D3 input, also connected to the output of IC2. Consequently the IC divides by one.

IC4 also divides by ten. In this case, however, a 74LS90 IC is used rather that the more expensive (but faster) 74LS196 in the previous stages. The Q4 output is disabled (reset to zero) when the RO1 and RO2 inputs are brought high by the carry out (CO) of IC19, which controls the gating function. A 1kΩ pull up resistor at the output of IC4 ensures that the voltage levels of this TTL output are compatible with the CMOS clock input of IC5.

IC5, IC6, IC7 and IC8 are 4029 preset-



Parts layout diagrams for the display board (left) and the remote FET buffer stage (right). Make sure that the displays are inserted the right way round.

table decade counters interconnected in a ripple clocking mode. In other words, the carry out, CO, of the first stage is connected to the clock (CK) input of the following stage and so on. These counters have jam load, or preload, inputs whereby instead of counting up or down from zero, they can count from a predetermined number. This number is loaded into the jam inputs, J1-J4, in BCD code.

When a high signal is applied to the preload enable (PE) of each counter, the binary number programmed on the J1-J4 pins is loaded into the counter. When the preload enable is subsequently brought low, the counters begin to count.

Switching between the two preload numbers is achieved with division switch S1a and S1b. In the divide by one position, J1 of IC6 and J4 of IC7 are brought to ground, and J3 of IC7 is connected to +5V. The converse applies for the divide by 10 position. In addition, the division switch is used to switch the display decimal points which are driven via separate 270Ω resistors.

The BCD outputs of the 4029 counters are decoded by 4511 BCD to seven-segment decoder drivers (IC9, IC10, IC11 and IC12). The decoder ICs read the count when the latch signal goes low and retain this count when the latch enable (LE) subsequently goes high. The decoded outputs of the ICs drive common-cathode FND500 LED displays via 270Ω current-limiting resistors.

Clock signals are derived from a crystal-controlled oscillator consisting of a 4MHz series-mode crystal and 74LS04 TTl inverters IC13a and IC13b. A 470Ω feedback resistor biases each inverter in the linear mode, so that they act as high gain amplifiers. The 39pF capacitor provides the correct capacitive load for the crystal, while the 27pF capacitors limit the maximum operating frequency of the circuit to prevent the crystal from operating in a spurious harmonic mode. IC13c buffers the oscillator output.

It is not necessary to use a trimmer capacitor to adjust the oscillator frequency, since the accuracy of the untrimmed crystal far exceeds the resolution of the display.

IC14, IC15, IC16 and IC17 each successively divide the oscillator frequency by 10. This division ratio totals 10,000, so the frequency at the output of IC17 is 400Hz. IC18 is a binary counter and the QC output provides division by eight to give an output frequency of 50Hz. Because the following IC is a CMOS device, the output from IC18 has a 1kΩ pull-up resistor.

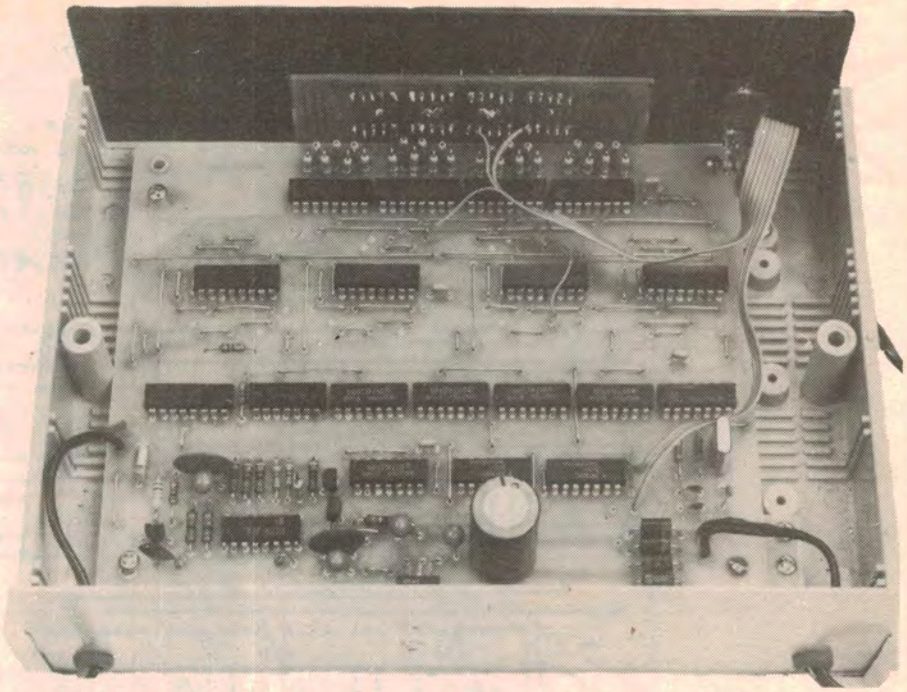
The 50Hz signal is now further divided by IC19, a 4017 CMOS decade divider with 10 decoded outputs. This IC provides the 5Hz gating signal to IC4, and provides control signals for the count and latch operations. Each of the 10 decoded outputs go high in sequence for a period of one clock cycle and we have used the "1" and "3" outputs for the latch and preload signals to the 4511 decoders and 4029 counters respectively.

Since the latch enables of the decoders require a low signal, the "1" output from IC19 is inverted with IC13d. The associated 1kΩ resistor ensures that the output from the TTL inverter is compatible with the CMOS inputs of the decoders. Fig.3 shows the waveforms used for timing the counting operation.

First, the preload enable goes high for 20ms and the counters are preloaded ready to begin counting. Then, 20ms later, the CO output (pin 12) of IC19 goes low and gates through the local oscillator signal from IC4 to the counters (IC5-IC8). This counting period lasts for 100ms, stopping when the gating signal subsequently goes high again. Finally, after a further 20ms, the latch enable to the decoders (IC9-IC12) goes low and the counted value is latched and displayed.

This cycle is then repeated for the next count.

The power supply is conventional and consists of a 7.5-15VAC plug-pack transformer driving a bridge rectifier. Filtering is provided by a 1000μF electrolytic capacitor and a regulated +5V supply rail for the ICs is derived using a 7805 3-terminal regulator. The 10μF tantalum capacitors ensure regulator stability and improve the transient response, while the 0.1μF decoupling capacitors prevent false triggering of the ICs due to supply line transients.



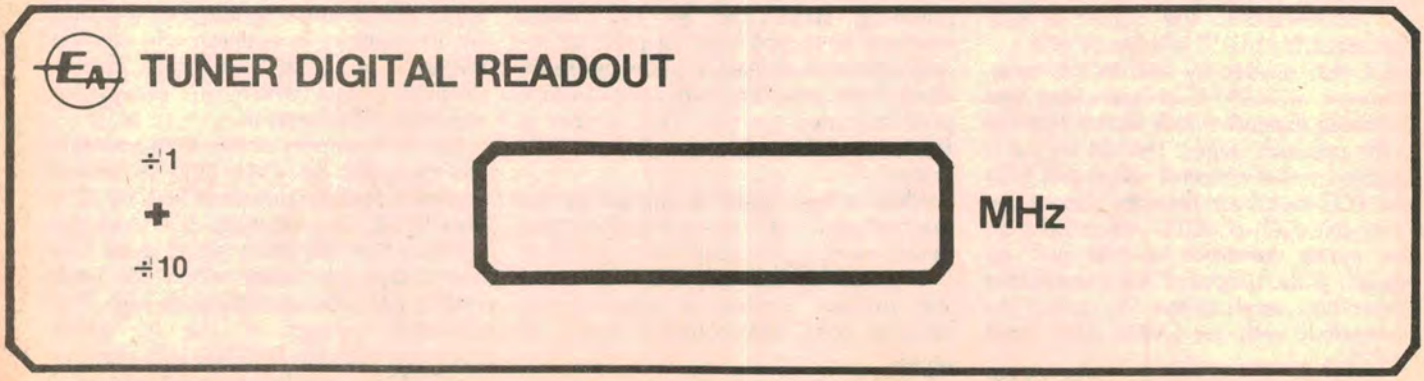
View inside the assembled prototype. Take care to ensure that the end-mounted resistors do not short connections on the back of the display PCB.

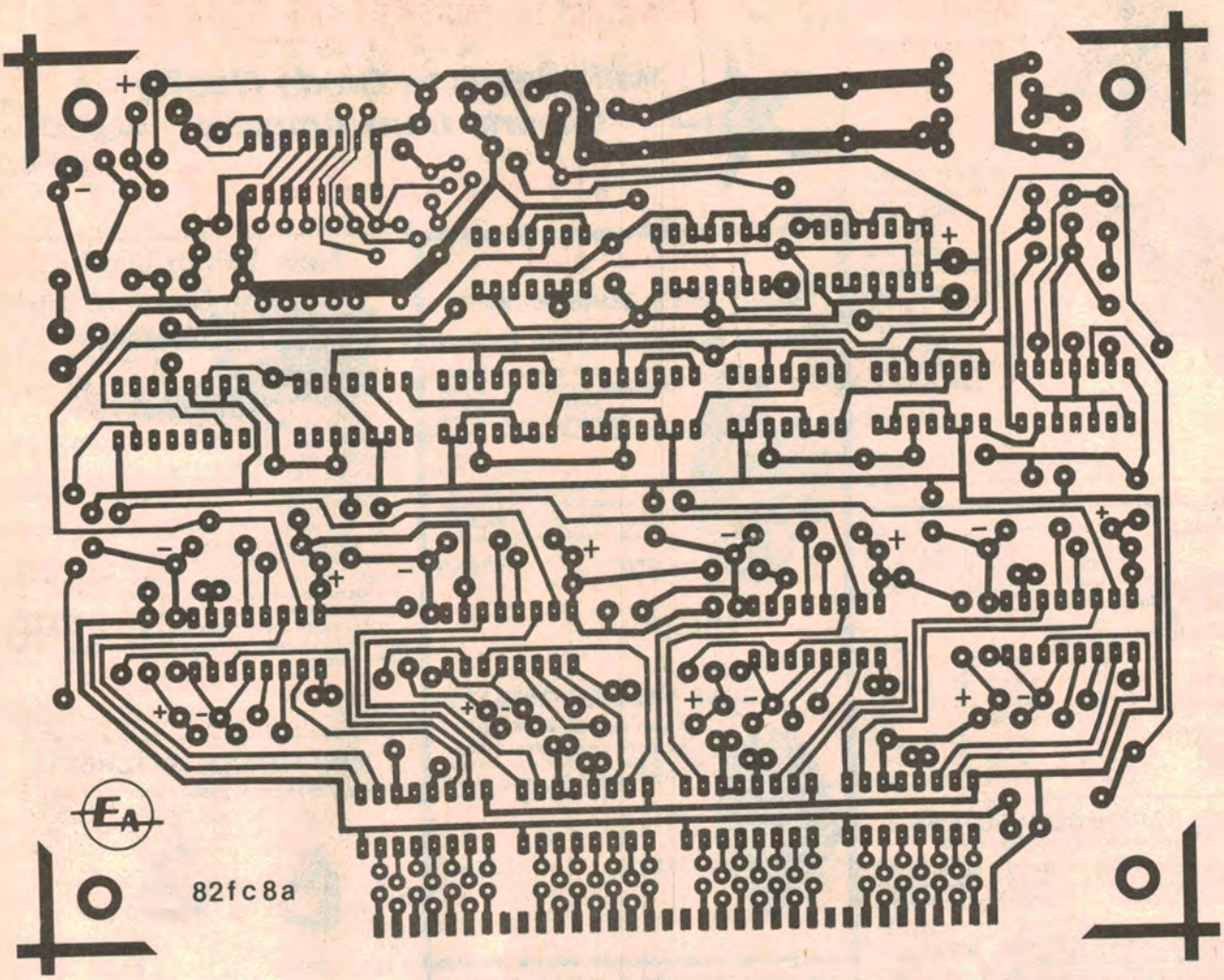
Construction

Three printed circuit boards (PCBs) are used for the wiring: a main board coded 82fc8a (160 × 125mm); a display board coded 82fc8b (93 × 33mm); and a small preamplifier board coded 82fc8c (38 × 23mm). The display board carries the four FND500 displays and is soldered at right angles to the main board to keep internal wiring to a minimum.

As explained previously, the remote preamplifier board (82fc8c) is necessary if the display is to be used with shortwave receivers or if the leads to the local oscillator would otherwise be fairly long. The preamplifier on the main board should be sufficient for most broadcast

Below is an actual size reproduction of the front panel artwork, but with the trim marks deleted so that it will fit on the page. Panel trim is 197 × 60mm.





Here are actual size reproductions of the three printed circuit boards.

band applications, provided that the interconnecting leads are kept short.

Start construction by assembling the main PCB (82fc8a) according to the parts overlay diagram. If the remote FET buffer stage is to be used, then the components enclosed by the dotted lines should be left out. Install link LK1 for the 30MHz version, but do not install any of the links shown dotted.

For the 10MHz version, omit IC2, switch S1 and link LK1, and install all the links shown dotted on the overlay diagram. These include LK2, LK3, and the three preload encoding links located above and below IC6 and IC7. In addition, pin 5 of the most significant digit should be connected to +5V via a 270Ω resistor so that the decimal point is displayed.

As shown, the dotted links adjacent IC6 and IC7 encode a 455kHz offset (or preload) if S1 is not used. This preload value can be altered to any value the reader wishes (if necessary), as explained later.

Although LS TTL ICs are specified in the parts list, standard TTL devices may be used if LS versions are unobtainable. Standard TTL draws about three times the power of LS versions and, if used throughout, an extra 100mA will be drawn by the circuit.

All the ICs face in the same direction except for CMOS ICs 9, 10, 11 and 12. When soldering the CMOS ICs, solder the power supply pins (8 and 16) first to enable the internal static protection diodes. The barrel of your soldering iron should be connected to the earth track on the PCB with a small clip lead before soldering.

The CMOS ICs are recognised by their 4029 and 4511 type numbers.

Note that many of the resistors are

PARTS LIST

1 Pac-tec case (or equivalent), 205 × 159 × 65mm
1 printed circuit board, code 82fc8a, 160 × 125mm
1 printed circuit board, code 82fc8b, 94 × 34mm
1 Scotchcal front panel, 197 × 59mm
1 4MHz series mode crystal
1 7.5-15VAC 500mA plugpack transformer
4 6mm spacers

SEMICONDUCTORS
1 MC10116 triple differential line receiver
1 74LS196 high-speed decade counter/divider
5 74LS90 decade counter/dividers
1 74LS93 divide-by-eight counter
1 74LS04 hex inverter
4 4029 presettable decade counters
4 4511 BCD to 7-segment latch decoder drivers
1 4017 decade counter/divider
1 7805 3-terminal 5V regulator
4 1N4002 1A silicon diodes
1 2N5485 VHF FET
2 2N4258 PNP transistors
4 FND500 common cathode displays

CAPACITORS
1 1000µF/25VW PC electrolytic
1 10µF/25VW PC electrolytic
1 10µF/25VW tantalum
2 10µF/10VW tantalum
4 0.1µF monolithic
2 0.1µF ceramic
1 .01µF metallised polyester
1 47pF polystyrene
1 39pF NPO ceramic
2 27pF NPO ceramic

RESISTORS
(¼W, 5% unless stated)
1 × 1MΩ, 5 × 1kΩ, 2 × 1kΩ 1%, 8 × 470Ω, 29 × 270Ω, 1 × 220Ω, 1 × 100Ω, 1 × 22Ω.

30MHz VERSION ONLY
1 74LS196 high speed decade counter/divider
1 DPDT toggle switch
1 270Ω ¼W resistor

REMOTE FET PREAMPLIFIER
1 printed circuit board, 82fc8c, 38 × 24mm
1 2N5485 VHF FET
1 .047µF metallised polyester capacitor (greencap)
1 .0047 polystyrene capacitor
1 .001µF ceramic capacitor
1 15pF ceramic capacitor
1 1MΩ resistor (¼W, 5%)
2 1kΩ resistors (¼W, 5%)
1 100Ω resistor (¼W, 5%)

MISCELLANEOUS
Rainbow cable, hookup wire, machine screws and nuts, solder, etc.

mounted end on. These include two adjacent to IC1, and 28 adjacent to ICs 9, 10, 11 and 12. The remaining resistors are mounted in the conventional manner.

The FND500 displays are mounted on the display PCB after the three wire links have been installed. These wire links are mounted underneath the displays, so be sure to mount them flush against the PCB. Take care with the orientation of the displays – the ribbed edge of each display is the top.

Construction of the remote preamplifier board (82fc8c) is straightforward. Make sure that you insert the FET the right way round, though!

Initially, the two main PC boards were designed to suit a standard Pac-tec case. Subsequently our prototype was installed in a case from Dick Smith Electronics. This case has almost identical external dimensions but internal details are different. This necessitated the contriving of two small brackets to mount the PC board, as the photographs show.

We designed a silver-on-black Scotchcal front panel label to provide an attractive finish. Carefully affix the Scotchcal label to the smooth side of the front panel, and drill and cut the mounting holes for the division switch and LED displays. The cutout for the displays can be made by first drilling a series of holes around the inside perimeter and then filing the rectangle to shape.

Proceed cautiously with this step, periodically offering the front panel to the display board so that you can judge how much progress has been made. Always file inwards, otherwise the file may tear the Scotchcal away from the plastic panel.

Larger than life-size photo of the remote FET buffer stage.

The display PCB can now be soldered to the main board. Carefully butt the two boards together at right angles, so that the edge buses line up, and lightly solder tack the two end pads. Test the assembly in the case, readjust as necessary, then solder all the pads together. Inspect the completed assembly carefully to ensure that the resistors on the main board do not foul connections on the display PCB.

Next, complete the wiring according to the parts overlay diagrams and mount the PCB assembly in the case using 6mm standoffs and machine screws and nuts. Use rainbow cable for the connections to switch S1 and don't forget the two connections to the back of the display board. The use of PC stakes will greatly facilitate external wiring connections to the main PCB.

A heatsink is required for the 3-terminal regulator and this is provided by using a 196 × 56mm aluminium sheet to replace the plastic rear panel supplied with the case. The regulator is bolted to an L-shaped bracket which, in turn, is bolted (or rivetted) to the rear panel. Two grommeted holes provide entry for the plugpack leads and the oscillator signal leads.

With construction completed, short the signal input on the main PCB to ground and switch on. If all is working correctly, the unit should display the offset value – 9545 in the divide by one position, and 9555 in the divide by 10 position. If there is no display, or the unit appears to be faulty, check the power supply to all ICs and check carefully for any missing links on the main PCB.

Note that the input must be shorted right at the main PCB for this test, irrespective of whether you are using the on-board FET preamplifier or the remote preamplifier. It is not sufficient to short the remote ends of the input leads, since the leads could act as an antenna and pick up electrical noise from the immediate environment to give a random display. This electrical noise will be swamped when the input leads are connected to a signal source.

We estimate that the cost of components for this project is approximately

$41

for the 10MHz version (excludes case and front panel). Add $2.50 for the remote FET preamplifier and $5 for parts for the 30MHz version.

Don't forget to remove the shorting link when you have completed your tests.

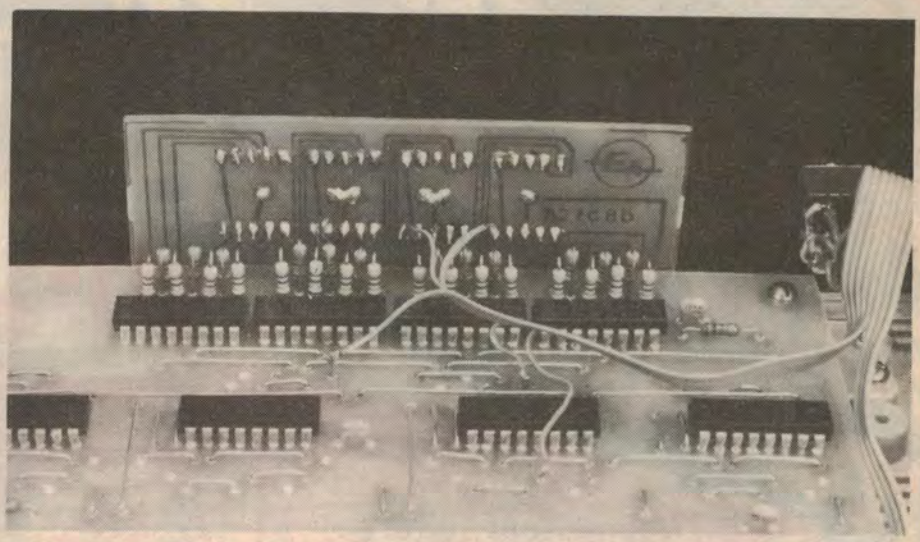
Installation

Installation simply involves connecting the signal input to a suitable point on the local oscillator of the receiver, and making the necessary ground connections. The majority of local oscillator circuits use a single transistor, although the exact circuit configuration will differ from one receiver to another. Additionally, some receivers employ separate oscillator and mixer circuits, while others employ self-oscillating mixers.

If a circuit diagram of the receiver is available, then the necessary information can be gleaned from this. If no circuit diagram is available, you will have to experiment by testing various locations around the oscillator. Generally, a direct connection to either the emitter or collector of the transistor will provide a usable signal. Select the point that affects the oscillator frequency the least.

If the remote FET preamplifier is used, it should be secured close to the local oscillator and short leads run to the oscillator output. On no account should screened cable be used to connect from the local oscillator to the buffer amplifier, since the extra capacitance will upset the local oscillator operation. Use hookup wire instead. The 1kΩ resistor in the earth leg of the on-board FET buffer amplifier was added to remove earth loop problems that may occur between the receiver and Tuner Digital Readout. Replace the resistor with a link if this problem is not evident.

Some readers may wish to alter the 455kHz preload value to suit receivers which have a different IF. To accommodate this, the main PCB has been designed so that linking can be used to select any offset required. Links from J1, J2, J3 and J4 (ICs 5 to 8) can be connected either to the positive supply rail or to the ground rail. These rails are clearly marked with + and – symbols on the track side of the PCB.



Close-up view showing how the display board is attached to the main PCB. Unused holes in the main PCB allow different IF offsets to be programmed (see text).

	J4	J3	J2	J1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Fig. 4

To calculate the preload value for the divide by one range, all you have to do is subtract the receiver's IF from 10,000 (eg. a 455kHz IF gives a preload value of 9545). The appropriate preload is then programmed into the J1-J4 pins of ICs 5 to 8 according to Fig. 4. A 5, for example, is programmed by tying J1 and J3 to +5V, and J2 and J4 to ground.

Similarly, the preload for the divide by 10 range is calculated by subtracting the IF from 100,000 and then rounding off to the four most significant digits. But it will usually not be necessary to program your own preload values. Most receivers use a 455kHz IF, so you can use the linking arrangement shown in the parts overlay diagram.