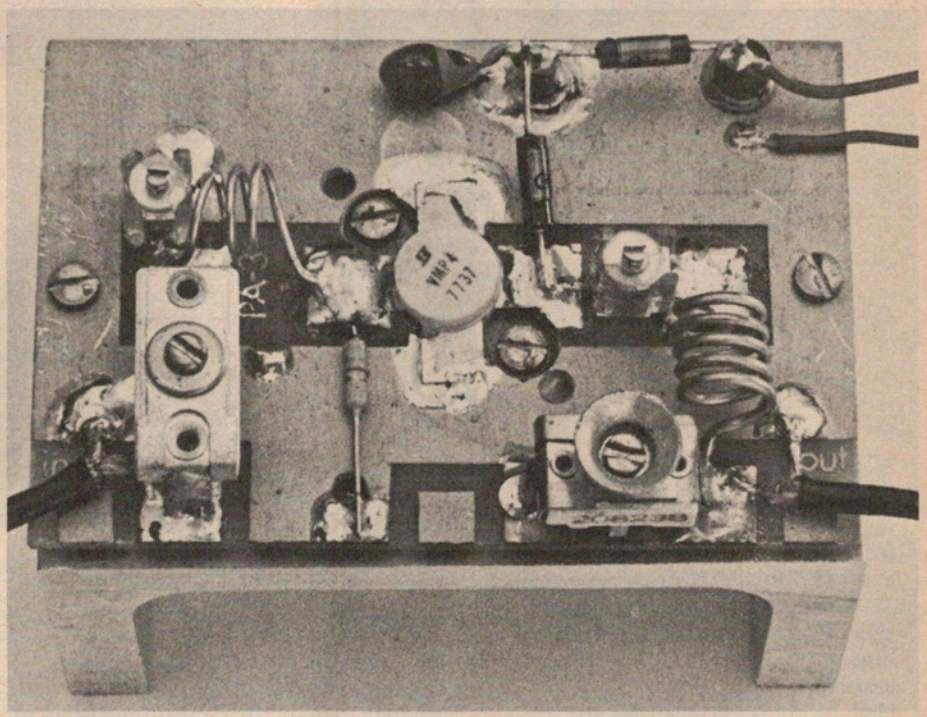
Project 720

144MHz VMOS Power Amplifier

This first practical project design for a VMOS RF PA, by Roger Harrison VK2ZTB and Phil Wait VK2ZZQ, shows these devices have a number of advantages over bipolar amplifiers.

THE LATEST DEVELOPMENT to emerge from the semiconductor research establishments is the VMOS FET. This device seems set to rapidly revolutionise many areas of solid-state technology, particularly fast switching/high current applications such as line drivers, optical data transmission, memory drivers, DC/DC converters and so on. However, VMOS devices also have unique advantages in communications circuitry. These are:

1. They can be used in any class of operation (A to D) due to the advantages of enhancement-mode operation.
2. They have excellent linear transfer characteristics. Fifth order intermodulation distortion figures are typically eight to ten dB better than bipolars.
3. The drain temperature coefficient has a negative characteristic which prevents thermal runaway. VMOS devices may be easily paralleled and will current share automatically.
4. VMOS devices have no minority carrier storage time thus allowing efficient class D operation as switching times are up to 200 times faster than bipolar devices and there are no switching transients.
5. They are, by virtue of their construction, protected against infinite VSWR problems.
6. They have a high source-drain breakdown voltage.
7. They have low gate-drain feedback capacitance. This characteristic particularly suits VHF/UHF operation.
8. Low noise figure: 2.5 dB is typical. A power amplifier can be used as a low-level amp as well.



Specification – ETI 720

Saturated output power:	V_d of 24 volts – 16 watts (13.5 watts specified) V_d of 36 volts – 22 watts (21 watts specified)
Power Gain:	V_d of 24 volts – 11.2 dB at 10 watts output (10 dB @ 200 MHz specified) V_d of 36 volts – 11 dB at 18 watts output.
Efficiency:	53%
Input VSWR:	less than 1.5:1.

The prototype was unconditionally stable without neutralisation.

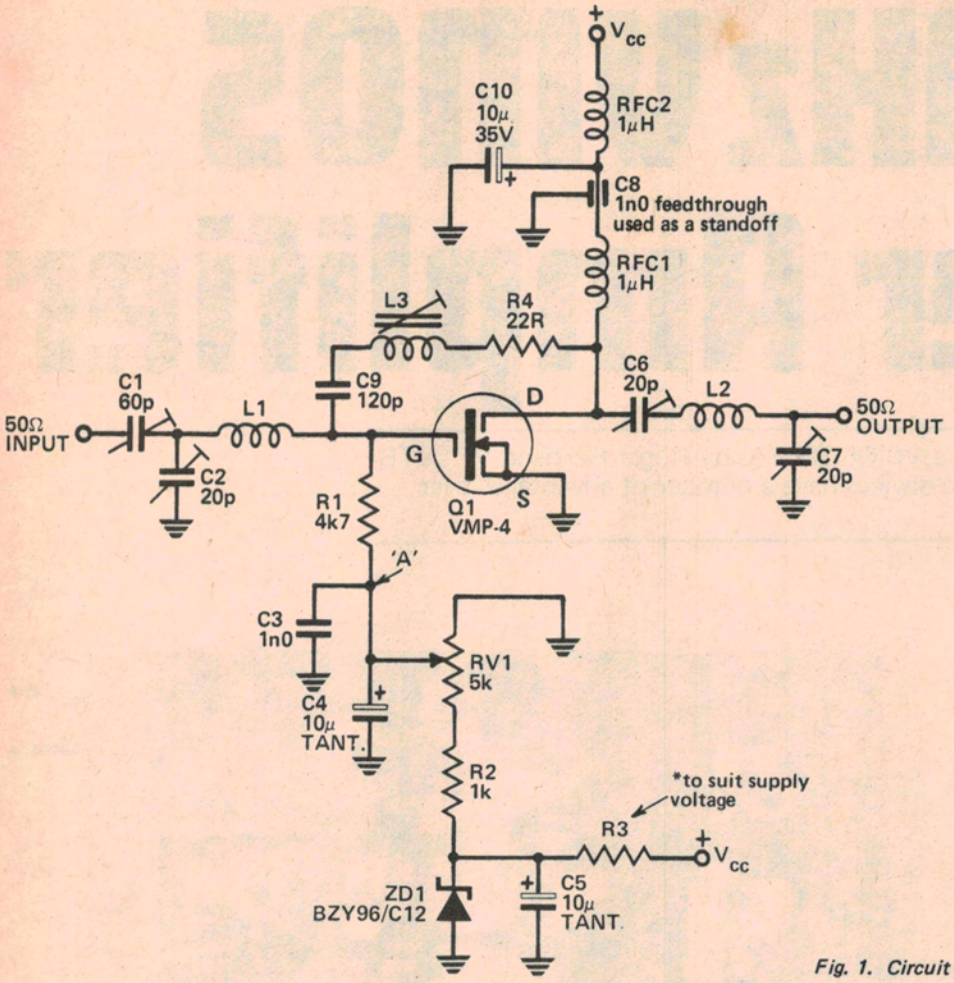


Fig. 1. Circuit diagram of the VMOS Power Amplifier.

9. Wide bandwidth and uniformity of characteristics across frequency range.
10. Higher gain than bipolars of equivalent power dissipation rating.
11. Input and output impedances generally higher than equivalent bipolar devices making matching easier.

High power MOS devices were pioneered in the mid-1960's by RCA laboratories who managed to produce an amplifier that delivered up to 14 watts at 10 MHz. The Russians next achieved 1 watt at frequencies up to 100 MHz.

Recently DMOS (double-diffused MOS) was developed in Japan and commercially produced by Signetics.

The performance of these early types of MOS technology has been surpassed by VMOS which can offer higher power levels by virtue of its inherent improved thermal transfer in the chip construction.

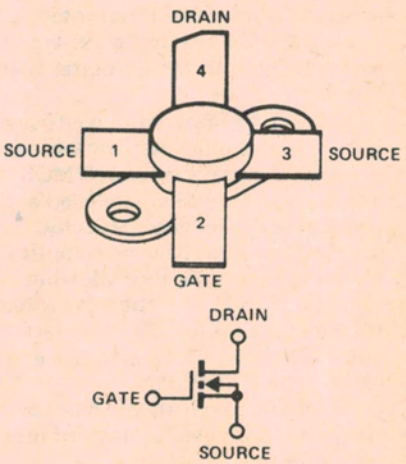
Several companies have developed VMOS devices for communications applications. These are; Westinghouse, Siliconix and the Communications Transistor Corporation. Other companies, such as Fairchild, have confined their interests to fast switching devices.

The Project

The amplifier described here will produce 10 watts output on the amateur two-metre band from a drive of less than one watt, using a 24 volt dc power supply. It can be operated in either class AB or C modes for SSB or FM applications. At a supply voltage of 36 volts (recommended maximum) the prototype delivered 22 watts of RF power driven by around two watts.

The amplifier was unconditionally stable and required no neutralisation, although the manufacturer recommended it. Typical efficiency should be greater than 50%, comparable to bipolar designs for this power level.

The device used is a Siliconix VMP-4, obtained through the Sydney agents, IRH Components, with some considerable delay between order and delivery.



NOTE: The bias and neutralisation components are not shown on the overlay. Neutralisation was not found to be necessary on the prototype.

If bias is required for linear operation R1 should be fed to the bias supply and this point by-passed through C3.

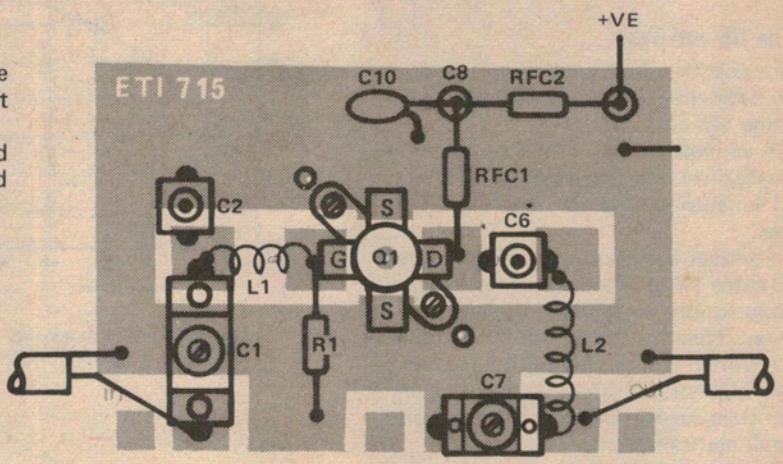


Fig. 2. Component Overlay.

PARTS LIST – ETI 720

Resistors all ¼W, 5% unless stated
R1 . . . . . 4k7
R2 . . . . . 1k
R3 . . . . . to suit supply voltage
R4 . . . . . 22R

Potentiometer
RV1 . . . . 5k lin

Capacitors
C1. . . . . 60p Elmenco mica compression trimmer, or miniature film trimmer
C2. . . . . 20p Philips miniature film trimmer
C3. . . . . 1n0 ceramic
C4, 5 . . . . 10μ tantalum
C6, 7 . . . . 20p mica compression trimmer or miniature film trimmer
C8. . . . . 1n0 feedthrough, used as standoff
C9. . . . . 120p ceramic

Semiconductor
Q1 . . . . . VMP-4 (Siliconix)

Miscellaneous
RFC1, 2 . . 1μ miniature moulded RF chokes
pc board . . ETI 715
heatsink . . to dissipate 20W
nuts, bolts, wire, etc.

We hope this article contributes to a considerable shortening of the delay in future. The VMP-4 costs around $20, although this may fluctuate due to exchange rate variations and price movements.

The circuit is shown in Figure 1. Conventional matching was employed with values calculated from data given in reference 1. Input and output impedances of the VMP-4, S_{11} and S_{22} respectively, were taken from the manufacturer's data sheet.

The neutralisation circuit, as recommended by Siliconix, shown in the circuit, was found to be unnecessary on the prototype and could probably be left out in many cases. If your amplifer proves to be unstable it may be added after construction and testing as it is quite a simple matter.

For class AB operation, bias is applied from a simple zener regulator through a pot. and resistor to the base (no messy base chokes!).

In class C operation, the 4k7 base resistor is simply earthed. RF Chokes RFC1-RFC2 are 1 uH miniature moulded chokes.

The VMP-4 is an SOE (stripline-opposed-emitter) package device with flange, rather than stud, mounting.

Construction

The amplifier is constructed on an ETI-715 printed circuit board. All components are mounted on the *copper* side of the board. Commence construction by drilling two holes diagonally opposite the transistor mounting hole, as shown in figure 2 and the photograph, to clear the mounting bolts for the transistor flange. A small file should be used to elongate the holes.

Drill two holes in the heatsink to accommodate the transistor flange securing bolts.

Next, carefully solder the VMP-4 to the copper side of the pc board taking care that the orientation is correct: gate to the input side, drain to the output side.

All the minor components may then be soldered to the board. Wind and mount the two coils L1 and L2 last.

Take care when mounting the pc board assembly to the heatsink. Secure the VFET flange-mounting bolts first. These could be tapped into the heatsink (as we did with the prototype) or secured by nuts through the other side of the heatsink.

The pc board should be secured, and at the same time grounded to, the heatsink by two bolts. These were placed at each end of the pc board, simply for convenience, and a suitable number of washers placed between the pc board and the heatsink so that the pc board was firmly secured without placing strain on the VFET leads.

Input and output switching, if required, may be effected by diode switching (as detailed in reference 4),

or a carrier-operated-relay circuit (see reference 5).

Tune Up and Test

Once construction is completed, and you have checked that all is correct, testing can commence.

A variable supply with a current limiting facility is suggested for initial test and tune up. Bias is not necessary at this stage.

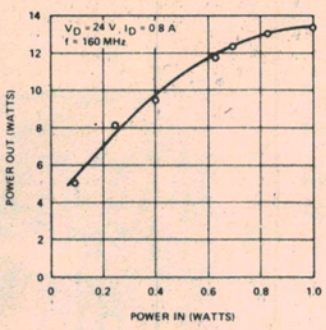
Connect the output to a dummy load and some RF power measuring device. Apply supply voltage and then drive power. Tune for maximum RF output! This should correspond with a peak in drain current. If 'funny' things happen here then suspect positive feedback and install neutralisation.

It's dead simple. However, take care not to grossly overdrive the device — VFETS do not take kindly to this sort of abuse. Becoming the owner of a four-legged stripline fuse can be a chastening experience!

For class AB linear operation, bias should be set to provide about 100 mA quiescent drain current, subsequently adjusted for best performance.

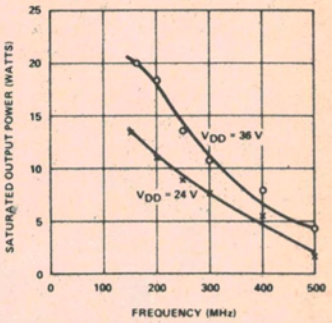
Some adjustment of the input network was required on the prototype suggesting that the input impedance, S_{11}, of the particular VMP-4 was lower than indicated on the data sheet.

Output Power vs Input Power*



*Conjugate input/output match

Saturated Output Power vs Frequency*
P_{IN} = 1 Watt, I_{DRAIN} = 0.8 A



*Conjugate input/output match

Characteristic		Min	Typ	Max	Unit
BV_{DSS}	Drain-Source Breakdown	60			V
$I_{D(on)}$	ON-State Drain Current	400	600		mA
g_{fs}	Forward Transconductance	170	240		m℧
C_{oss}	Common-Source Output Capacitance		34	37	pF
C_{iss}	Common-Source Input Capacitance		32	35	
C_{rss}	Reverse Transfer Capacitance		4.8	6.5	
G_{ps}	Common-Source Power Gain	10			dB
NF	Small Signal Spot Noise Figure		2.5		

Conclusion

This project proved exceptionally easy to build and its performance very impressive. Other VMOS devices should be available soon from CTC who are marketing a range with output powers from 10 W to 100 W (see ETI, March 1978, page 92).

One obvious application of a VMOS amplifier takes advantage of its excellent small- and large-signal characteristics. One could construct a unilateral mast-head amplifier with the supply voltage fed up the centre-conductor of the feedline coax. With a bit of cunning PIN-diode switching the device would serve as a power amplifier on transmit and a low-noise preamp on receive. A hand-held low power transceiver such as a Ken KP202, or a low power (home-brew) transverter/transceiver would then combine to make quite a powerful base station. Less expensive coax, having a higher loss than could normally be tolerated (like RG58), could be used at a saving approaching the cost of the amplifier in many cases.

This project is but a starting point.

Coil Winding Details - ETI 720

L1. . . . . 5 turns 18 B+S (19 SWG) tinned copper wire 6mm inside dia. 10mm long.

L2. . . . . 3 turns 18 B+S (19 SWG) tinned copper wire 6mm inside dia. 6mm long.

L3. . . . . 4 turns 26 B+S (27 SWG) enamelled wire wound on Neoside L1010 former with F29 slug.

References

1. "VFETS for Everyone", by Wally Parsons, ETI January 1978, pp. 37-41; and February 1978, pp. 53-58.

2. "Matching Network Designs with Computer Solutions", by Frank Davis, Motorola Applications Note AN-267.

3. "Solid State RF Power Amplifiers", by Roger Harrison VK2ZTB and Phil Wait VK2ZZQ, from Proceeding of the Symposium of Future Amateur Communications Techniques (FACT), May 20-21, 1978.

4. "VHF Power Amplifiers", by Roger Harrison VK2ZTB and Phil Wait VK2ZZQ, ETI November 1977 (part 1).

5. "VHF Power Amplifiers", by Roger Harrison VK2ZTB and Phil Wait VK2ZZQ, ETI February 1978 (part 3).