SCRs, triacs and power control

SCRs and triacs are high speed solid state switches specifically intended for use in ac and dc power control applications. Ray Marston explains their basic principles in this edition of Circuit File, to be followed next edition with a stack of application circuits.

Ray Marston

FOR ELECTRONIC switching applications in dc and ac circuits, SCRs and triacs have no equals and wide application. The SCR is like a diode you can turn on and off while the triac is like two back-to-back diodes you can turn on and off (back-to-back SCRs!). That's the easiest way to think of these two very useful, related, devices. But to be able to appreciate their characteristics and how to use them, you need to know about them in somewhat more depth. So, let's look at some basic theory and circuits first.

The SCR: basic theory

The SCR, or silicon controlled rectifier, is a four-layer pnpn semiconductor switching device. It is represented by the symbol shown in Figure 1a. Figure 1b shows the transistor equivalent circuit of the SCR, which takes the form of a complementary regenerative switch in which the base current of Q1 is derived from the collector of Q2 and the base current of Q2 is derived from the collector of Q1. Figure 1c shows the basic connections for using the SCR as a switch in dc power control circuitry. The basic characteristics of the SCR can readily be understood with the aid of Figures 1b and 1c, and are as follows.

(1) When power is first applied to the SCR (by closing SW1 in Figure 1c) the SCR is 'blocked' and acts like an open-circuit switch. This action can be understood by looking at Figure 1b, where it can be seen that, since Q1 base is shorted to the cathode via R1-R2, Q1 is cut off through lack of base current and thus feeds no base drive to Q2, which is also cut off. As both transistors are cut off under this condition only a small leakage current flows between the anode and cathode of the device.

(2) The SCR can be turned on and made to act like a closed switch (or forward-biased silicon rectifier) by simply applying positive gate current by closing SW2 in Figure 1c. This gate current causes the SCR to switch on very rapidly.

If the externally-applied gate current is sufficiently large it will apply base drive to Q1, causing Q1 to start to turn on. As Q1 starts to turn on, its collector current feeds base drive to Q2, causing Q2 to turn on and feed increased base drive into Q1, etc. A fast regenerative action thus takes place, with both transistors switching rapidly into saturation, the total saturation voltage typically being in the range one to two volts.

(3) Once the SCR has been turned on and is conducting significant forward current, the gate loses control and the SCR remains latched on even if the gate drive is subsequently removed. Thus, only a brief pulse of gate current is needed to latch the SCR on. Note from Figure 1b that, because of the presence of R1 and R2, the SCR can *not* be turned off by shorting or reverse-biasing the gate-cathode terminals of the device.

(4) Once the SCR has latched into the on state it can only be turned off again by momentarily reducing its anode current below a value known as the 'minimum holding current'. Since turn-off occurs whenever the current is reduced below this critical value, it follows that turn-off occurs automatically in ac circuits near the zero-crossing point at the end of each half-cycle.

(5) Internal capacitance inevitably

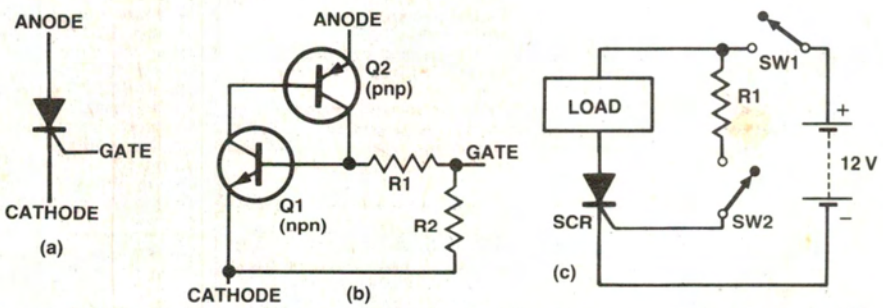

Figure 1. (a) SCR symbol (b) transistor equivalent circuit of the SCR and (c) basic connection for using the SCR as a dc power-control switch.

DATA FILE 7 DEVICE TYPE NO.	PIV RATING	TOTAL CURRENT RATING, RMS/average	V_{GT} (max)	I_{GT} (max)	I_H (max)
TAG 1/100	100 V	1 A/0.64 A	2.5 V	10 mA	25 mA
TAG 1/600	600 V	1 A/0.64 A	2.5 V	10 mA	25 mA
C106D	400 V	4 A/2.5 A	0.8 V	0.2 mA	3 mA
2N3525	400 V	5 A/3.2 A	2 V	15 mA	20 mA
BT109	500 V	6.5 A/4 A	2 V	15 mA	3 mA
IR122A	100 V	8 A/5 A	1.5 V	25 mA	30 mA
IR122D	400 V	8 A/5 A	1.5 V	25 mA	30 mA
C116D	400 V	8 A/ 5 A	1.5 V	20 mA	35 mA
C126M	600 V	12 A/7.5 A	1.5 V	30 mA	35 mA

Figure 2. Basic details of some of the most popular SCRs.

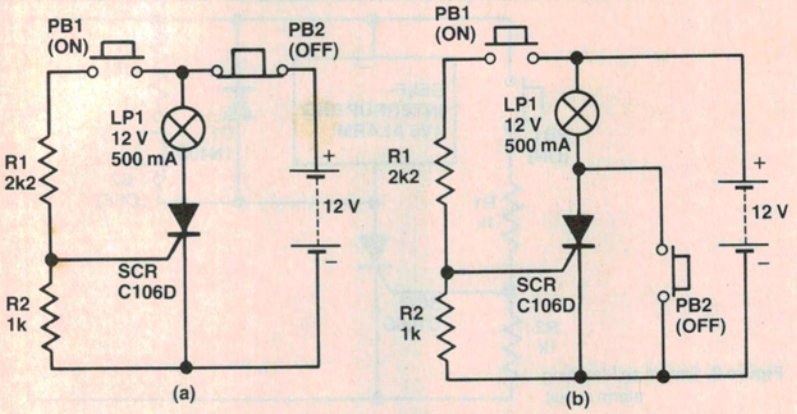

Figure 3. (a) Simple dc on/off circuit and (b) alternative dc on/off circuit.

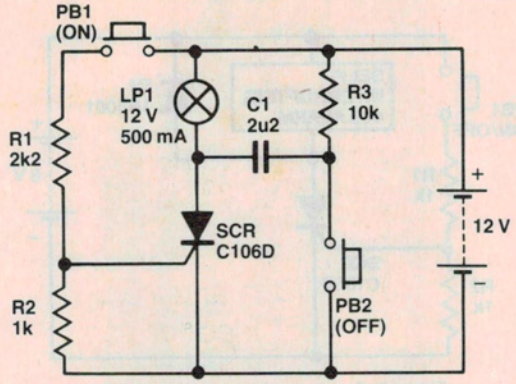

Figure 4. Capacitor turn-off circuit.

exists between the anode and gate of the SCR. Consequently, if a sharply rising voltage is applied to the SCR anode this internal capacitance can cause part of the rising voltage to break through to the gate and thus trigger the SCR on. This 'rate-effect' turn-on can be caused by supply-line transients, and sometimes occurs at the moment that supplies are switch-connected to the SCR anode. Rate-effect problems can usually be overcome by wiring a simple RC 'snubber' network between the anode and cathode of the SCR, to limit the rate-of-rise to a safe value.

These then, are the basic characteristics of the SCR. As you can see, it's a pretty simple device. If you ever need to select an SCR for a particular application, you'll usually find that the most significant parameters are the main voltage and current ratings, plus the gate sensitivity rating and (occasionally) the device's 'minimum holding current' value. The list of Figure 2 gives basic details of a few of the most popular SCRs.

The SCR: basic dc circuits

SCRs have applications in both dc and ac power control circuitry. Let's look first at some basic dc circuits. Figures 3a and 3b show alternative ways of using the SCR as a pushbutton-controlled on/off power switch feeding a 12 volt, 500 mA lamp. In both circuits the lamp and SCR can be latched on by momentarily closing PB1, thereby feeding gate drive to the SCR via R1. Note that the gate is tied to the cathode via R2, to give improved stability. Once the SCR has latched on, it can only be turned off again by momentarily reducing the anode current below the device's I_H value; in Figure 3a this is achieved by momentarily opening PB2; in Figure 3b the turn-off action is achieved by using PB2 to place a momentary short between the anode and cathode of the SCR.

Figure 4 shows another way of achieving SCR turn-off. Here, once the SCR has turned on, C1 charges up to almost the full supply voltage via R3 and the SCR anode, with the R3 end going positive. When PB2 is subsequently closed it clamps the positive end of C1 to ground, and the C1 charge forces the SCR anode to momentarily swing negative, thereby reverse-biasing the SCR and causing it to turn off. The capacitor charge bleeds away rapidly under this condition, but has to hold the SCR anode negative for only a few microseconds to ensure complete turn-off. Note that C1 must be a non-polarised component.

A variation of the capacitor turn-off circuit is shown in Figure 5. A slave SCR is used to replace PB2 of Figure 4 and capacitive turn-off of SCR1 is achieved by briefly driving SCR2 on via PB2. SCR2 turns-off once PB2 is released, since the anode current provided by R3 is lower than the SCR2 holding current.

Figure 6 shows how the above circuit can be modified so that it acts as an SCR bistable or flip-flop driving two independent lamp loads. Assume that SCR1 is on and SCR2 is off, so that C1 is fully charged with its LP2 end positive. The state of the circuit can be changed by briefly operating PB2. SCR2 is then driven on via its gate, and as it goes on it drives SCR1 off capacitively via its anode. C1 then recharges in the reverse direction. The state of the circuit can then again be changed by briefly operating PB1, thus driving SCR1 on via its gate and driving SCR2 off capacitively via its anode. The flip-flop process is repeated ad infinitum.

The dc circuits that we have looked at so far have all used simple resistive 'lamp' loads and have inevitably produced a self-latching ▶

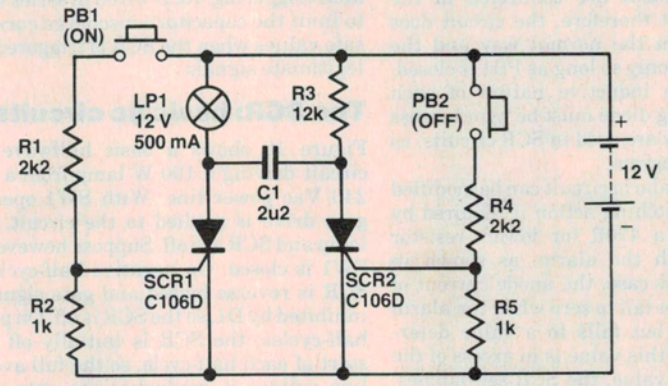

Figure 5. Capacitor turn-off with SCR slaving.

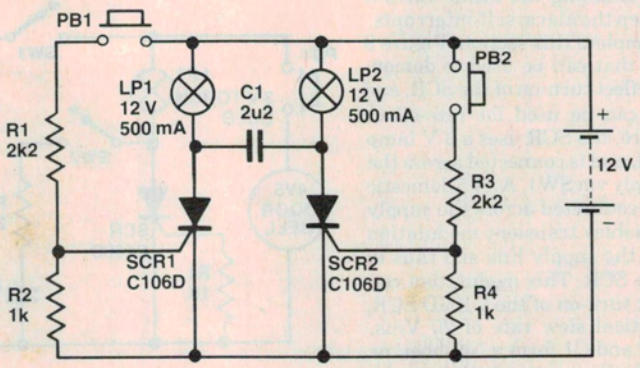

Figure 6. SCR bistable or flip-flop.

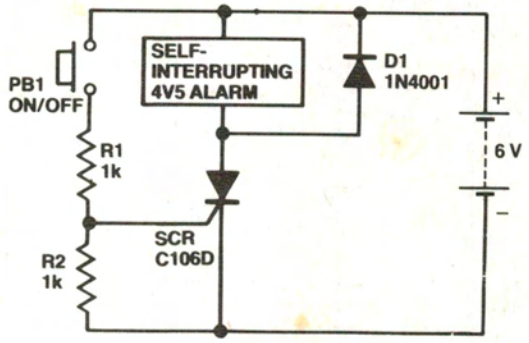

Figure 7. Simple non-latching alarm circuit.

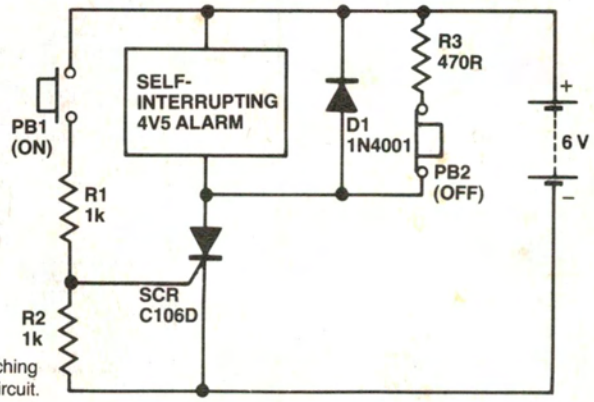

Figure 8. Simple self-latching alarm circuit.

action in the SCRs. Figure 7 however, shows a simple dc alarm circuit driving a self-interrupting load such as a bell or buzzer, and gives a non-latching action.

When self-interrupting devices such as bells or buzzers are connected across a supply, a current flows through a built-in solenoid via a pair of contacts. This current induces a magnetic field in the solenoid and causes a striker to fly outwards and open the contacts, causing the current to fall to zero and making the magnetic field collapse. Once the field has collapsed the striker falls back again and the contacts close, so current is again applied to the solenoid and the action repeats. Consequently, this type of load acts like a switch that repeatedly opens and closes rather rapidly.

When such loads are connected in the Figure 7 circuit therefore, the circuit does not self-latch in the normal way and the alarm operates only so long as PB1 is closed. Because of the inductive nature of such loads, a damping diode must be wired across them when they are used in SCR circuits, as shown in the diagram.

The Figure 7 alarm circuit can be modified to give a self-latching action if required by simply wiring a 470R (or lower) resistor in parallel with the alarm, as shown in Figure 8. In this case, the anode current of the SCR does not fall to zero when the alarm self-interrupts, but falls to a value determined by R3. If this value is in excess of the SCR's 'holding' value, the SCR self-latches. The circuit can be unlatched by briefly operating PB2, enabling the anode current to fall to zero when the alarm self-interrupts.

Finally, to complete this section, Figure 9 shows a circuit that can be used to demonstrate the rate-effect turn-on of the SCR, and a method that can be used for rate-effect suppression. Here, the SCR uses a 3 V lamp as its anode load, and is connected across the 4V5 battery supply via SW1. A 4V5 domestic door bell can be connected across the supply via PB1, and enables transient modulation to be applied to the supply line and thus to the anode of the SCR. This modulation can cause rate-effect turn-on of the C106D SCR, which has a critical slew rate of 20 V/us. The network R2 and C1 form a 'snubber' or rate-effect suppression network and can be connected to the SCR via SW2.

To demonstrate the rate-effect, open SW2, close SW1, and then close PB1 so that the bell rings. The resulting supply line transients should be enough to trigger the SCR and turn the lamp on; if not, wire a one ohm resistor in series with the battery. Once the SCR and lamp have been triggered on, they can be turned off again by briefly opening SW1.

Once the turn-on rate-effect has been demonstrated, the effect of the suppressor network can be demonstrated by closing SW2 and SW1 and then operating the bell via PB1. The lamp resistance (plus R2) acts with C1 as a smoothing network that reduces the rate of rise of the anode modulation signal, thereby protecting the SCR against false triggering. R2 is wired in series with C1 to limit the capacitor's discharge currents to safe values when the SCR is triggered on via legitimate signals.

The SCR: basic ac circuits

Figure 10 shows a basic halfwave on/off circuit driving a 100 W lamp from a 120 or 240 Vac power line. With SW1 open, zero gate drive is applied to the circuit, so the lamp and SCR are off. Suppose however, that SW1 is closed. On negative half-cycles, the SCR is reverse biased and gate signals are inhibited by D1, so the SCR is off. On positive half-cycles, the SCR is initially off at the start of each half-cycle, so the full available line voltage is applied to the gate via the lamp and D1-R1; shortly after the start of the half-cycle sufficient voltage is available to trigger the SCR, which turns on. As the SCR goes on its anode voltage falls to near zero, thus removing the gate drive but the SCR remains self-latched for the duration of the half-cycle. The SCR automatically turns off again when the half-cycle ends and the anode current falls to zero.

The Figure 10 circuit gives halfwave operation only. Figures 11 and 12 show alternative ways of obtaining fullwave operation. In these circuits, the ac is converted to rough (unsmoothed) dc via a bridge rectifier and the rough dc is applied to the SCR. With SW1 open the SCR is off, so zero current flows through the bridge and the load. When SW1 is closed the SCR is driven on shortly after the start of each half-cycle of rough dc, so fullwave power is applied to the load. As the SCR goes on in each half-cycle, the gate drive is automatically removed but the SCR stays latched on for the duration of the half-cycle. The SCR switches off at the end of each half-cycle as its anode current falls to zero, so power is removed from the load when SW1 is opened.

Note in the Figure 11 circuit that the load is connected to the dc side of the bridge. A fuse must be placed on the ac side of the bridge, to give protection in the event of a short in the bridge rectifier. In the Figure 12 circuit the load is placed in the ac side of the bridge, which does not need fuse protection since the load itself will limit currents to a safe value in the event of a bridge failure.

A pair of SCRs can easily be wired in

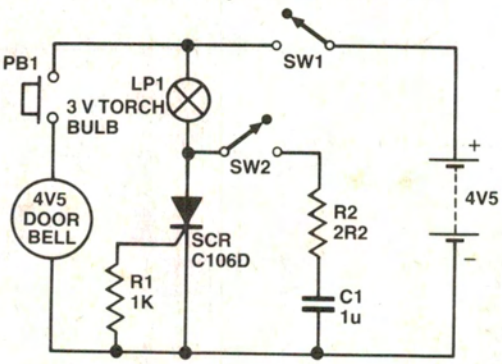

Figure 9. Rate-effect demonstration circuit.

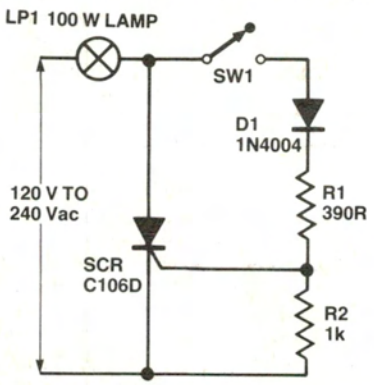

Figure 10. Line driven halfwave on/off circuit.

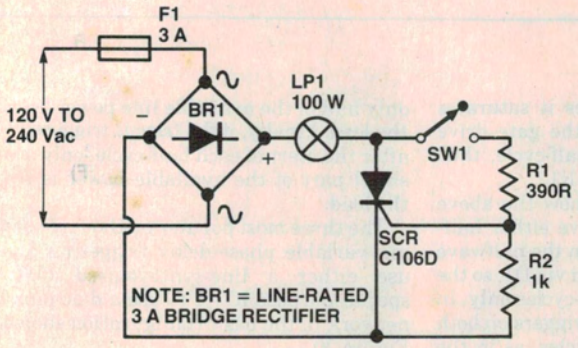

Figure 11. Fullwave on/off circuit.

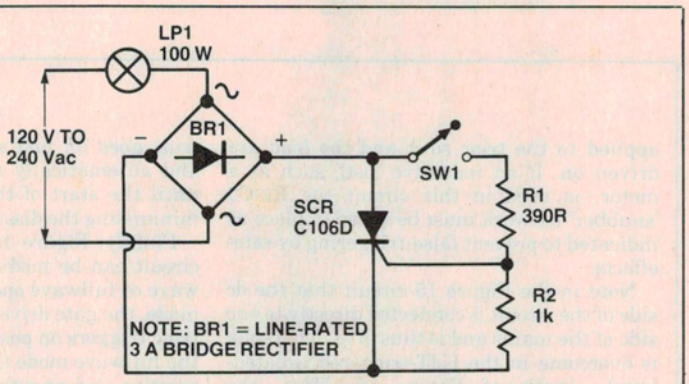

Figure 12. Alternative connection for fullwave on/off circuit.

inverse parallel and used to give fullwave power control without the use of additional rectification. In reality, however, a far more effective way of obtaining fullwave power control is to use a triac in place of the SCRs. Let's now look at triac basics.

The triac: basic theory

A triac can be regarded as being equal to two conventional SCRs connected in inverse parallel within a single three-terminal package, but so arranged that they share a single gate terminal. The triac acts as a solid state power switch that can conduct current in either direction and can be switched from the off to the on state by a gate signal of either polarity.

Figure 13a shows the triac symbol and Figure 13b shows a basic connection for using the device as an ac power switch. The load is wired in series with the triac's main terminals, the combination being wired directly across the ac power line. By closing SW1 dc gate drive can be applied to the triac. Referring to Figure 13b, the basic characteristics of the triac are as follows:

(1) Normally, with no gate signal applied, the triac is off and acts (between MT1 and MT2) like an open circuit switch.

(2) If MT2 is appreciably positive or negative relative to MT1 the triac can be turned on (so that it acts like a closed switch) by applying a gate signal via SW1. The device takes only a few microseconds to turn on. A saturation potential of one or two volts is developed across the triac in the on mode. Once the triac has turned on it self-latches and remains on so long as main-terminal current continues to flow. Only a brief pulse of gate current is thus needed to turn the triac on.

(3) Once the triac has self-latched the gate loses control and the triac can only be turned off again by reducing its main-terminal current below a minimum holding value. When the triac is used as an ac power switch therefore, turn-off occurs automatically near the zero-crossing point at the end of each half-cycle as the main-terminal currents fall to zero.

(4) The triac can be turned on by either a positive or negative gate signal, irrespective of the polarities of the main-terminal voltages. The device thus has four possible triggering modes or 'quadrants', signified as follows:

I+ Mode, MT2 current = +ve, I_{gate} = +ve.
I− Mode, MT2 current = +ve, I_{gate} = −ve.
III+ Mode, MT2 current = −ve, I_{gate} = +ve.
III− Mode, MT2 current = −ve, I_{gate} = −ve.

Gate sensitivities in the I+ and III− modes are approximately equal and about twice as high as in the I− and III+ modes.

(5) Triacs can handle very high surge or non-repetitive currents. Typically, a device with a 10 A RMS rating may be able to handle a single-cycle, non-repetitive 50 Hz surge current of 100 amps!

Figure 14 shows basic details of a limited range of popular triacs. In most applications this limited information is sufficient for user needs. Let's now move on and look at some basic ways of using the triac.

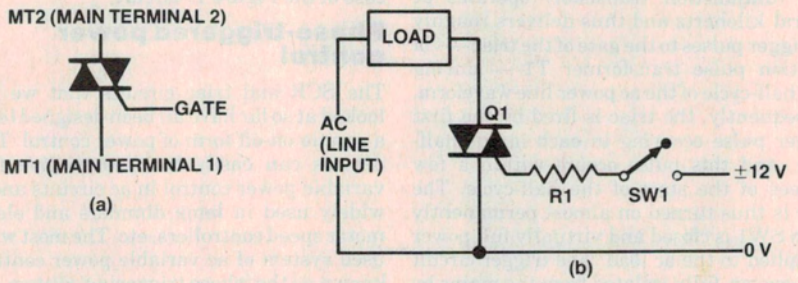

Figure 13. (a) Triac symbol and (b) basic triac circuit with dc gate drive.

The triac: basic circuits

Figure 15 shows the practical circuit of a simple dc-triggered triac power switch in which the dc supply is derived via step-down transformer T1. When SW1 is open, no current flows to the gate of the triac, which is thus off. When SW1 is closed, gate drive is

DEVICE TYPE NO.	PIV RATING	TOTAL CURRENT RATING RMS	V_{GT} (max)	I_{GT} (max)	I_H (max)
C206D	400 V	3 A	2 V	5 mA	30 mA
2N6073	400 V	4 A	2.5 V	30 mA	70 mA
C226D	400 V	8 A	2.5 V	50 mA	60 mA
SC146D	400 V	10 A	2.5 V	50 mA	75 mA
TIC246D	400 V	15 A	2.5 V	50 mA	50 mA

Figure 14. Basic details of some popular triacs.

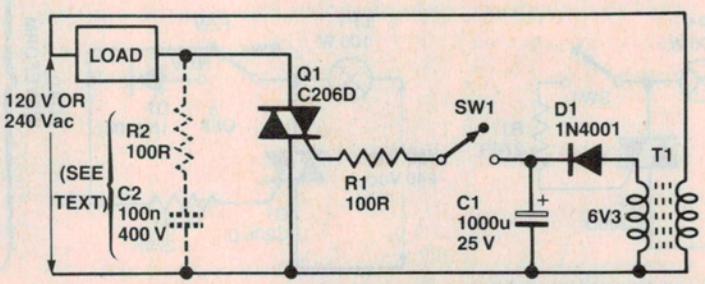

Figure 15. Simple ac power switch with dc gate triggering.

applied to the triac so it and the load are driven on. If an inductive load, such as a motor, is used in this circuit the R2-C2 'snubber' network must be wired in place as indicated to prevent false-triggering by rate-effects.

Note in the Figure 15 circuit that the dc side of the circuit is connected directly to one side of the mains and is thus 'live'. This snag is overcome in the UJT-triggered isolated-input circuit of Figure 16. Here, the UJT (unijunction transistor) operates at several kilohertz and thus delivers roughly 50 trigger pulses to the gate of the triac — via isolation pulse transformer T1 — during each half-cycle of the ac power line waveform. Consequently, the triac is fired by the first trigger pulse occuring in each mains half-cycle, and this pulse occurs within a few degrees of the start of the half-cycle. The triac is thus turned on almost permanently when SW1 is closed and virtually full power is applied to the ac load. The trigger circuit is, however, fully isolated from the mains by transformer T2 and pulse transformer T1.

Figure 17 shows how the triac can be used as a simple line switch with line-derived triggering. With SW1 open, zero gate drive is applied so the triac and lamp are off. Suppose however, that SW1 is closed. At the start of each half-cycle the triac is off, so the full line voltage is applied to the gate via the lamp and R1. Shortly after the start of the half-cycle, enough drive is available to trigger the triac and the triac and lamp go on. As the triac goes on and self-latches it saturates and automatically removes the gate drive until the start of the next half-cycle, thus minimising the dissipation in R1.

Finally, Figure 18 shows how the above circuit can be modified to give either half-wave or fullwave operation. In the halfwave mode, the gate drive is applied via D1, so the triac triggers on positive half-cycles only. In the fullwave mode the triac triggers on both positive and negative half-cycles, as in the case of the Figure 17 circuit.

Phase-triggered power control

The SCR and triac circuits that we have looked at so far have all been designed to give a simple on-off form of power control. These devices can easily be used to give fully-variable power control in ac circuits and are widely used in lamp dimmers and electric motor speed controllers, etc. The most widely used system of ac variable power control is known as the 'phase triggering' system.

Figure 19 illustrates the principle of phase-triggering using a triac as the power control element. Here, instead of the triac being triggered 'directly' from the ac power line, it is triggered via a variable phase-delay network that is interposed between the power line and the triac gate. Thus, if the triac is triggered 10° after the start of each half-cycle, almost the full available line power is fed to the load. If the triac is triggered 90° after the start of each half-cycle, only half of the available line power is fed to the load. Finally, if the triac is triggered 170° after the start of each half-cycle, only a very small part of the available power is fed to the load.

The three most popular methods of obtaining variable phase-delay triggering are to use either a line-synchronised UJT, a special-purpose IC, or to use a diac plus RC network in the basic configuration shown in Figure 20.

The diac can be regarded as a bilateral threshold switch. When connected across a voltage source, it acts like a high impedance until the applied voltage rises to about 35 volts, at which point it switches into a low impedance state and remains there until the applied voltage falls to about 30 volts, at which point it reverts to the high impedance mode. It then stays in this state until the applied voltage rises back to 35 volts, at which point the process repeats.

In the Figure 20 circuit, in each mains half-cycle the R1C1 network applies a variable phase-delayed version of the mains waveform to the triac gate via the diac, and

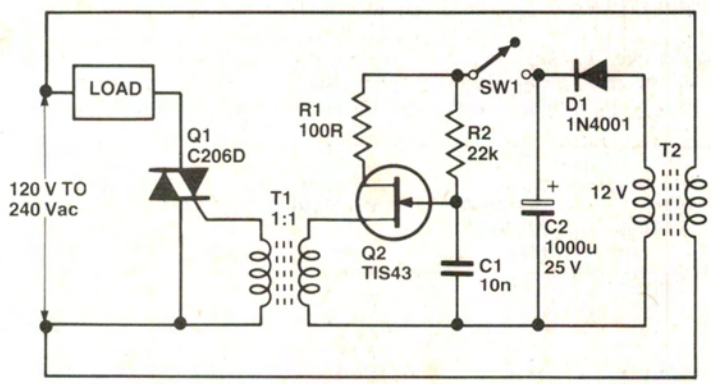

Figure 16. UJT-triggered isolated-input ac power switch.

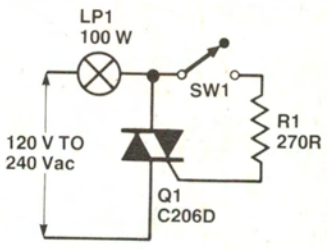

Figure 17. Line-triggered triac switch.

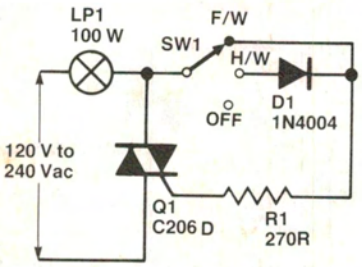

Figure 18. Three-way line switch.

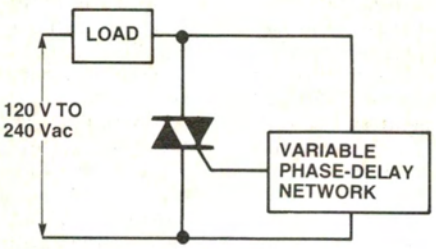

Figure 19a. Variable phase-delay 'switch'.

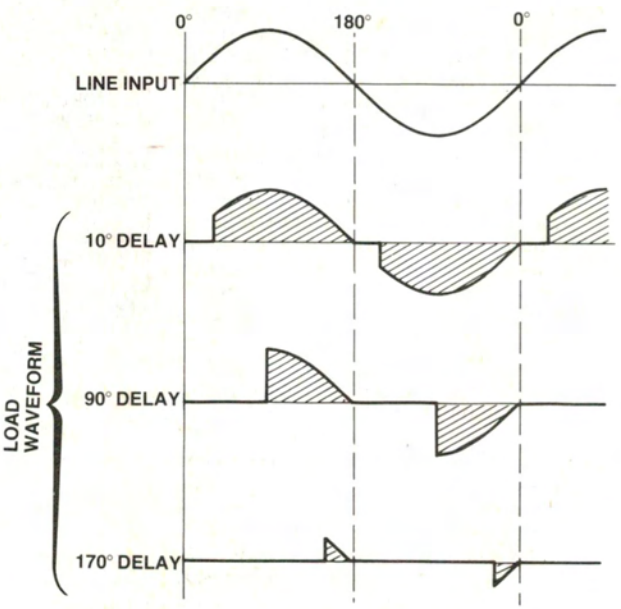

Figure 19b. Variable phase-delay waveforms.

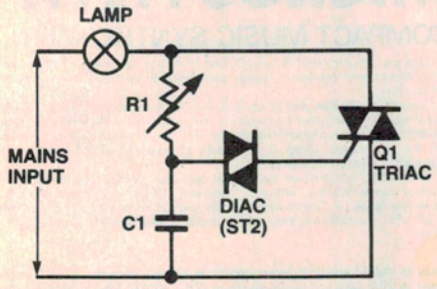

Figure 20. Basic 'diac-type' variable phase-delay lamp dimmer circuit.

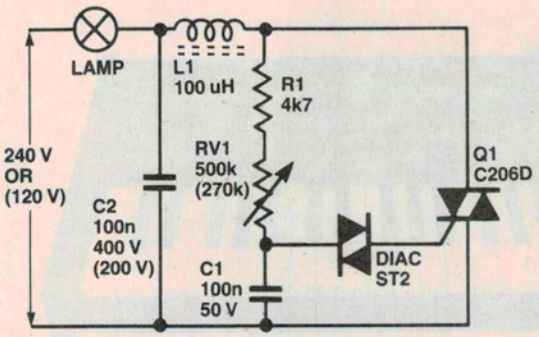

Figure 21. Practical lamp dimmer with RFI-suppression.

each time the C1 voltage rises to 35 volts the diac fires and delivers a trigger pulse to the triac gate, thus turning the triac on, simultaneously applying power to the lamp load and removing the drive from the RC network. The mean power to the load (integrated over a full half-cycle period) is thus fully variable from near-zero to maximum, via R1.

Radio frequency interference (RFI)

You can see from the Figure 19 waveforms that, each time the triac is gated on, the load current changes abruptly (in a few micro-seconds) from zero to a value determined by the load resistance and the instantaneous mains voltage. This action generates radio frequency interference (RFI). The RFI is greatest when the triac is triggered at 90°, and is least when the triac is triggered close to the 0° and 180° 'zero-crossing' points of the mains waveform.

In lamp dimmer circuits, where there may be considerable lengths of mains cable between the triac and the lamp load, this RFI may be offensive as it will be widely radiated, interfering with radio and television receivers and other appliances. In practical lamp dimmers the circuit is usually provided with an LC RFI suppression network, as shown in Figure 21, to overcome this problem. (Note: in Figure 21 the values in brackets are applicable to 120 V mains operation.)

Zero-crossing techniques

When high power loads, such as electric heaters, are driven from triac circuitry special techniques must be used to minimise RFI. Even if the triac is used as a simple on-off switch in such applications, a 'spurt' of RFI will be generated each time the switch is turned on, and will be of maximum amplitude if the instantaneous phase delay happens to be 90° at the moment of turn-on. RFI problems can be eliminated in high-power applications by using the synchronous or 'zero-crossing' gating technique illustrated in Figure 22.

Here, a low power 12 volt dc supply is generated directly from the mains via R1-D1-ZD1 and C1. A simple zero-crossing detector network (a couple of transistors) is

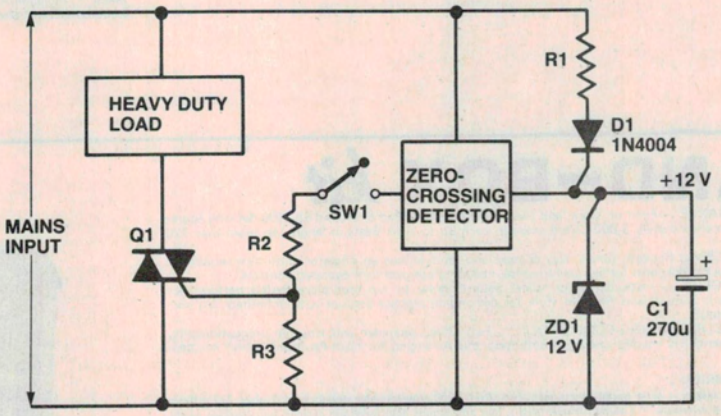

Figure 22. Basic synchronous or 'zero-crossing' mains power switch.

connected directly across the mains and controls the passage of current from C1 to SW1 in such a way that the C1 current is made available for only 5° or so on either side of each zero-crossing point of the mains waveform. Thus, if SW1 is closed, a pulse of gate current is fed to the triac at the start of each half-cycle of mains voltage, at which point the mains voltage is close to zero, so the triac always generates minimal RFI as it turns on.

The 'zero-crossing' technique can be used to provide RFI-free variable power control in high-power loads, such as electric heaters, by replacing SW1 of Figure 22 with a variable mark/space-ratio waveform generator so that a variable integral number of complete mains power cycles are alternately fed or not fed to the load.

Figure 23 illustrates the basic principle, in which the total integral period is equal to eight mains cycles. Thus, if the power is alternately switched on for four cycles and off for four cycles, the mean load power is equal to half of the total available power, and if the power is on for one cycle and off for seven cycles, the mean power is equal to only one eighth of the total available power.

In the next edition of 'Circuit File' we'll look at some practical 'zero-crossing' and integral-cycle power controllers, together with a variety of lamp dimmers and motor-speed controllers. ●

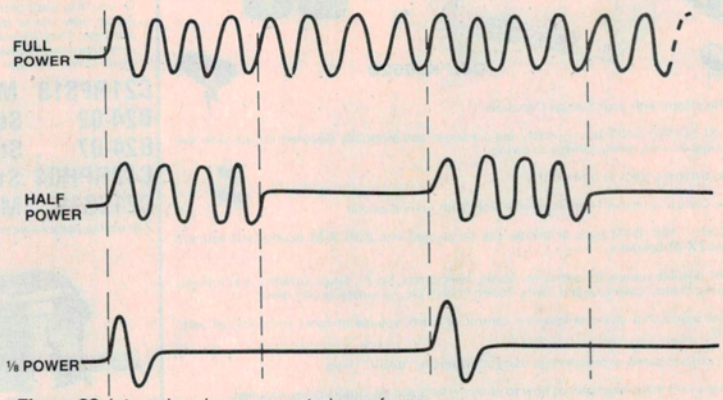

Figure 23. Integral-cycle power control waveforms.