TEXAS INSTRUMENTS

POWER MANAGEMENT

Analog Applications Journal

BRIEF

Understanding Power Supply Ripple Rejection in Linear Regulators

By John C. Teel • *Analog IC Designer, Member Group Technical Staff*

Power Supply Ripple Rejection (PSRR) is a measure of how well a circuit rejects ripple at various frequencies coming from the input power supply and is very critical in many RF and wireless applications. In the case of an LDO, it is a measure of the output ripple compared to the input ripple over a wide frequency range (10Hz to 10MHz is common) and is expressed in decibels (dB). The basic equation for PSRR, and more specifically PSRR for an LDO, can be written as:

$$PSRR = 20 \log \frac{Ripple_{INPUT}}{Ripple_{OUTPUT}}$$

where A_V is the open-loop gain of the regulator feedback loop and A_{VO} is the gain from V_{IN} to V_{OUT} with the regulator feedback loop open.

$$PSRR = 20 \log \frac{A_V}{A_{VO}}$$

From this equation it can be seen that to increase the PSRR it is beneficial to increase the open-loop gain and decrease the gain from V_{IN} to V_{OUT}. Typically, A_{VO} is significantly less than 0dB with –10 to –15dB being typical and this is entirely driven by parasitics (internal and external) from input to output and at the gate of the pass-FET. Figure 1 shows a simplified block diagram of a PMOS pass-FET.

Another parameter that is closely related to PSRR is line transient response. PSRR is specified at specific frequencies, whereas a line transient essentially contains all frequencies due to the Fourier components of a step function; however, the primary difference is that PSRR is a small signal response, whereas line transients are large signal and thus are theoretically much more complicated in nature. However, what improves PSRR improves line transient response and typically vice versa (unless what improves the line transient is only a large signal improvement) so many times it is convenient to just improve one or the other knowing that both will be improved. Therefore, all of the effects on PSRR discussed in this article will also have the same effect on the line transient response.

A curve showing PSRR over a wide frequency range is shown in Figure 2.

Figure 1:

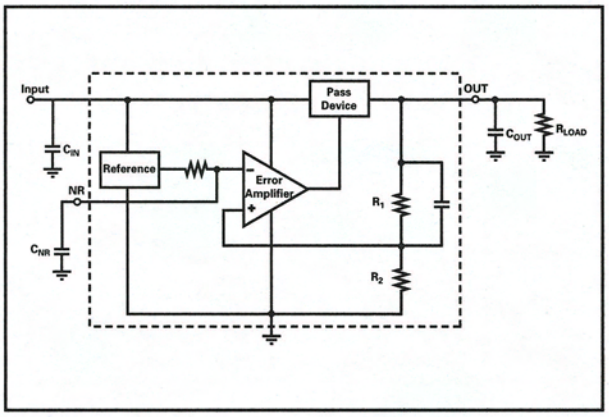
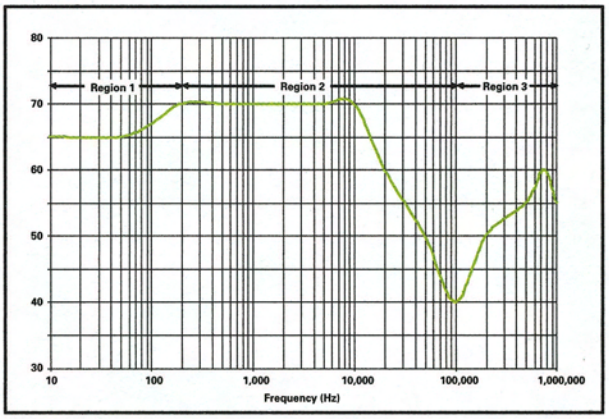


Figure 2:



As mentioned previously the open-loop gain of the LDO feedback circuit is the dominant factor in PSRR (at least in a limited frequency range) and therefore LDOs requiring good PSRR typically have high gain with a high unity-gain frequency (large gain-bandwidth product); however, this also makes the loop more difficult to stabilize and that keeps a limit on how much the gain-bandwidth product can be increased to improve PSRR. It is important to have a high unity-gain frequency so that the amplifier does not lose open-loop gain at relatively low frequencies thus causing PSRR to also roll off.

The curve in Figure 2 shows that PSRR for an LDO can be broken down into three basic frequency regions. The first region is from DC to the rolloff frequency of the bandgap filter and is dominated by both open-loop gain and bandgap PSRR. The second region extends from the bandgap filter rolloff frequency up to the unity-gain frequency and in this region PSRR is dominated mainly by the open-loop gain of the regulator. Above the unity-gain frequency is region three and here the feedback loop has very little effect because there is no longer any open-loop gain and the output capacitor dominates along with any parasitics from V_{IN} to V_{OUT}. Also the gate driver's ability to drive the pass-FET gate at high-frequency has an effect in region three . A larger output cap with less ESR will typically improve PSRR in this region. It should be noted that although increasing C_{OUT} can improve PSRR it can also actually decrease the PSRR at some frequencies. This is because increasing the output capacitor lowers the unity-gain frequency thus causing the open-loop gain to rolloff earlier therefore lowering PSRR in that region. Although a larger output capacitor will cause the PSRR to roll off earlier, the minimum PSRR that occurs at the unity-gain frequency will typically be improved.

Anything affecting the gain of the feedback loop also affects PSRR in region two. One example is load current. As load current increases the open-loop output impedance of the LDO decreases (a MOSFET's output impedance is inversely proportional to the drain current) thus lowering the gain. In addition to lowering the gain, increasing the load current also pushes the output pole to higher frequencies thus broadbanding the feedback loop. So the net effect of increasing the load is a reduction in the PSRR at lower frequencies (because of the reduced gain) along with an increase of PSRR at higher frequencies.

Another example that affects PSRR by changing the regulator open-loop gain is the differential DC voltage between input and output. As V_{IN}–V_{OUT} is lowered less than about 1V, the internal pass-FET (which provides gain in a PMOS design) starts to be pushed out of the active region (saturation) of operation and into the triode/linear region thus causing the feedback loop to lose gain. The dividing line between the active region and the triode region is proportional to the square-root of the drain current (load current). So as the load current is increased the necessary voltage across the device (V_{IN}–V_{OUT}) to keep it in the active region increases as the square-root of load current. So, for example, having V_{IN}–V_{OUT} at only 0.5V may have no negative effect on PSRR at light load currents because the pass device doesn't need much headroom to stay in the active region so the gain is preserved. However, at heavier loads 0.5V may no longer be sufficient and the pass device will enter the triode region and the circuit will lose gain and PSRR will be reduced. When comparing PSRR among various LDOs, it's always important to compare them at identical V_{IN}–V_{OUT} and ILOAD conditions (it's also important to compare LDOs at identical output voltages since PSRR is usually better at lower output voltages).

One of the dominant internal sources of PSRR in an LDO is the PSRR of the bandgap reference. Any ripple that makes its way on to the reference will get gained up and sent to the output so it's important to have a bandgap reference with high PSRR. Typically, the solution that is chosen is to simply filter the bandgap with a low-pass filter. This way only the PSRR at low-frequencies (i.e. line regulation) is important for the bandgap thus greatly simplifying the bandgap, design because the LPF takes care of all the ripple at frequency. This LPF is almost always accomplished with an internal resistor and an external capacitor (large resistors are much easier to fabricate on-chip than large capacitors). The effect of this LPF can be seen in Figure 2 and as can be seen below the RC filter frequency (region 1), the PSRR is reduced somewhat by the PSRR of the bandgap coming into play.

As has been shown there are many things that can be done to improve the PSRR in a LDO application. The most important being to start off with an LDO designed for high PSRR such as the TPS793/4/5/6xx family of low-noise, high-PSRR LDOs and the TPS799xx low-noise, high-PSRR, low-I_Q LDO. The next most critical decision is the selection of the output capacitor with a low ESR ceramic capacitor being the best choice and the capacitance value being determined depending on at which frequencies PSRR is most important. Finally, board layout must be carefully done in order to reduce the feedthrough from input to output via board parasitics.

Related Web Sites
www.ti.com/TPS79333
www.ti.com/TPS79933