SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SWITCHING WITH MOSFETs AND IGBTs: 50Hz TO 200kHz

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ABSTRACT

The basics of IGBT and Power MOSFET characteristics are discussed and their switching behaviour analysed. Circuits for loss evaluation of MOSFETs and IGBTs are described and evaluation methods for output charge and energy are shown. It is demonstrated that on-resistance and output capacitance are related and how loss minimization can be achieved in different PWM and resonant topologies. Gate drive methods enabling reduced switching loss, better overload behaviour and less driver energy consumption are also shown.

INTRODUCTION

The excellent switching behaviour of Power MOSFETs is an incentive to power supply designers to increase switching frequencies and thus reduce the cost and size of the magnetics. Nevertheless, low frequency switching with controlled current and voltage rise times can also lead to new concepts and cost reduction. When optimising low and high frequency power control circuits, the neglected parasitic effects of Power MOSFETs and their bipolar counterparts, IGBTs, become important and have to be taken into account for circuit - design.

A: UNDERSTANDING POWER MOSFET AND IGBT BEHAVIOUR

Over the last few years, Power MOSFET high voltage capability and on-resistance have been very much improved. The on-resistance per die area is a means by which these improvements can be measured (fig.A1).

On resistance per die area is close to the physical limits for Power MOSFETs having a 600 - 1000V breakdown voltage, thus major improvements in the on-resistance of these devices can be obtained only by increasing the die area.

Bipolar operation is the only way to decrease on-resistance per unit area to below the physical limit dictated by the resistance of the n-body of the MOSFET.

The Insulated Gate Bipolar Transistor (IGBT), the Bipolar Modulated FET (BM-FET) and the Field Controlled Thyristor (FCTh) have bipolar modes of operation.

THE DIFFERENCE BETWEEN POWER MOSFETS AND IGBTS

The IGBT can be understood as a Power MOSFET driving a PNP-transistor (fig.A2). During conduction, the p-layer injects minority carriers into the resistive n-layer, thus significantly reducing the on-resistance of the device (fig.A2).

The higher the breakdown voltage of the device, the higher the difference in on-resistance between a unipolar Power MOSFET and a bipolar IGBT. Fig.A3 shows the output characteristics of 1000V devices having similar die-size.

The reduced on-resistance of IGBTs does not come for free: IGBTs exhibit more turn-off losses than Power MOSFETs (fig.A4) and their protection against overload is more difficult.

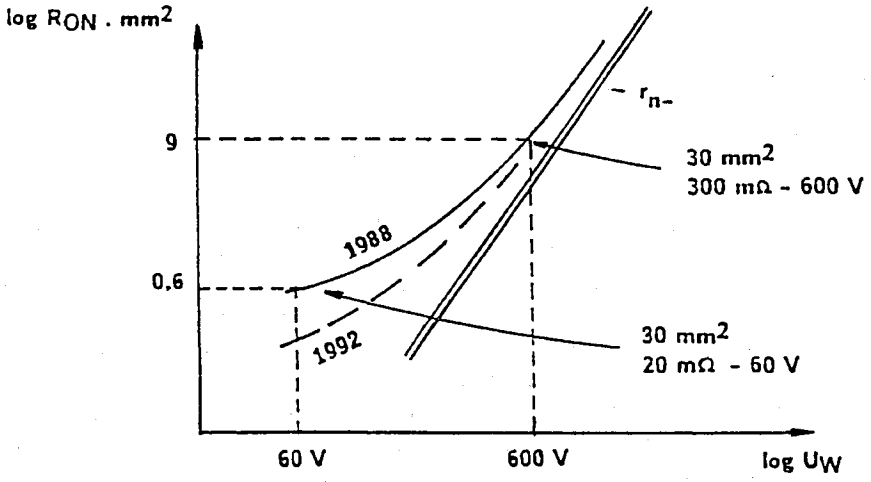


Fig. A1: MOSFET's on-resistance per silicon area versus breakdown voltage. With high voltage devices it is close to bulk-resistance. Low voltage devices have much potential for improvement.

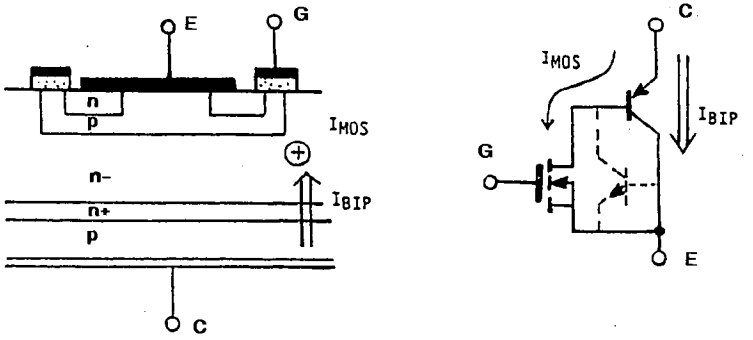


Fig. A2: Cross section and simplified equivalent circuit of an Insulated Gate Bipolar Transistor (IGBT). This device combines low on-resistance with simple drive requirements.

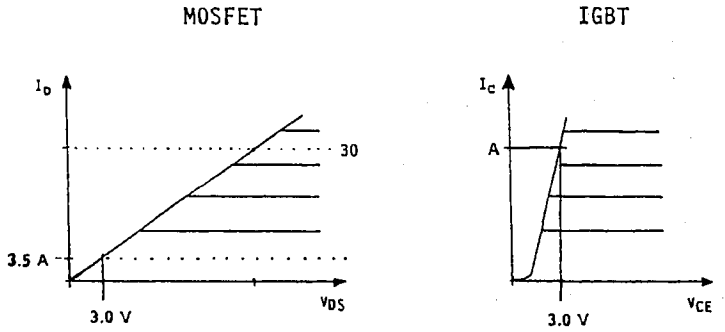


Fig.A3: Output characteristics of a 1000V-MOSFET and an IGBT having similar die-size.

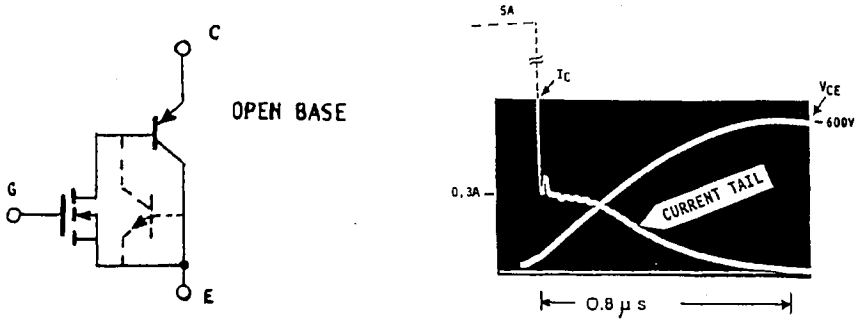


Fig. A4: IGBTs exhibit a turn-off collector current tail and significant turn-off losses in PWM circuits.

HOW TO CONTROL TURN-ON SWITCHING

Turn-on switching when the freewheeling diode is conducting leads to losses in a Power MOSFET and to similar losses in an IGBT (fig.A5). Increasing the di/dt of the drain current, or for an IGBT the collector current, leads to reduced turn-on losses. Reducing di/dt leads to higher losses, but makes the reverse recovery behaviour of the freewheeling diode "softer", thus reducing RFI problems.

When switching a short circuit, drain-source or collector-emitter voltage is at a constant high level while the drain or collector current increases at a certain di/dt (fig.A6). It stabilises at a certain current value, I_{SC} . The amplitude and duration of this current should be minimised in order to minimise energy stress on the semiconductor device. The output characteristics of the Power MOSFET IRFP450 helps us to understand how we can control di/dt and I_{SC} (fig.A7). The time needed to move the gate - source voltage from approximately 2V to about 6V determines the rate of rise (di/dt) of drain-current. The amplitude of a short circuit current, I_{SC} , is controlled through applied gate-source voltage. An IGBT behaves similary (fig.A7b). The di/dt and I_{SC} control can be implemented with a driver stage which monitors drain-source or collector-emitter voltage (fig.A8). The rate of rise of gate-voltage is controlled through R1. The Zener diode, D2, clamps the gate voltage to, for example, 6V and thus limits I_{SC}.

Under normal operating conditions, the drain-source or collector-emitter voltage decreases after the reverse recovery of the freewheeling diode, T1 blocks and the gate voltage can increase to about 10V.

Such a circuit greatly limits energy stress under short circuit conditions.

TURN-OFF SWITCHING

The switching device should not be damaged during turn-off switching. A power transistor datasheet usually contains the test circuit used for establishing the safe operating area (SOA) of the device (fig.A9). During operation the load line should not cross the limits of the SOA, but it is important to remember that the SOA itself is valid for given drive, junction temperature and dV/dt conditions.

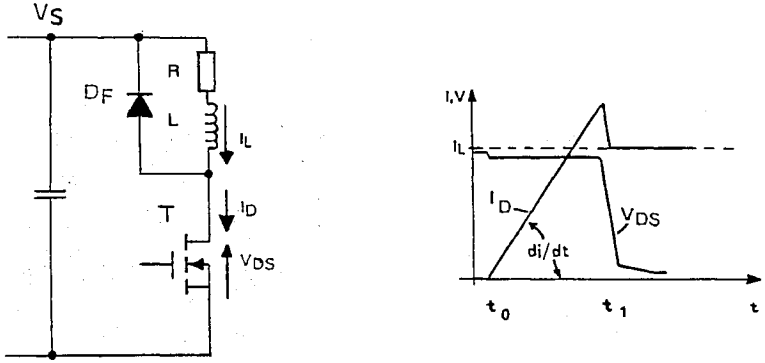


Fig. A5: Turn-on switching with a conducting freewheeling diode.

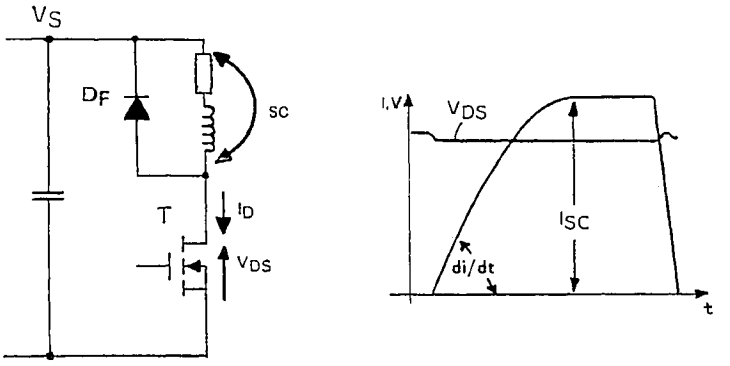
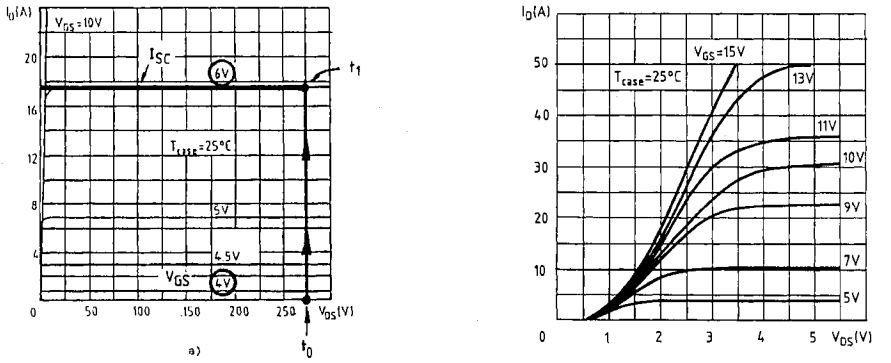


Fig. A6: Switching-on to a short circuit.



POWER MOSFET IRFP450 IGBT STGH20N50

Fig. A7: Output characteristics of a POWER MOSFET and an IGBT

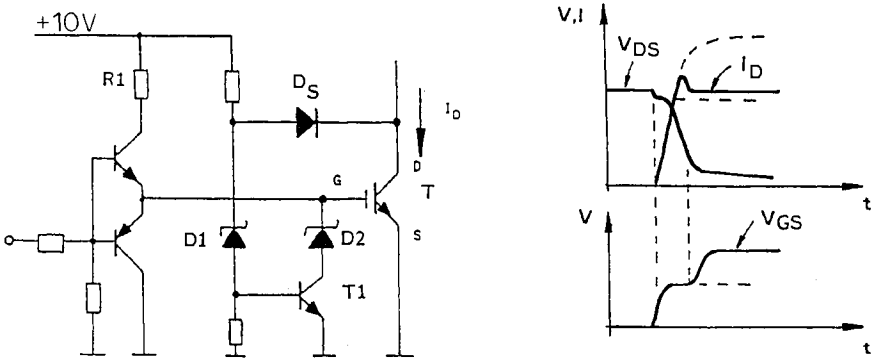
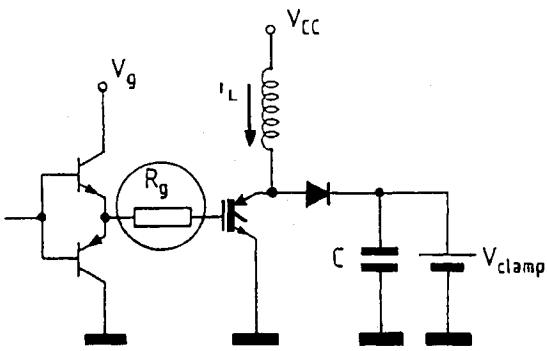
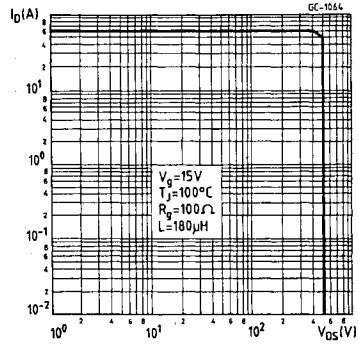


Fig. A8: Principle of driver stage controlling di/dt and short circuit current amplitude.



(a)

Reverse biased SOA



(b)

Fig. A9: Test circuit for the safe operating area (a) and SOA of IGBT STGH20N50 (b).

The rate of rise of collector-emitter-voltage (dv/dt), junction operating temperature, Tj, and drive conditions strongly affect the turn-off behaviour of IGBTs. In particular, the latching current is modified by these parameters.

The simplified equivalent circuit of an IGBT (fig.A10) can be used to understand modifications of latching current: transistor T1 conducts when the Power MOSFET structure is on; T2 will conduct when the voltage drop across Rs exceeds about 0.6V; the IGBT "latches" if this happens. Once the device latches removing the gate-emitter voltage will not turn off the device and the device may be destroyed.

The value of Rs doubles between 25°C and 125°C. The base-emitter threshold voltage of T2 diminishes at about 2mV/°K - both contributing to a reduction of latching current from 100% at 25°C to 30% at 125°C. At turn-off switching, a dv/dt between collector and emitter will add a capacitive current flowing into Rs, thus reducing latching current further and making it dependent upon dv/dt (fig.A11).

The resistance Rg between gate and emitter, strongly affects turn-off behaviour of Power MOSFETs and IGBTs. When the collector-emitter (drain-source) voltage increases, capacitive current flows into the drive circuit and leads to a voltage drop across Rg, thus maintaining V_{ge}(V_{gs}) at a dv/dt dependent level. The resistor Rg can be used to control dv/dt during turn-off. Thus turn-off losses, RFI and latching current can be set to desired values. The higher the Rg value, the lower the turn-off dv/dt and the higher the latching current.

B - DRIVER CIRCUITS FOR POWER MOSFETs AND IGBTs

Driver circuits have an influence on cost, performance and reliability of the whole power switching function.

Driver circuits should transform the logic level control signal into a suitable voltage/current waveform, exhibit low power consumption and often offer galvanic isolation between input and output.

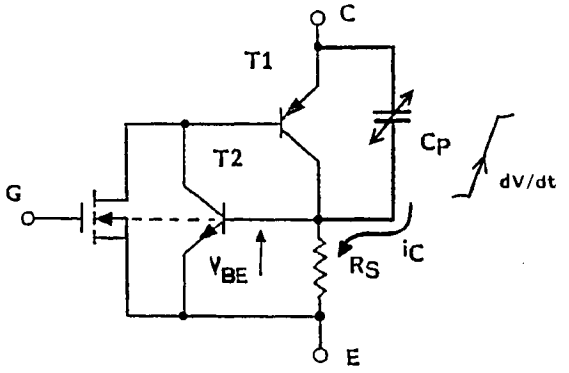


Fig. A10: Equivalent circuit of an IGBT for understanding the latching behaviour.

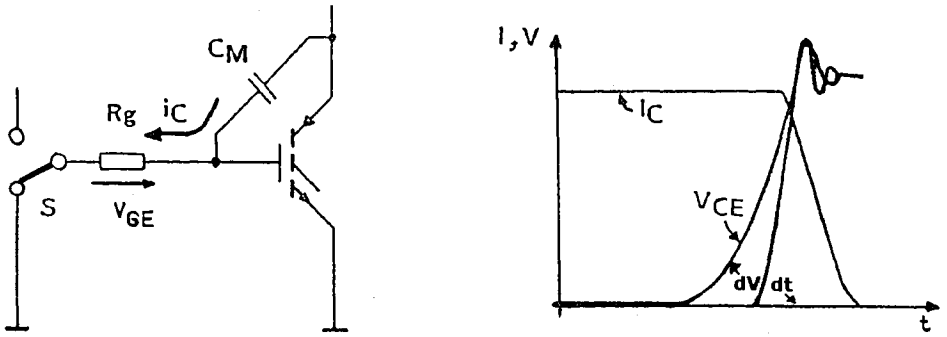


Fig. A11: Turn-off dv/dt as a function of gate resistance.

AVOIDING SPURIOUS TURN-ON

In bridge legs, Power MOSFETs and IGBTs are subject to dv/dt, when the opposite transistor switches on (fig.B1). This dv/dt will charge the parasitic drain-source or collector-gate capacitance and lead to a current flow out of the gate. If the voltage drop across Lp, Rp and Rg exceeds about 1V to 2V, the Power MOSFET/IGBT will conduct, leading to extra switching losses.

A driver stage having three different states gives a good compromise (fig.B2): dv/dt during turn-off switching can be set by means of Rg, thus obtaining excellent safety against latching and low RFI. After turn-off switching, a low driver output impedance gives good immunity against spurious conduction.

Nevertheless the parasitic resistance, Rp and inductance, Lp, should not exceed certain limits depending on dv/dt, die-size and parasitic package inductances.

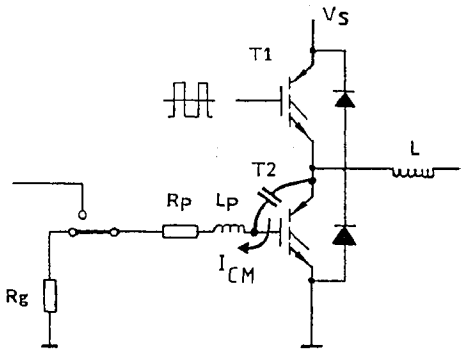


Fig. B1: Bridge leg with inductive load, where transistor T2 is subject to "passive" dv/dt.

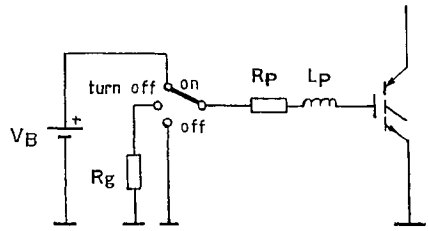


Fig. B2: Tri-state driver limiting turn-off dv/dt and having high immunity against passive dv/dt.

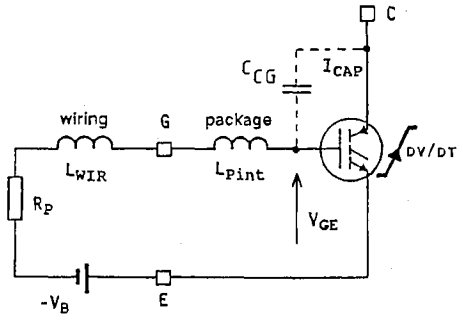


Fig. B3: IGBT with parasitic capacitances and inductances.

PACKAGE	MAXIMUM DRIVER IMPEDANCE
TO 220	10 Ω / 300 nH
TO 218	5 Ω / 150 nH
ISOTOP	2 Ω / 60 nH
TO 240	NEGATIVE BIAS
MODULE	NEGATIVE BIAS

dV/dt = 10kV/ µs

TABLE I: Maximum driver impedance as a function of device package.

MAXIMUM DRIVER IMPEDANCE/ NEGATIVE BIAS?

During dv/dt, the gate voltage should not exceed about 1 volt. The maximum driver impedance must be fixed at a value that is dependent on the die size, which is related to C_{CG} and the parasitic package inductance $Lp_{(int)}$ (fig.B3). If $Lp_{(int)}$ is very high, negative bias may be required in order to avoid spurious conduction. Table I indicates the maximum required driver impedance for a dv/dt of 10kV/µs.

PULSE CONTROLLED DRIVER SUITABLE FOR 0 - 1 MHz OPERATION

When applying a voltage pulse with, for example, a 10V amplitude and 500ns duration, to the gate of a Power MOSFET (T) or an IGBT,

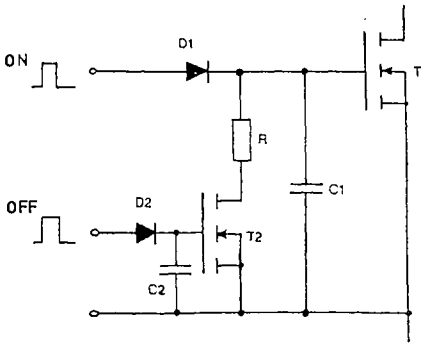


Fig. B4: Pulse controlled driver circuit memorizing on-state and off-state.

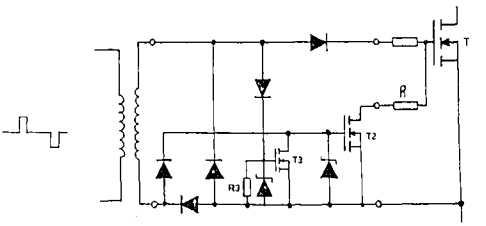


Fig. B5: Pulse controlled drive with transformer isolation. Even though there is no auxiliary supply, any pulse width, at virtually any relevant frequency, can be controlled.

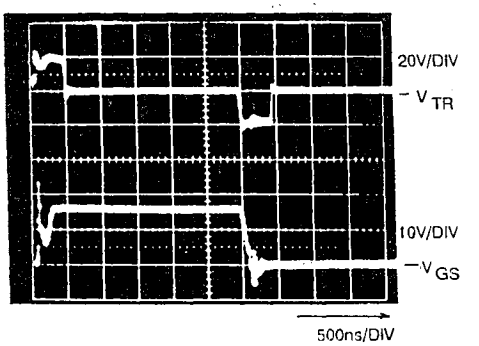


Fig. B6: Transformer output signal at gate-emitter/ gate-source voltage with pulse controlled driver.

charge will be stored in the gate capacitance fig.B4). Thus the power device will remain conducting, even after removal of the input ulse. This is called the "memory-effect".
f a similar pulse is applied to a second Power MOSFET (T2), the latter will conduct, lischarge the gate of Power MOSFET (T) and emain conducting - the off-state is memorised. Supposing R is low enough, dv/dt applied to Power MOSFET (T) does not lead to spurious conduction.

It is possible to add a pulse transformer for galvanic isolation and a third Power MOSFET (or bipolar transistor) can be used to discharge the gate of T2, whenever an "on-signal" is generated (fig.B5).

When using the "memory-effect", only pulses of about 5µVs have to be transmitted by the transformer; a very small toroid transformer is sufficient. Figure B6 shows the transformer output voltage and resulting gate-source/gate-emitter voltage. The circuit can handle any duty cycle.

RESONANT DRIVER FOR POWER MOSFETs AND IGBTs

Power MOSFET and IGBT driver circuits for high frequency conversion should drive the power devices in such away that the resulting switching losses are low. Even at high

operating frequency, the driver circuit should have negligible power consumption. Power MOSFETs and IGBTs are charge controlled devices. For turn-on one has to supply a certain amount of charge into the gate. For turn-off, charge has to be removed.

During switching, one can consider the drain source path of a Power MOSFET as a fast varying current source - moving in a drive determined time from conduction to zero current or vice versa.

Driving the gate with a rectangular shape current (constant amplitude during a certain amount of time) would enable faster charge removal and faster switching but it is difficult to realise. Resonant gate drive with an inductance between driver and gate is easy to realise - one can even use an increased parasitic wiring inductance. With this approach, the time to charge or discharge the gate can be reduced by a factor of about two. Depending on the circuit, gate charge can be recovered and gate drive power consumption reduced.

One of the possible resonant gate driver circuits can be supplied from a single 5V source, and it generates a ten volt gate voltage for conduction and a negative bias for the off-state.

Conventional gate driver circuits charge and discharge a Power MOSFET's input capacitance through resistors and a parasitic inductance Lp (fig.B7).

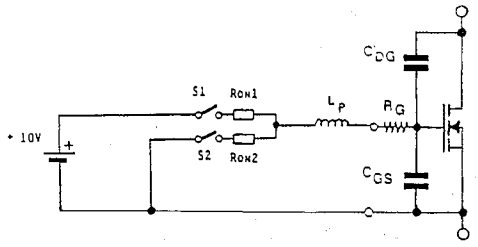


Fig. B7: Principle of conventional driver circuit with simplified equivalent circuit of MOSFET

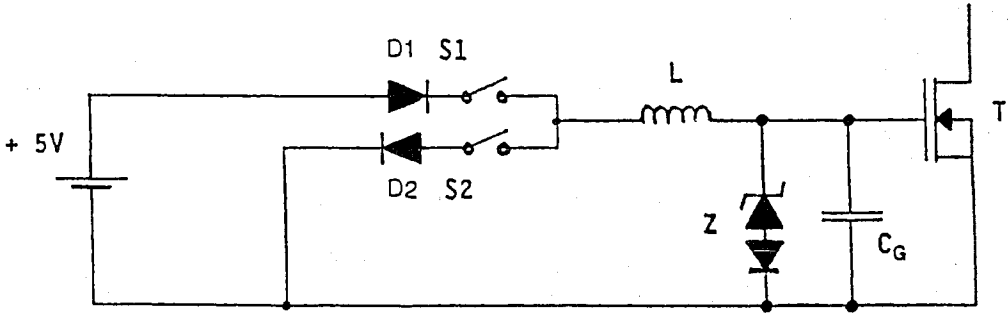


Fig. B8: Resonant gate driver. Power consumtion of the driver is 1/4 of a conventional driver.

At turn-on switching $E = {}^1/_2 CV^2$ is lost in $R_{on}1$. At turn-off switching, same amount of energy is lost in $R_{on}2$. When driving power Power MOSFETs at high frequency these losses become significant and should be reduced. Resonance effects can be used for this purpose (fig.B8).

When driver transistor S1 is turned on; a sinusoidal current flows into the gate capacitance of the power device. The gate voltage reaches about twice the driver supply voltage $V_{aux.}$ Thus, a Power MOSFET requiring a gate-source voltage of 10V can be driven from a 5V-supply. The diode D1 avoids discharging the gate. For turn-off switching, S2 is closed, a sinusoidal current removes the charge from the gate. The gate-source, or gate-emitter in the case of an IGBT, voltage of the power device is inverted (negative). Most of the stored energy is used to generate a negative bias voltage (fig.B9). Diode D2 avoids discharging the negative gate charge. Due to resonance overvoltage, gate voltage would reach the breakdown voltage of the gate oxide after a number of switching cycles.

A Zener diode, Z, has to be used to limit gate voltage. The energy consumption of a resonant gate driver is about a quarter of that of a conventional driver.

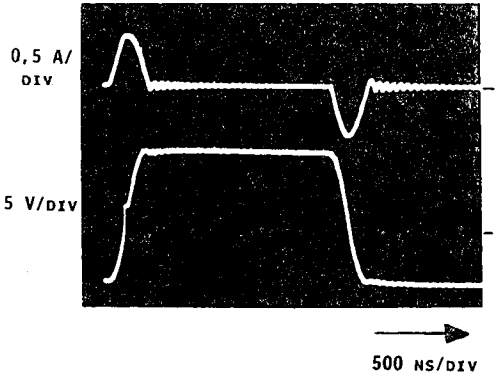
The charging and discharging of a capacitor with a given peak current, is achieved more rapidly through an inductance of an appropriate value. Resonance driver circuits therefore have the ability for the fast switching of power devices (fig.B10).

C - LOSS REDUCTION IN PWM CONVERTERS

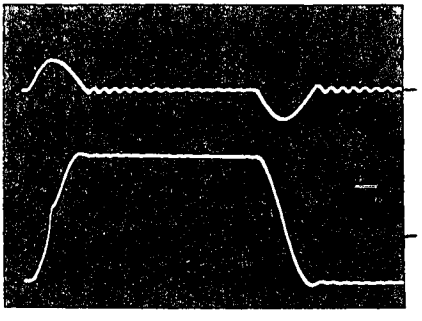
PARASITIC CAPACITANCES CONTRIBUTE TO LOSSES

The influence of the Power MOSFET output capacitance is negligible in low voltage, low frequency applications. This changes greatly when increasing operating voltage and switching frequency. The effect of the output capacitance, C_{out}, has to be taken into account in high voltage, high frequency applications.

For switching loss evaluation, it is possible to



a) POWER - MOSFET IRFP450



b) IGBT STGH20N50

Fig. B9: Gate-current and gate-source/gate-emitter voltage waveforms.

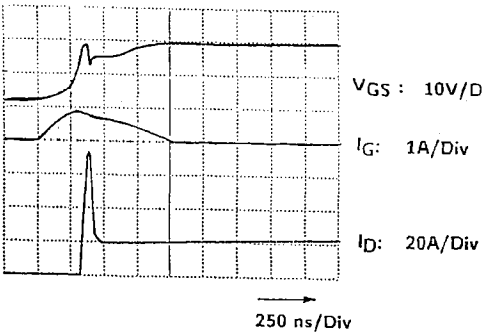


Fig. B10: An ISOFET TSD5MG40V (1000V, 0.7Ω) driven by a resonant driver. Switching losses are greatly reduced.

use a simplified equivalent circuit of Power MOSFETs (fig.C1).

The function of the output capacitance can be understood as a built-in capacitive snubber. At turn-off switching, this capacitance is charged from V_{on} to the maximum voltage $V_{DS(off)}$ applied to the Power MOSFET (fig.C2). Once charged, the capacitor contains energy. Depending on the converter structure, this energy may either be recovered or dissipated.

In PWM circuits (fig.C3) the Power MOSFET discharges its output capacitance at turn-on switching and ($0.5 * C_{out} * V_{DS(off)}^2$) Joules are lost. ($C_{out}$ is the effective output capacitance of the Power MOSFET, $V_{DS(off)}$ the drain source voltage just before turn-on switching).

The discharge-current flows inside the Power MOSFET, it cannot be observed on an oscilloscope.

HOW TO MEASURE STORED CHARGE ?

A simple circuit can be used for evaluation and specification of the output capacitance (fig.C4): The device under test (DUT) is connected to a high voltage supply via a resistor. A second Power MOSFET is paralleled to the DUT. The Power MOSFET under test is permanantly blocked, the second Power MOSFET switches periodically. At turn-on of the latter, you can observe the discharge current and time on an oscilloscope and determine the amount of charge, energy and the value of the capacitance.

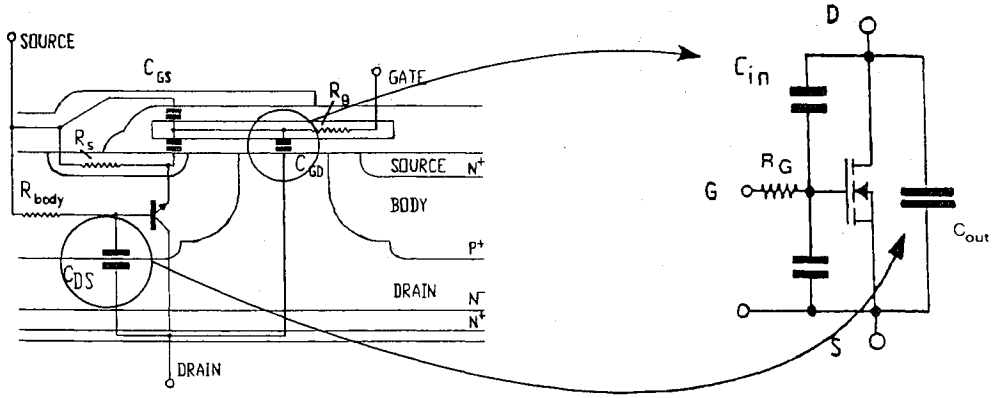


Fig. C1: Power MOSFET cross section - a) parasitic capacitors b) equivalent circuit.

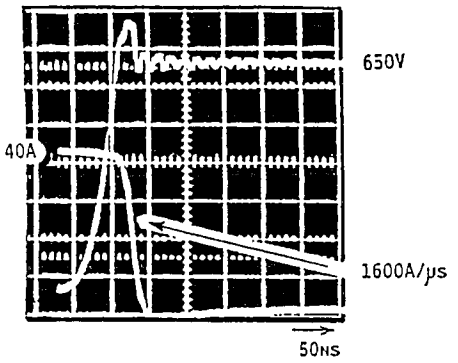


Fig. C2: Turn-off switching of a 1000V-0.7Ω Power MOSFET.

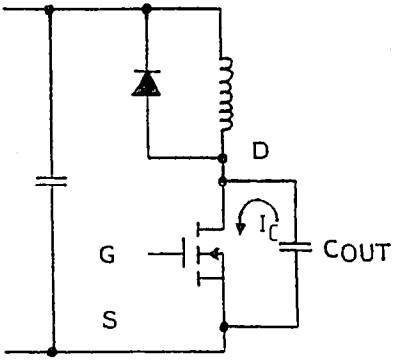
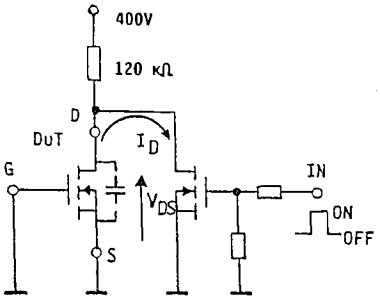


Fig. C3: Discharging output capacitance during turn-on switching.



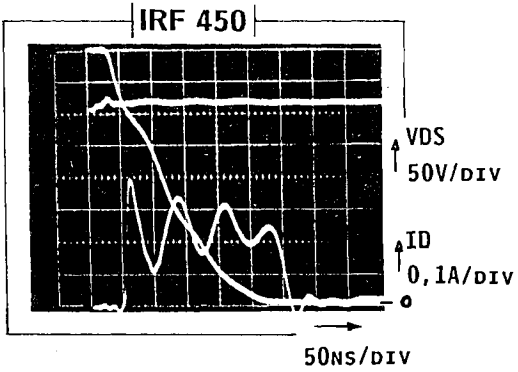


Fig. C4: Evaluation of Power MOSFET output capacitance,
a) test circuit,
b) waveforms with IRF450, $V_{DS(off)}$ = 400V.

ON-RESISTANCE - CAPACITIVE LOSSES

A Power MOSFET's contribution to converter losses are conduction, switching and gate drive losses. Conduction losses can be reduced by increasing the die size, leading to smaller on-resistance. Increased die size introduces increased output capacitance and switching losses (fig.C5).

Minimum losses are obtained when losses due to discharge of the output capacitance and conduction losses are equal (fig.C6). Optimisation depends on the supply voltage, the converter structure and the switching frequency.

The consequences are: from a certain

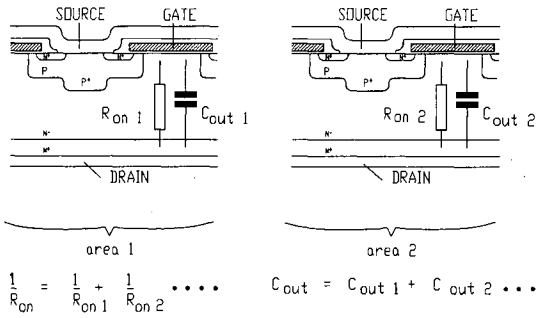


Fig. C5: Power MOSFET cross section. Increase of silicon area or paralleling discrete devices reduces on-resistance but increases output capacitance.

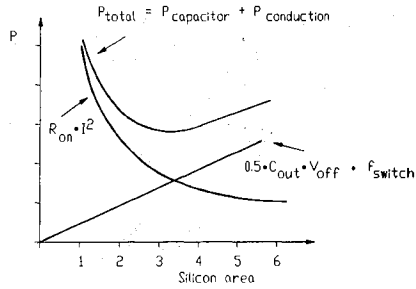


Fig. C6: Conduction and switching losses versus area. Total loss has a frequency dependent minimum.

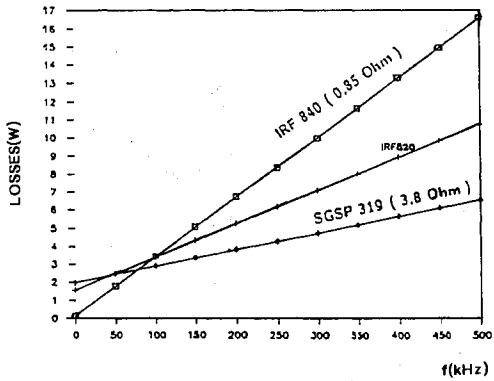


Fig. C7: Total losses versus frequency calculated asymmetrically with three 500V Power MOSFETs (same technology, different on-resistance).

switching frequency upwards, a size reduction of the Power MOSFET leads to improved efficiency, even when it is associated with an increased on-resistance.

In SMPS applications with PWM and with a maximum drain-source voltage of 400V, switching losses due to the discharge of the output capacitance are dominant at switching frequencies exceeding 100kHz to 150kHz (fig.C7). For loss reduction in SMPS operating below 100kHz Power MOSFETs with low on-resistance are preferable - above 100kHz Power MOSFETs with low output capacitance and higher on-resistance are better.

INFLUENCE OF TOPOLOGY

Comparing energy stored in the two Power MOSFETs of an asymmetrical half bridge

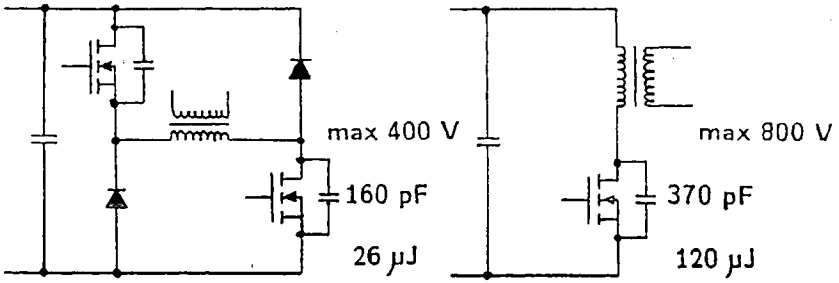


Fig. C8: Energy stored in the output capacitance of two 0.4Ω 1000V Power MOSFETs and in one 0.8 Ω - 1000V MOSFET.

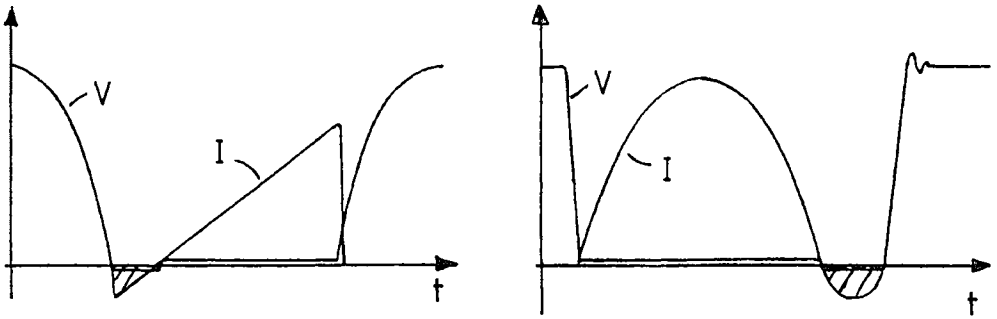


Fig. D1: Typical waveforms with zero voltage switching (a) and zero current switching (b).

flyback converter with a single switch flyback shows that significantly more energy is stored in the high voltage device used in the single switch flyback (fig.C8). It is possible to estimate that between 30% to 60% of that energy is dissipated.

D - POWER MOSFETs AND IGBTs IN RESONANT CONVERTERS

A large number of different resonant and quasi-resonant topologies exist. For the purpose of choosing semiconductors, one can distinguish two basic modes of operation: Zero voltage switching and zero current switching (fig.D1). The other modes are in between. IGBTs are as simple to drive as Power MOSFETs and offer, in the area of high voltage switching, much better on-resistance per unit silicon area and may offer less conduction losses or lower costs. Depending on the converter topology, either Power MOSFETs or IGBTs may be more suitable.

ZERO VOLTAGE SWITCHING

A typical circuit with zero voltage switching consists in a switch, T, with paralleled capacitor and series choke (fig.D2). The whole is supplied from a voltage source. During conduction in the switch, the choke current increases with time. At turn-off, the voltage across C and the switch increases as a sinuoidal function and may reach several times the supply voltage (fig.D3). Afterwards it swings back to below zero where it is clamped by the diode. The output capacitance of the semiconductor switch and the capacitor are discharged via the inductance. Thus the energy is recovered. The only losses are due to the parasitic resistance Rs, which is a part of the Power MOSFET's on-resistance. Increasing silicon area reduces on-resistance, Ron, and parasitic damping resistance, Rs. An increase of silicon area is not paid for with an increase of capacitive loss. Power MOSFET switching losses can be considered as negligible with this operation mode.
High voltage IGBTs exhibit significantly lower conduction losses than high voltage Power MOSFETs with similar die size. The IGBT can be understood as a Power MOSFET driving a PNP-bipolar transistor (fig.D3). The on-resistance of the Power MOSFET is virtually divided by the bipolar gain. It is possible to compare the switching to that of a high voltage PNP-transistor, switching with open base - resulting in a collector current tail. This tail cannot be ignored as the resulting loss is a major limitation for the application of IGBTs in converters with zero voltage switching.

ZERO CURRENT SWITCHING

A typical circuit using zero current switching consists of a switch with a series choke, the whole paralleled with a capacitor and supplied

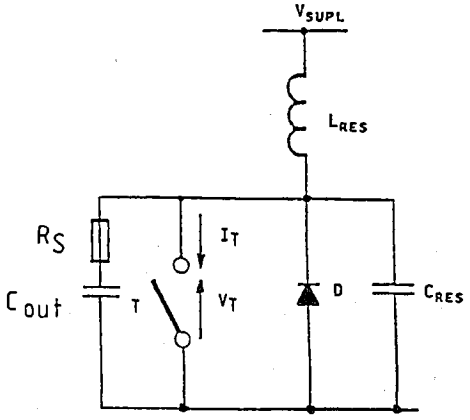


Fig. D2: Typical circuit with zero voltage switching.

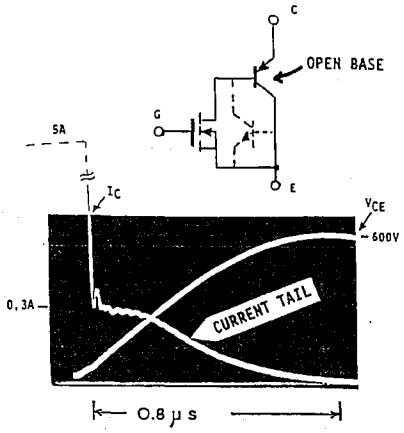


Fig. D3: Equivalent circuit of an IGBT and waveforms in a ZVS-circuit. Even a small tail current leads to significant turn-off energy loss.

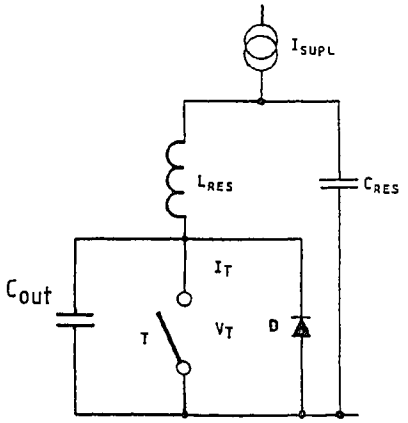


Fig. D4: Typical circuit with zero current switching.

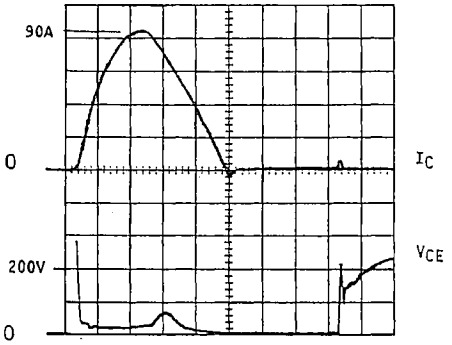


Fig. D5: Collector current and collector emitter voltage of a 10 Amp-500Volt IGBT (STGP10N50) with zero current switching.

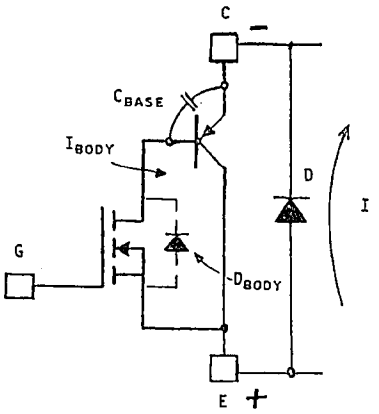


Fig. D6: Equivalent circuit explaining the absence of a current tail. When the collector-emitter voltage of the IGBT is negative, a current flows thourgh the body diode into the base of the PNP. This current blocks the PNP structure efficiently.

from a current source (fig.D4). At turn-on, the current through the switch increases with a sinuoidal function and then swings below zero (fig.D1). The negative half wave flows through the diode.

At turn-on switching, output capacitance is discharged into the switch; capacitive losses similar to PWM-converters can be observed. IGBTs do not show current tail in this configuration! After the zero crossing of the collector current a short negative current pulse can be observed (fig.D5). It flows through the body diode into the base of the PNP, sweeping stored carriers away, thus avoiding current tail and corresponding losses (fig.D6). IGBTs are very suitable for resonance converters with zero current switching where they offer a better cost/performance compromise than Power MOSFETs and can be operated at frequencies of several hundred kHz.

RESONANCE IN PWM CIRCUITS

The advantages of zero current switching with IGBTs can also be used in PWM converters: (this is similar to forced switching circuits as used with SCRs - improved MORGAN circuit (fig.D7).

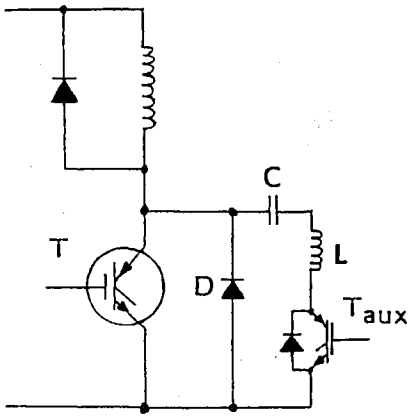


Fig. D7: Circuit using resonance in a PWM converter. With this circuit the IGBT is virtually free from turn-off losses and can be used at inaudible frequencies.

With these circuits it is possible to take advantage of the high current handling capability of IGBTs without any risk of loosing control as is the case with these earlier thyristor circuits. Thus PWM operation of IGBTs at inaudible switching frequencies is possible.

CONCLUSION

Investing more effort into understanding and designing driver circuitry for Power MOSFETs and IGBTs opens the way to better performance, lower costs and new applications.

Through suitable gate control, Power MOSFETs can be made even faster. However, it is also possible to slow them down in order to reduce RFI-filter requirements in phase control, soft start circuits etc...

Through zero current mode operation, the current tail of IGBTs can be avoided, and then IGBTs can be operated in PWM circuits at up to 20kHz and resonant converters even at 200kHz. Maybe some of the well proven thyristor circuit topologies could be used and even improved with IGBTs.

The key to all these new applications with improved performance is in forgetting prejudice and thinking about what really happens inside the power semiconductor devices.

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