SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SWITCHING WITH IGBTS: HOW TO OBTAIN A BETTER PERFORMANCE

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ABSTRACT

IGBTs are now being used in a variety of switching applications due to their attractive characteristics, particularly their current density, ruggedness and gate driving circuit. To exploit the best aspects of IGBTs it is necessary to understand how their switching performance can be controlled by the designer and how much the voltage and current waveforms can be shaped to obtain an acceptable compromise in terms of switching speed, ruggedness, power dissipation and EMI.

This paper, starting with voltage and current waveform analysis, highlights both the device and driving circuit characteristics which govern the switching. It suggests, by using a simple driving circuit, how to control both voltage and current slopes, independently.

The influence of negative gate bias and driving impedance versus dV/dt ruggedness are analyzed.

Finally the IGBTs switching behaviour, when connected in parallel, is examined.

1 - ANALYSIS OF PARAMETERS WHICH INFLUENCE SWITCHING WAVEFORMS

The switching behaviour of IGBTs is affected by the unavoidable parasitic capacitance of the structure. Moreover the turn-off losses are strongly dependent on the characteristic of the tailing effect on the collector current during turn-off. Nevertheless switching losses can be predicted and then limited to an acceptable value, that is compatible with the need for safe and noiseless switching. The main parameters governing switching behaviour: gate bias, driving impedance, stray inductances, gate charge must also be taken into account.

Fig. 1 shows a schematic circuit where the parasitic inductances which influence switching behaviour are highlighted.

In the following discussion it has been assumed that the stray inductances are small enough so that dI/dt >> Vcc/(Ls+Lc+Ld).

1.1 TURN-ON

When the freewheeling diode is conducting during turn-on switching (fig. 2) , increased losses occur in the diode if the dI/dt in the IGBT collector is increased. However the losses in the IGBT decrease with increasing dI/dt in the IGBT collector (fig. 3).

Reducing dI/dt leads to higher losses in the power switch but it makes the reverse recovery behaviour of the freewheeling diode softer, thus reducing EMI problems. Fig. 4 shows dI/dt versus Rg with Ls as a parameter. Ls includes both stray inductances due to package and external inductances due to source grounding layout. These inductances strongly influence dI/dt at turn-on because they act as negative feedback to the gate thus reducing the effective voltage applied to the device. This effect is emphasized in fig. 5 where the collector and gate current are shown.

The gate voltage was set at 15 V to give a low Vcesat and also because this value is applied as a standard gate voltage when various device characteristics are defined in data sheets.

1.2 TURN-OFF

The IGBTs turn-off (fig. 6) can be divided into three consecutive phases:

a) the gate voltage begins to decrease until it reaches the value when the Miller effect occurs;during this phase the collector voltage increases slightly changing the output characteristics with Ic=constant.

b) this phase is the Miller effect and the gate voltage remains constant because of modulation of the collector-gate capacitance.
This is due to collector voltage rapidly increasing to its maximum value.

c) the collector current begins to fall quickly (it is related to the turn-off of the MOS part of the IGBT structure) then it continues with a "tail" which is due to recombination of minority carriers in the substrate.

This tail, which causes the major losses, is strongly related to technology and its effect can not be mitigated by driving circuit.

After the collector current, collector voltage and junction temperature has been determined, turn-off losses can be controlled only during phase b) varying dv/dt through Rg while losses occurring during phase c) are slightly influenced by the driving circuit.

Increasing dV/dt decreases losses but it is necessary to take care not to exceed the RBSOA boundaries which also depend on junction temperature, collector current and collector voltage.

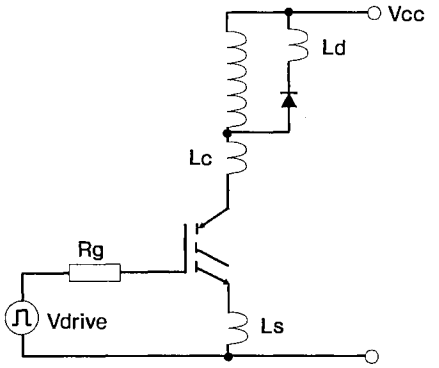

Fig. 1: Parasitic inductances influencing the switching behaviour

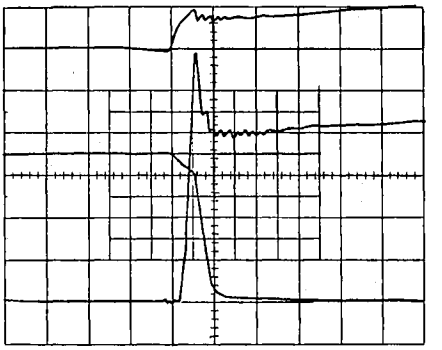

Fig. 2: Turn-on switching during freewheeling diode conduction

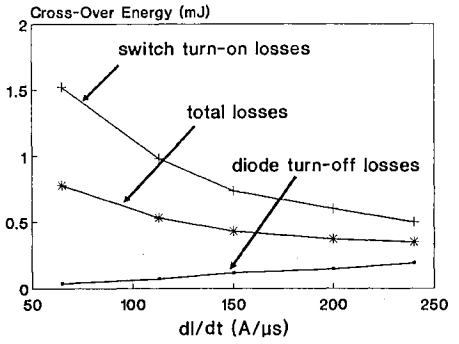

Fig. 3: Switching losses comparison

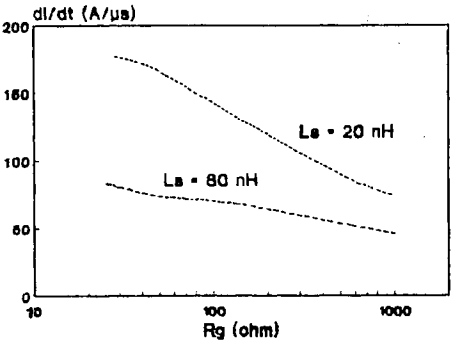

Fig. 4: Rg and Ls influence on dI/dt during turn-on

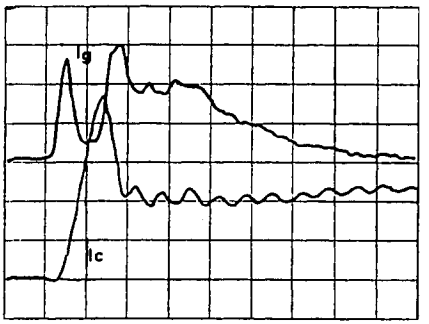

Fig. 5: Ic and Ig during turn-on

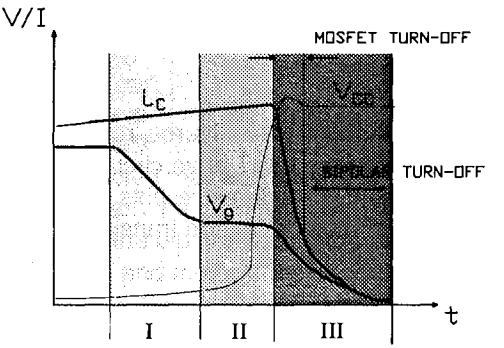

Fig. 6: IGBTs turn-off

2 - HOW TO MANAGE DI/DT AND DV/DT

Useful information about switching behaviour of IGBTs can be obtained from the gate charge curve. Even if the measuring conditions are quite different from the operating ones the total charge supplied to gate during switching is the same. The switching speed of a voltage driven device is strictly related to the rate of supplying charge to the gate input. This is true for IGBTs too, except during the falling edge of the collector current.

If we are able to control the rate of supplying this charge, i.e. if we can manage the amplitude of the gate current during switching we can independently vary both the voltage and the current slope.

2.2 TURN-ON

The driving circuit shown in fig. 7 allows dI/dt to be varied through R1 but at the same time this resistance fixes the collector voltage slope. Increasing R1 leads to a lower dI/dt and also to a lower dV/dt which increases turn-on losses.

It would be useful to have a di/dt low enough to reduce EMI problems and a dV/dt fast enough to keep power losses to a minimum. It is possible to achieve that using a driving circuit which operates according to the schematic shown in fig. 8.

The current slope is fixed by R1 and voltage slope by R2 by turning Q2 on after Q1 with a suitable delay. The waveforms in figures 9a and 9b show the difference between the standard circuit and the improved version.

2.3 TURN-OFF

The driving circuit can only control the slope of the collector voltage (fig. 10) and only slightly influences the fall of the collector current which is responsible of the major losses due to the tailed turn-off.

Figures 11, 12 and 13 show the effect of Vc, Ic and Tj on the amplitude of the tail of the collector current.

To minimize turn-off losses it is best to choose a device whose characteristics matches better the required operating conditions in terms of Vc, Ic and Tj.

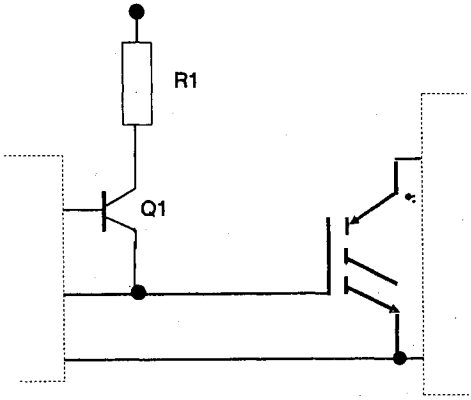

Fig. 7: Standard driving circuit

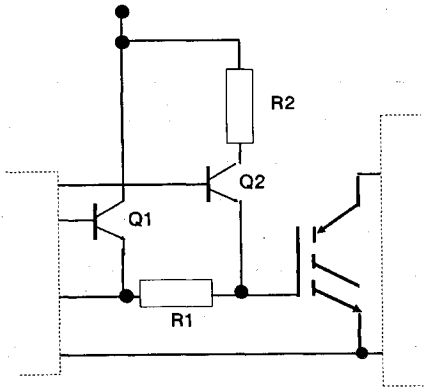

Fig. 8: Improved driving circuit

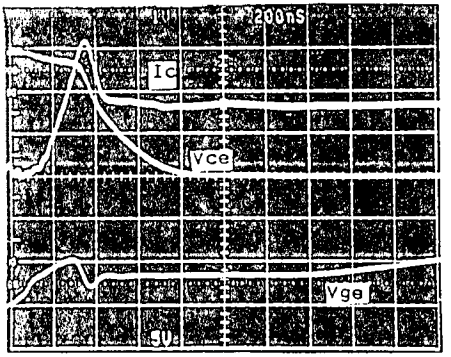

Fig. 9 a: Switching waveforms with standard driving circuit

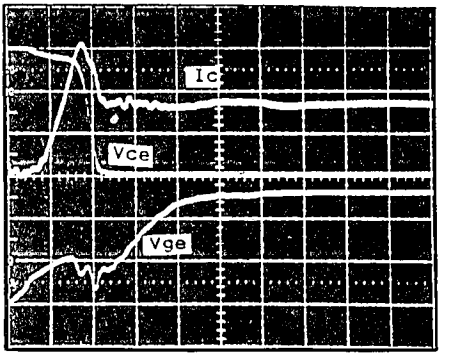

Fig. 9 b: Switching waveforms with improved driving circuit

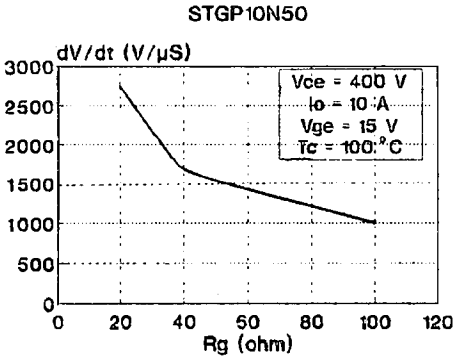

Fig. 10: Rg influence on dV/dt during turn-off

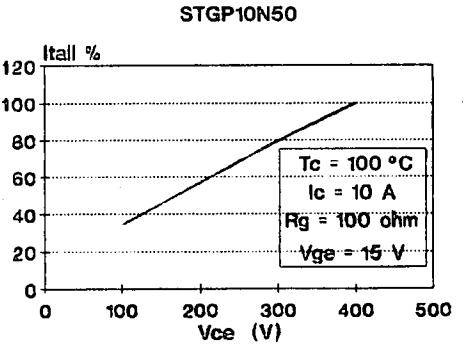

Fig. 11: I_{tail} versus collector voltage

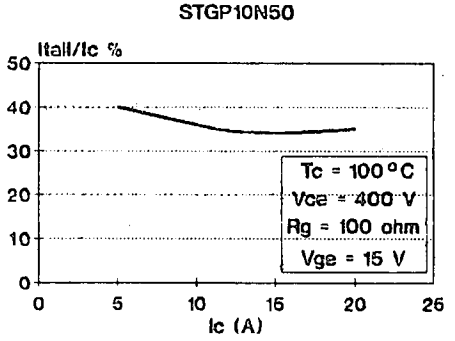

Fig. 12: I_{tail} versus collector current

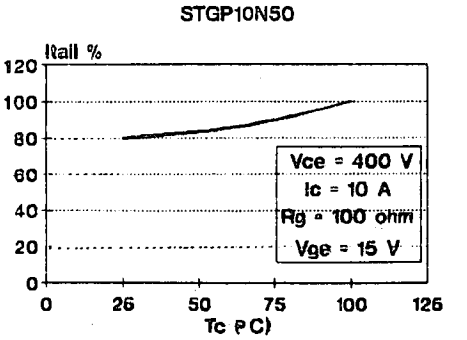

Fig. 13: I_{tail} versus Tj

3 - HOW TO AVOID DV/DT PROBLEMS

The spurious turn-on problem due to dV/dt is typical of the circuit shown in fig. 14.
The free-wheeling diodes in parallel with each IGBT are turned off during the opposite IGBT turn-on generating a dV/dt whose value depends on :

- opposite IGBT turn-on speed (dI/dt)
- free-wheeling diode "softness"
- wiring inductances
- gate bias and driving impedance

This applied dv/dt, acting through the collector-gate capacitance (fig.15) causes the gate voltage to rise turning the device on and leading to additional losses. This undesired effect is emphasized when temperature increases because of temperature dependence of Vth and gfs.
It is possible to avoid this effect either minimizing the dv/dt value or making the device less sensitive to dV/dt by a driving circuit specifically designed for this purpose or combining the two techniques above mentioned.
The first item requires using fast soft recovery diodes, reducing wiring length and turning the IGBTs on slowly. The second one requires the driving impedance to be fixed at such low value that the gate voltage can not exceed the threshold voltage during dV/dt. The value of this driving impedance depends on die-size of the device: fig. 16 shows the Rge needed to avoid spurious turn-on due to dv/dt.
Another way of avoiding spurious turn-on is to bias the gate negatively. Fig. 17 shows the different behaviour of gate voltage with and without negative bias.
The lower peak of the gate voltage is due to the different equivalent input capacitance when the gate is negatively biased.

4 - PARALLELED IGBTS SWITCHING BEHAVIOUR

The influence of the spread of parameters, of drive circuit and lay-out unbalance was investigated splitting the analysis as follows:

a) driving IGBTs with one gate resistance for each device (fig. 18);
b) driving IGBTs with a common gate resistance for all the devices (fig.19);
c) unbalancing emitter wire connection (fig. 20);
d) paralleling devices with the maximum spread of the parameters.

The performed analysis pointed out that voltage and collector current waveforms are stable even in the worst case conditions which occur when the gates are driven with a common resistance and the wiring inductances are strongly unbalanced.
In detail :
- IGBTs behaviour during turn-on is not very different in a) or b) conditions (fig. 21 and fig. 22).
If the paralleled devices have different storage times, driving the gates with one resistance for each device has the drawback shown in fig. 23: the collector current of the device having the smaller storage time begins to fall before the other one do.
Consequently, because of the inductive load, the 2nd IGBT has to switch-off a collector current greater than the other device thus increasing storage current unbalance. Driving the gates with only one gate resistance minimizes this effect (fig. 24): the device with the higher storage time holds the gate voltage to "V_{th} + I_c/gfs" until the fall time phase, so equalizing the storage times.
- The effect of a poorly balanced emitter connection is highlighted during the rising and the falling edge of the collector current.

Fig. 25 shows the peak current unbalance, during turn-on, when the condition c) occurs. In the case shown $\Delta Ls = 0.15\mu H$.

Fig. 26 and fig. 27 show the corresponding effect during turn-off: wiring inductance imbalance affects only the power-MOSFET phase.

This behaviour creates negligible switching losses imbalance compared with the total turn-off ones.The current unbalance just before current fall affects the tail amplitude and it can create significant imbalance in the switching losses.

- IGBTs with the maximum spread in parameter values were paralleled; the comparison of current waveforms in fig. 21 and fig. 22 demonstrates that, during turn-on, the influence of parameter spread is low (Ls $\approx$ 30 nH).

The spread of IGBTs parameters (gfs, Vth, gate-charge) leads to different storage times and causes current imbalance thus creating switching losses imbalance.

Current imbalance due to the IGBTs parameter spread can be calculated with the equations (2) and (3).

The curve of fig. 28 shows the imbalance in switching losses between two devices where the Vth and gfs values are the limits of the parameter spread.

$$I_{load} = I_{1st} + I_{2st} = V_{GE}\,(g_{fs1} + g_{fs2}) - (g_{fs1}V_{th1} + g_{fs2}V_{th2}) \quad (2)$$

$$I_{storage} = I_{1st} - I_{2st} = V_{GE}\,(g_{fs1} - g_{fs2}) - (g_{fs1}V_{th1} - g_{fs2}V_{th2}) \quad (3)$$

CONCLUSION

A careful analysis of circuit and device parameters, influencing switching waveforms, was carried out taking into account negative gate bias, dV/dt influence and effects of device paralleling.

The following statements were explained:

- it is possible to manage separately both the current and the voltage slope except the collector current tail;

- negative gate bias reduces spurious turn on caused by dV/dt in bridge configurations;

- negative gate bias without Rg adjustment reduces the RBSOA because of increased dV/dt;

- common resistor on the gate of paralleled devices improves switching losses balance;

- stray inductance on emitter connection reduces switching speed and can causes losses unbalance in paralleled devices;

Performance improvements obtained by optimization of gate driving circuit involve cost increases. It is task of the system designer to define a good trade off between cost and performances.

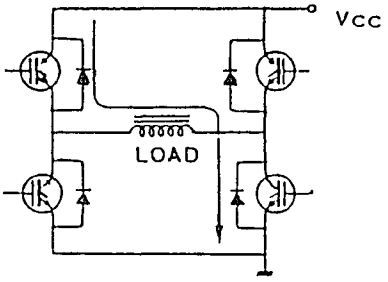

Fig. 14: Typical circuit where dV/dt conduction can occur

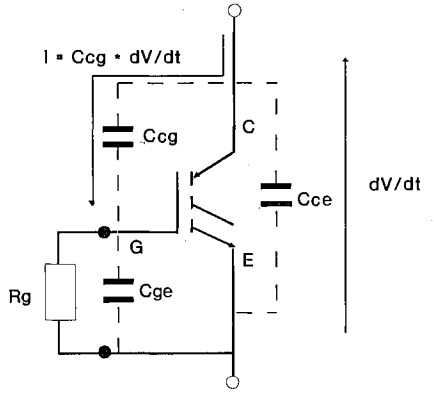

Fig. 15: Current flow through IGBT capacitance due to dV/dt

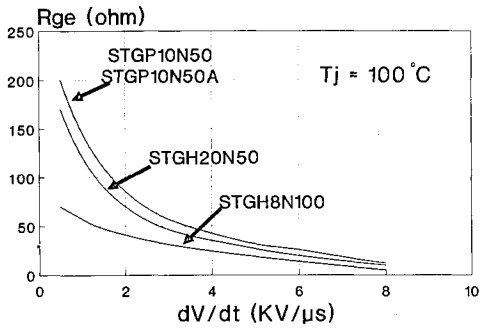

Fig. 16: Rge values that avoid dV/dt conduction versus dV/dt

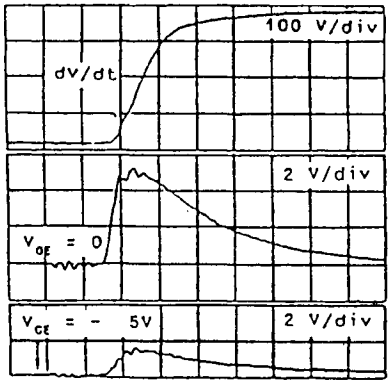

Fig. 17: Comparison of gate voltage behaviour with and without negative bias

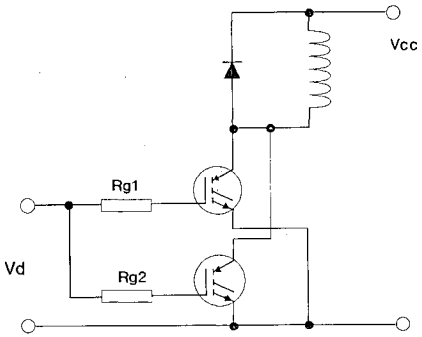

Fig. 18: Driving with separate gate resistance

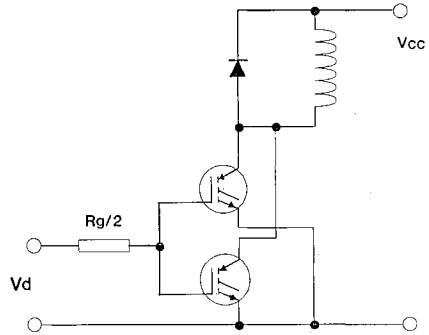

Fig. 19: Driving with one gate resistance

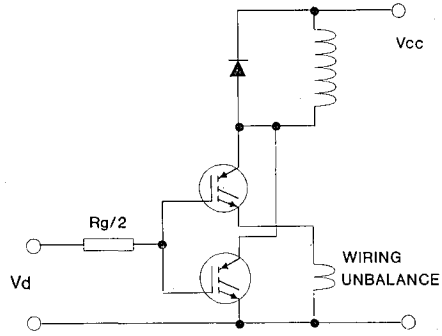

Fig. 20: Emitter grounding unbalance

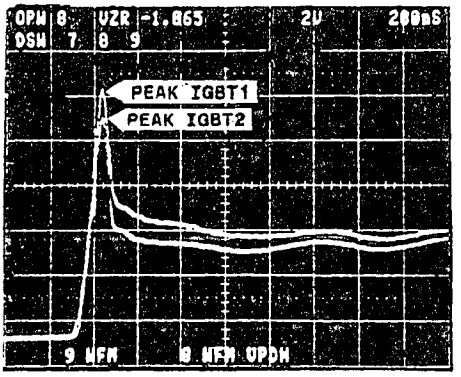

Fig. 21: Turn-on with separate gate drive (fig. 18) of an STGH8N100. I_c = 2A/div

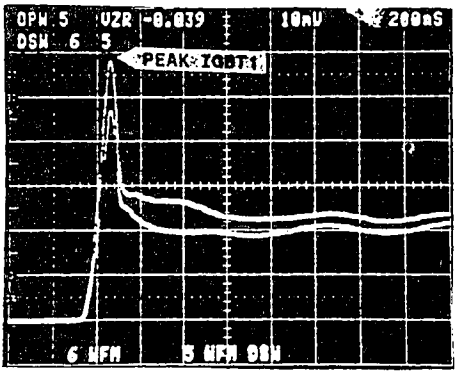

Fig. 22: Turn-on with one gate resistance (fig. 19) of an STGH8N100. I_c = 2A/div

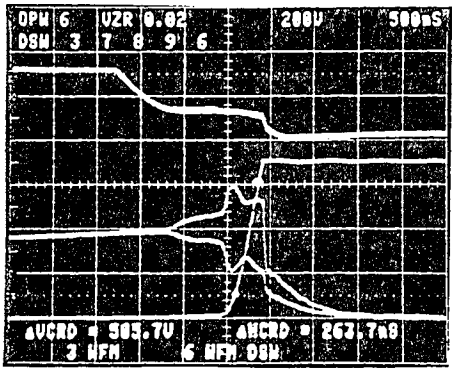

Fig. 23: Effect of separate gate drive on storage current waveforms. I_c = 2A/div, V_{ce} = 200/div, V_{ge} = 10/div

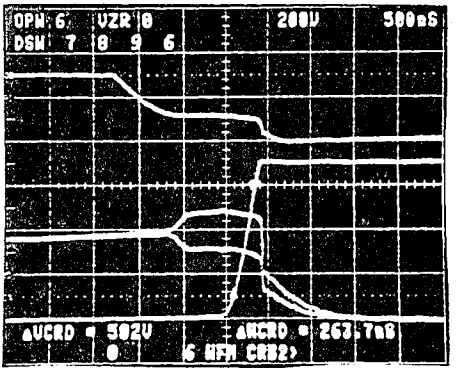

Fig. 24: Turn-off with one gate resistance. I_c = 2A/div, V_{ce} = 200/div, V_{ge} = 10/div

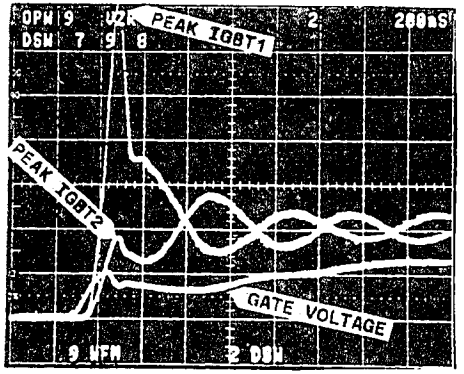

Fig. 25: Turn-on with unbalanced emitter-ground connection (fig. 20). I_c = 2A/div

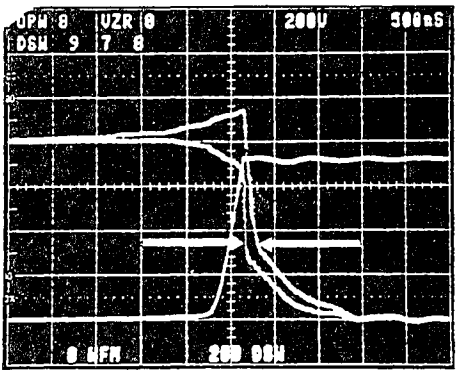

Fig. 26: Turn-off with unbalanced emitter-ground connection (fig. 20). I_c = 2A/div

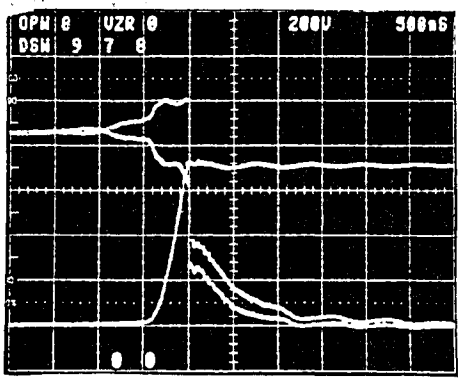

Fig. 27: Turn-off current waveforms with balanced gate-emetter wiring (fig. 19). I_c = 2A/div

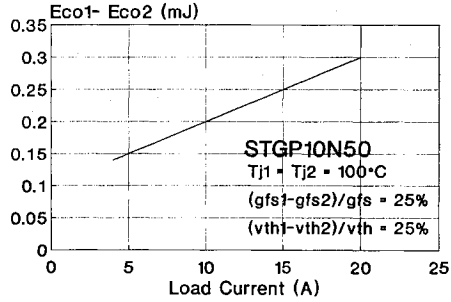

Fig. 28: Switching losses unbalance

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