SGS-THOMSON
MICROELECTRONICS

APPLICATION NOTE

STATIC AND DYNAMIC BEHAVIOUR OF PARALLELED IGBTs

by R. Letor

ABSTRACT

Problems associated with power device characteristics when power devices are connected in parallel, such as thermal stability and balanced switching behaviour can be solved by using insulated gate bipolar transistors (IGBT).
This note deals with parallel IGBT behaviour analyzing both static and dynamic characteristics.
The influence of heatsink mounting, lay-out, and drive circuit are described in order to demonstrate the best way to parallel IGBTs for optimum performance.
In addition the major advantages of the ISOTOP package are shown.

I. INTRODUCTION

When switching devices are paralleled, the following points must be carefully considered:
1) On-state losses balance.
2) Switching losses balance.
3) Thermal stability.
The loss unbalance, depending mainly on the spread of the device parameters (V_{CEsat}, switching time), can cause excessive power dissipation in one or more devices.

The thermal instability, correlated to the behaviour of the devices when the temperature increases, can cause thermal runaway and lead to the failure of the device.
This note explains the theory, describes practical examples and suggests possible solutions.
The behaviour of the IGBTs considered is not dependent on type, hence, the results can be extended to all SGS-Thomson IGBTs.

II. BEHAVIOUR OF PARALLELED IGBTS IN THE ON STATE.

The IGBT is a voltage driven device, hence when the devices are in parallel the drive conditions are the same for all devices (i.e. they all have the same V_{GE}).
Thus the influence of output characteristics and of the transfer characteristics can be studied separately.

A. Current balance in the on state.

Current balance can be studied with the simplified circuit of fig.1 where the following conditions are respected:

$$V_{CEsat1} = V_{CEsat2}$$
$$I_{C1} + I_{C2} = I_{LOAD}$$
$$V_{CEsat1} = f(I_{C1}, T_{j1}, V_{GE1})$$
$$V_{CEsat2} = f(I_{C1}, T_{j2}, V_{GE2}) \quad (1)$$

This system of equations (1) has a graphical solution which is shown in fig.2 for the extrapolation of current balance in two paralleled IGBTs with the same junction temperature ($T_{j1} = T_{j2}$).
Figure 3 shows the influence of the spread of V_{CEsat} on the current balance.

B. The influence of the temperature on current balance.

The fig.4 shows the basic equivalent structure of the IGBT.
The device functions as a bipolar transistor which is supplied base current by a Power-MOSFET.
The IGBTs output characteristic combines both the bipolar and the Power-MOSFET characteristics.

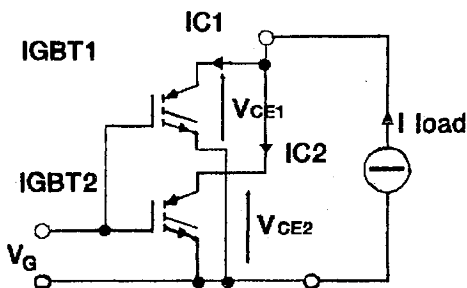


Fig. 1. Circuit where current balance depends only on IGBT characteristics.

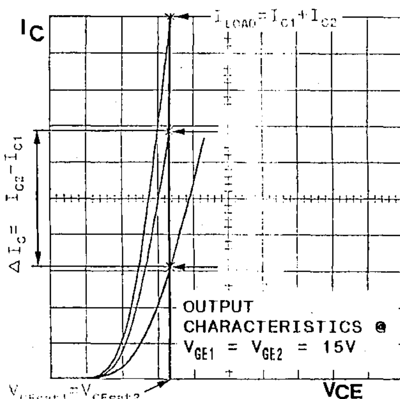


Fig. 2. Graphical extrapolation of current balance in the on state for two STGP10N50 @ I_{LOAD} = 10A; $T_{j1} = T_{j2}$ = 25°C; I_C = 1A/div.: V_{CE} = 0.5V/div.

The curves in fig.5 show these effects and highlight the following points:

1 - The temperature coefficient of V_{CEsat} is negative at low current density ($I < I_{NOM}$) (bipolar effect).

2 - The temperature coefficient of V_{CEsat} is positive at high current density ($I > I_{NOM}$) (Power-MOSFET effect).

3 - The temperature coefficient of the dynamic resistance (di/dv) is positive (Power-MOSFET effect).

The effect of this behaviour is that the influence of the temperature on current balance is small and that the current balance improves when the temperature increases, if $T_{j1} = T_{j2}$ ($\Delta T_j = 0$), (fig.6).

Figure 7 shows the effect on current balance when the junction temperature of paralleled devices are different ($\Delta T_j = 0$) and the medium temperature is constant $(T_{j1} + T_{j2})/2=K$:

- At low current, current balance is worst when the temperature difference increases, but the temperature coefficient is low.

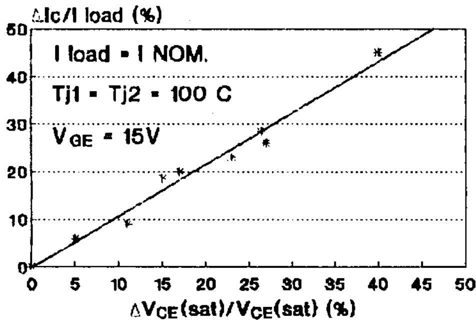


Fig. 3. Current balance versus the V_{CE}(sat) difference in two paralleled IGBTs.

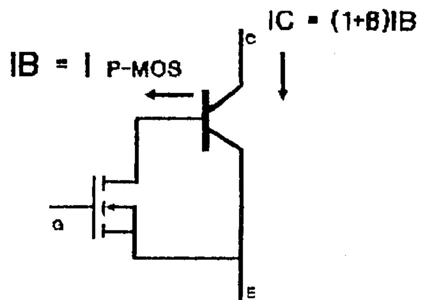


Fig. 4. Simplified equivalent circuit of an IGBT.

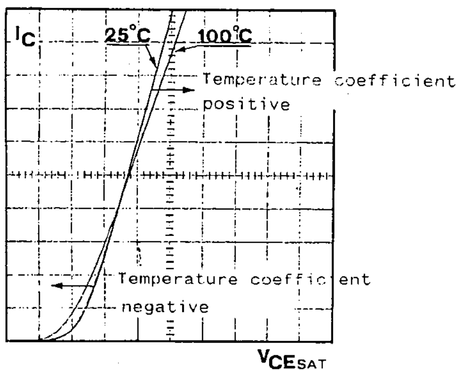


Fig. 5. Output characteristics versus the temperature for STGP10N50. I = 2A/div.; V = 0.5V/div.

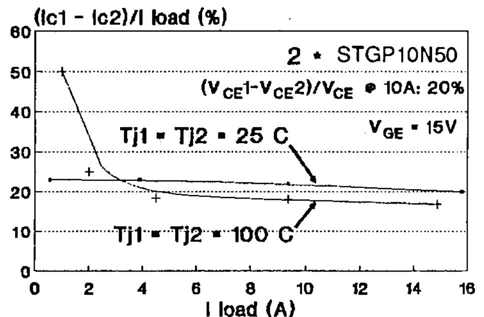


Fig. 6. Current balance versus I_{LOAD} and temperature in two paralleled IGBTs.

- At high current the behaviour is similar to the power- MOSFET behaviour; in fact, current balance improves when the temperature difference increases.

C.INFLUENCE OF THE TRANSFER CHARACTERISTICS.

When IGBTs are strongly saturated, the influence of the transfer characteristics on paralleled devices behaviour is small.

The figure 8 shows that the gate voltage scarcely influences the V_{CEsat} value; hence it is not possible to improve the current balance in the on-state by connecting an emitter-ground resistance.

III. PARAMETERS INFLUENCING SWITCHING BEHAVIOUR.

The IGBT's switching behaviour depends on:

- Device parameters (V_{th}, g_{fs}, C_i, C_{rss}, C_o).
- Drive circuit.
- Lay-out (Parasitic inductances).

The switching behaviour is studied in the circuit of figure 9 where the stray inductance "$L_{s1}+L_{s2}+L_{s3}$" is small and the IGBTs are turned on, while the free wheeling diode is still conducting; with this working condition di/dt is not limited by the stray inductances and depends on the IGBTs switching speed

$$dI/dt \gg Vcc/(L_{s1} + L_{s2} + L_{s3}).$$

A. Turn-on.

During turn-on, the switching losses depend mainly on the di/dt that influences the peak current due to the diode recovery ($Eco \approx Ipeak \cdot tcross \cdot Vcc/2$).

In the circuit of figure 9, the voltage drop caused by the inductance of the emitter-ground connection (L_{s1}), reduce the drive current ($I_G = (Vd - V_G - L_{s1} \cdot di/dt) / R_G$), and acts as a negative feedback during current rise time. Taking into account the effect of L_{s1}, the value of di/dt is:

$$di/dt \approx (Vd - V_{th}) / (R_G C_i / g_{fs} + Ls1)$$

For 1000V devices and with RG = 100Ω:

$$15 \cdot 10^{-9} < R_G C_i / g_{fs} < 25 \cdot 10^{-9}$$

The inductance of 1cm of wiring is:

$$L_{s1} \approx 10 \cdot 10^{-9}\ H/cm$$

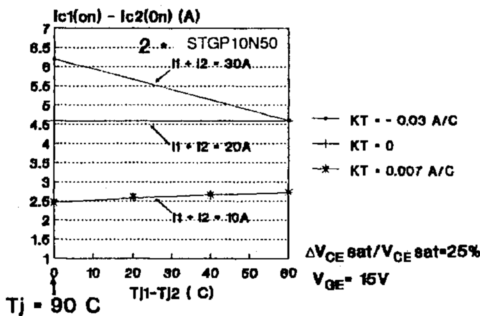


Fig. 7. Influence of ΔT_j on current balance during the ON-state. KT is a temperature coefficient.

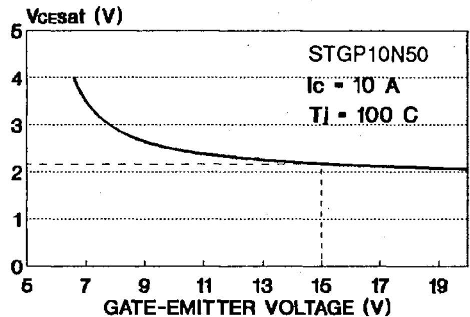


Fig. 8. Typical V_{CEsat} versus gate bias.

From this it can be seen that the spread of device parameters has less influence on the di/dt value than the parasitic inductance of the emitter-ground connection.

B. Fall.

During current fall two distinct phases can be seen (figure 10).
Phase 1 is similar to the current fall of power-MOSFET and the parameters influencing the di/dt are the same parameters that influence di/dt during turn-on.
The tail during phase 2 which is due to the minority carriers stored in the substrate mainly affects the switching losses.
The tail amplitude depends on Tj and on the turn-off current; hence, the turn-off current and the working temperature mainly influence the losses during the fall time (Fig. 11,12).

C. Storage.

During the storage time "$I_C = g_{fs} (V_{GE}-V_{th})$", "$di/dt \approx 0$", and the current waveform depends only on the IGBTs parameters (g_{fs}, V_{th}) and on the drive circuit.

IV. PARALLELED IGBT'S SWITCHING BEHAVIOUR.

The influence of the drive circuit, of the lay-out and of the device parameters was verified using the following conditions:

- 1 Gate drive with separate gate resistances (fig.13).
- 2 Gate drive with one gate resistance (fig.14).
- 3 Unbalanced emitter-ground wiring connection (fig.15).
- 4 Paralleling devices with the maximum spread of the parameters.

The voltage and collector current waveforms are stable in all conditions, even in the worst case condition where the gates are driven with a common resistance and the wiring inductances are strongly unbalanced

A. Turn-on.

Photo 1,2 show that the drive circuit influence on peak current balance is small and photo 3 shows that the peak current unbalance is significant in condition 3, where $\Delta L_{s1} = 0.15\mu H$.

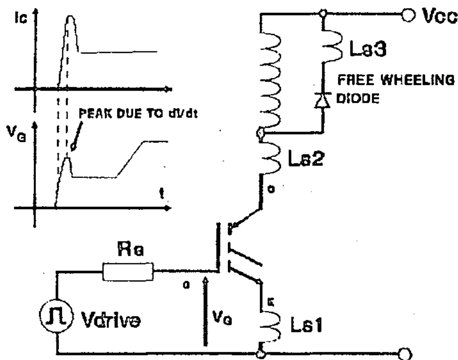


Fig. 9. Circuit showing the parasitic inductances influencing the switching behaviour.

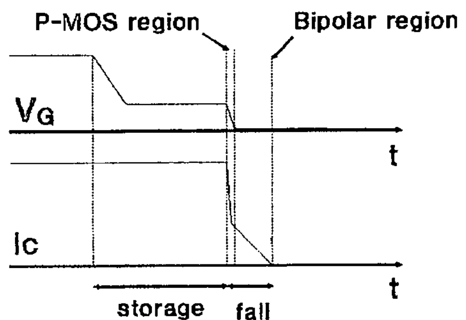


Fig. 10. Gate voltage and current waveforms during turn-off time.

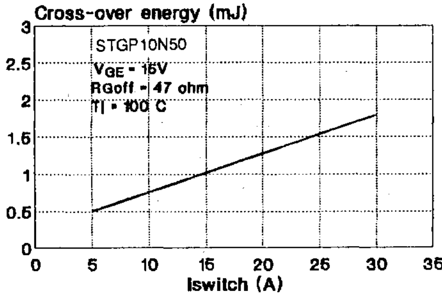


Fig. 11. Switching losses at turn-off V_s turn-off current.

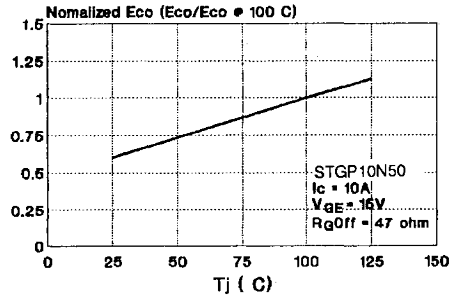


Fig. 12. Influence of temperature on turn-off losses.

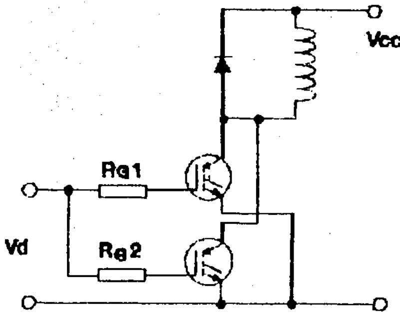


Fig. 13. Driving with separate gate resistance.

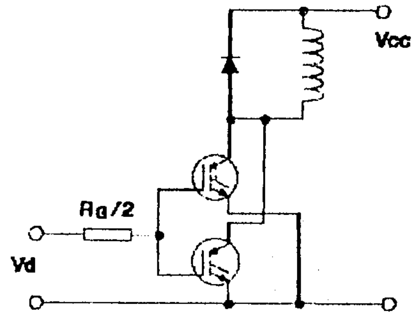


Fig. 14. Driving with one gate resistance.

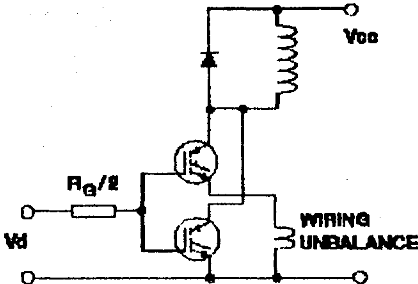


Fig. 15. Emitter ground wiring unbalance.

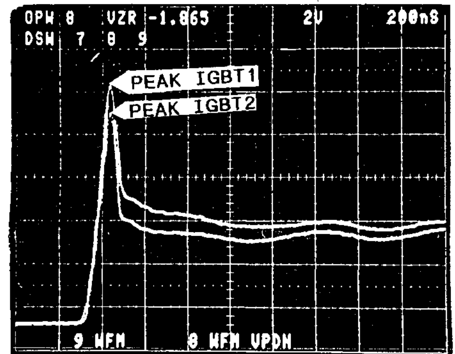


Photo 1. Turn-on with separate gate drive (fig. 13) of an STGH8N100; I = 2A/div., t = 200ns/div.

IGBTs with the maximum difference in parameter values were paralleled; the comparison of current waveforms in photo 1 and 2 demonstrates that the influence of parameter spread is low ($L_{s1} \approx 30$ nH).

B. Fall.

Photo 4 and 5 show that the wiring inductance unbalance affects only the power-MOSFET phase; but this behaviour creates negligible switching loss unbalance in comparison to the total turn- off switching losses.

The current unbalance just before current fall that affects the tail amplitude can create significant switching loss unbalance (see fig 17).

C. Storage.

During the storage time, the spread of the IGBTs parameters (g_{fs}, v_{th}) and the difference

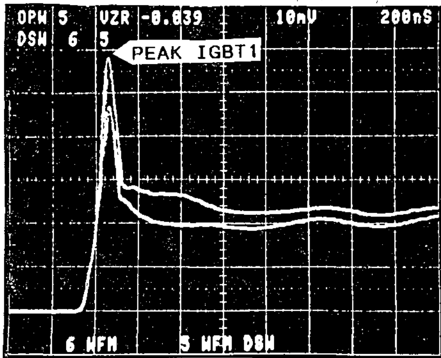


Photo 2. Turn-on with one gate resistance (fig. 14) of an STGH8N100; I = 2A/div., t = 200ns/div.

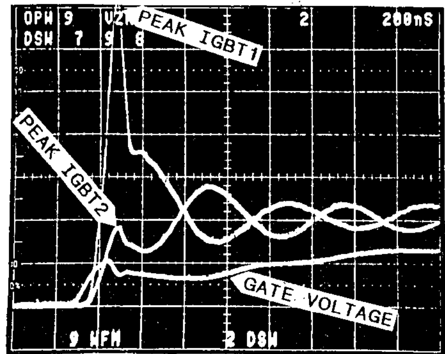


Photo 3. Turn-on with unbalanced emitter-ground wiring (fig. 15) of a STGH8N100; I = 2A/div., t = 200ns/div.

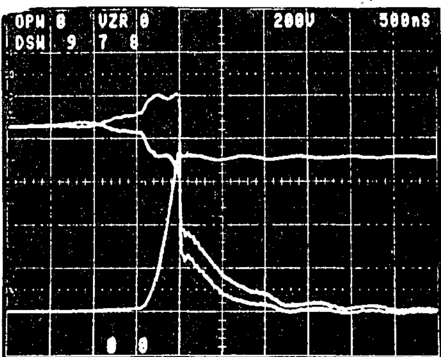


Photo 4. Turn-off with balanced gate-emitter wiring (fig. 14) of a STGH8N100; I = 2A/div., V = 200V/div., t = 500ns/div.

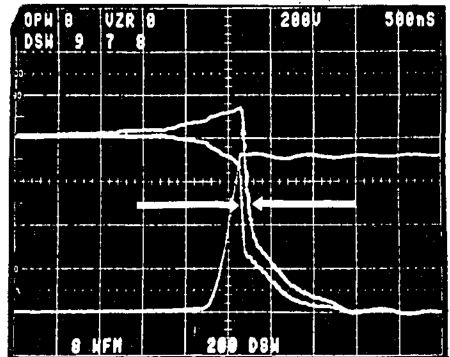


Photo 5. Turn-off with unbalanced emitter-ground wiring (fig. 15) of a STGH8N100; I = 2A/div., V = 200V/div., t = 500ns/div.

between storage times causes current unbalance thus creating switching loss unbalance.

Photo 6 shows the effect of the storage time differences when the gates are driven with separate gate resistances.

The collector current begins to fall in the device with the smaller storage time, consequently the current increases in the other IGBT so increasing storage current unbalance.

Driving the gates with only one gate resistance minimize this effect (photo 7); the device with the higher storage time hold the gate voltage to "$V_{th}+g_{fs}I_C$" until the fall time phase, so equalizing the storage times.

Current unbalance due to the IGBTs parameter spread can be calculated with the equations (2) and (3).

The curves of fig.16,17 show, respectively , storage current unbalance and the consequent switching loss unbalance between two devices where the V_{th} and g_{fs} values are the limits of the parameter spread.

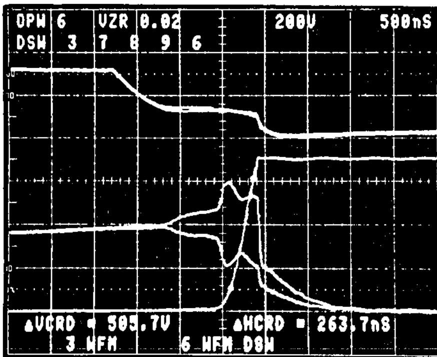


Photo 6. Effect of separate gate drive on storage current waveform. I_C=2A/div., V_{CE}=200V/div., V_{GE}=10V/div., t=500ns/div.

$$I_{load} = I_{1st} + I_{2st} = V_{GE}\,(g_{fs1} + g_{fs2}) - (g_{fs1}V_{th1} + g_{fs2}V_{th2}) \qquad (2)$$

$$I_{storage} = I_{1st} - I_{2st} = V_{GE}\,(g_{fs1} - g_{fs2}) - (g_{fs1}V_{th1} - g_{fs2}V_{th2}) \qquad (3)$$

V. THERMAL STABILITY.

When IGBTs are connected in parallel the on-state current is greater in the device with the smaller V_{CEsat} (fig.2); thus, the power dissipation and the junction temperature is higher in this device.

This phenomenon can cause a thermal instability because of the following reasons:

- Current unbalance increases when junction temperature difference increases (fig.7).
- Switching loss unbalance increases when junction temperature difference increases (fig.12).

The thermal stability can be achieved by mounting the paralleled IGBTs on the same heatsink; in this way the heatsink works as a negative feedback, because it transmits the heat from the device with the higher T_j to the device with the lower T_j so reducing the junction temperature difference.

In the ideal case where the thermal resistances ($R_{thj\,h}$,$R_{th\,x}$) are null, the thermal stability is assured because the devices work at the same temperature and the current balance improves when the temperature increases as shown in fig.6.

In real conditions the thermal resistances "R_{thjh}" are not negligible and the thermal stability can be studied with the equivalent thermal circuit of fig.18 which can be simulated with the system shown in fig.19.

The behaviour of the system near the final working point, is simulated using two paralleled IGBTs driving a constant inductive load; the devices are only active when the

heatsink temperature is uniform and at the final temperature which is independent of the current balance as the equations (4),(5),(6),(7),(8) show.

$$(T_{heatsink}=T_{amb.}+R_{th\ h\text{-}amb.}(V_{CE(sat)}(I_{C1}+I_{C2})+\text{Switching losses}) \approx const. \quad (4)$$

$$I_{C1}+I_{C2}=I_{LOAD}=const. \quad (5)$$

$$V_{CEsat} \approx const. \quad (6)$$

$$\text{Switching losses} \approx const. \quad (7)$$

$$T_{amb.} = const. \quad (8)$$

The stability was evaluated with the following conditions:

- heatsink temperature constant (load constant).
- Initial junction temperature equal to the heatsink temperature (100°C).
- Turn-off current unbalance constant and equal to the maximum value (worst case).
- Thermal capacitances disregarded.

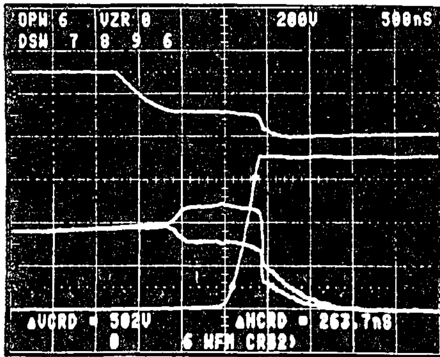


Photo 7. Turn-off with one gate drive resistance; I_C=2A/div., V_{CE}=200V/div., V_{GE} = 10V/div., t = 500ns/div.

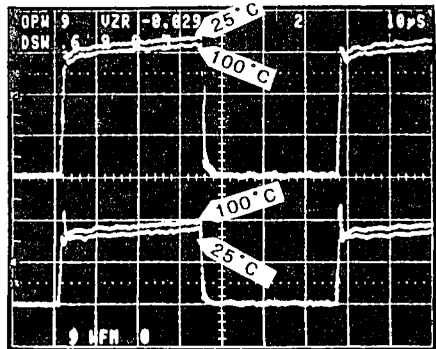


Photo 8. Comparison of current balance at T_j=25°C and 100°C; I_C=2A/div., t=10µs/div.

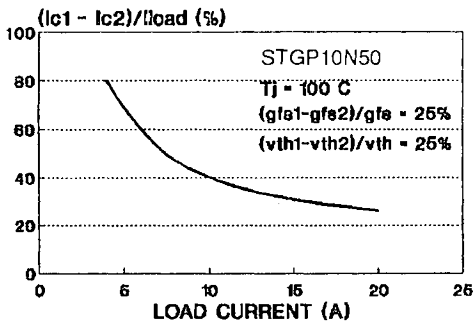


Fig. 16. Storage current unbalance versus load current.

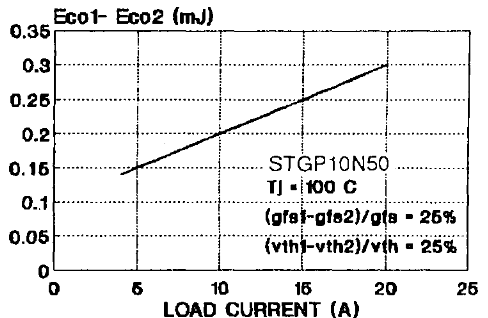


Fig. 17. Switching losses unbalance due to storage current unbalance.

The blocks in fig.19 signify the following computations:

1 - calculates initial current unbalance ($\Delta T_j = 0$) depending on the output characteristics of paralleled IGBTs.

2 - Calculates junction temperature difference depending on the on-state current unbalance (ΔI_{on}) and on switching current unbalance (ΔI_S).

$$\Delta T_j = R_{thjh} * (\Delta \text{ Power dissipation}).$$

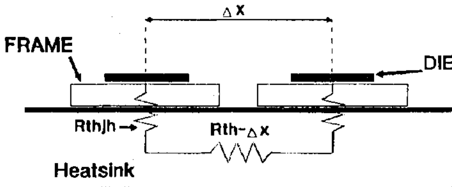


Fig. 18. Equivalent thermal circuit.

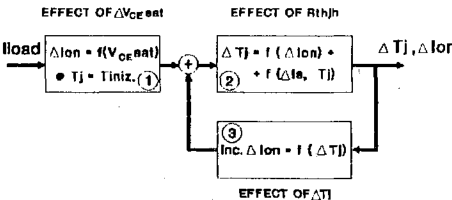


Fig. 19. Simulation of the temperature changes for two paralleled IGBTs.

3 - Calculates the growth of current unbalance (incr.ΔI) due to junction temperature difference (fig.16).

If $R_{th\ x}$ is negligible ($R_{th\ x} << R_{th\ jh}$):

$$f(\Delta I_{on}) = R_{th\ jh} * \Delta Pd_{on} =$$

$$R_{th\ jh} * V_{CEsat} * (t_{on}/T) * \Delta I_{on} = K_R * \Delta I_{on} \quad (9)$$

$$f(\Delta I_S, \Delta T_j) = R_{th\ jh} * Pd_{switching} =$$

$$R_{th\ jh} * f * \Delta E_{co}(\Delta I_S\ , \Delta T_j) \quad (10)$$

$$\Delta E_{co}(\Delta I_S, \Delta T_j) = \Delta E_{co}(\Delta I_S, 100°C) *$$

$$* (1+\Delta T_j * K_S) \text{ (see fig.12,17)} \quad (11)$$

$$\text{incr } \Delta I_{on} = K_T * \Delta T_j \text{ (see fig.7)} \quad (12)$$

The equation (13) is the transfer function of the system.

$$\Delta T_j = K_R * \Delta I_{on} + R_{th\ jh} * f * \Delta E_{co} /$$

$$(1-(K_R * K_T + K_S * R_{th\ jh} * \Delta E_{co} * f)) \quad (13)$$

Thermal stability is guaranteed if the equation (14) is true.

$$(K_R K_T + K_S R_{th\ jh} * \Delta E_{co} * f) < 1. \quad (14)$$

A. Example of two paralleled STGP10N50FI (Fully insulated package).

Conditions: $f = 15KHz$

$I_{LOAD} = 10A$

$\Delta V_{CEsat}/V_{CEsat} = 20\%$

$R_{th\ jh} = 3.5°C/W$

$t_{on}/T = 0.5$

Parameters	Reference
$\Delta E_{co} = 0.2$ mJ	See fig.17
$K_S = 0.005/°C$	See fig.12
$K_T = 0.007$ A/°C	See fig.7

$K_R = 3.5$ $K_R = 2\ R_{th\ jh} \cdot t_{on}/T$

$\Delta I_{on}\ (\Delta T_j{=}0) = 2A$ See fig.3

$V_{CEsat} = 2V$

Solution of the equations (13) and (14):

$$K_R K_T + K_S * R_{th\,jh} * \Delta E_{co} * f) = 0.08 << 1 \quad (15)$$

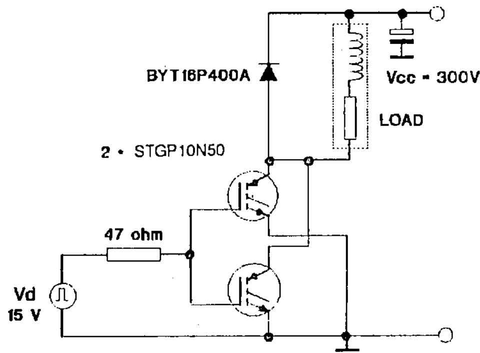


Fig. 20. Chopper circuit where paralleled IGBT behaviour was checked.

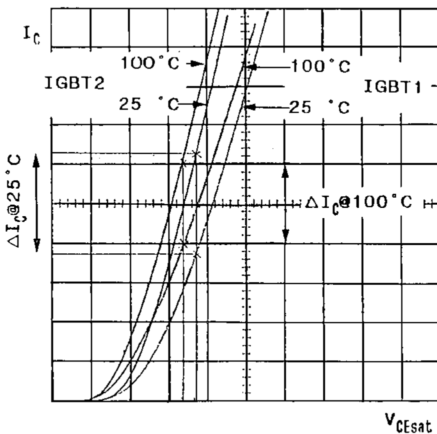


Fig.21. Output characteristics of the devices in fig. 20 and estimation of current balance at $T_{j1} = T_{j2} = 25°C$ and 100°C.

$$\Delta T_j = 19°C \quad (16)$$

$$\Delta Ion\ (\Delta T_j = 19°C) = 2.13\ A \quad (17)$$

The equations (15) (16) (17) show that the thermal stability is very high even when the devices are insulated and switching loss unbalance is high (worst case).

The conditions studied in this paper were carried out by mounting the paralleled devices in the chopper circuit shown in fig.20.

Photo 8 shows the current balance improvement when the heatsink temperature increases (25°C - 100°C) and the devices are working in the chopper circuit.

The fig.21 shows the output characteristics of the paralleled devices and the estimated on-state current.

VI. IGBTS IN THE ISOTOP PACKAGE.

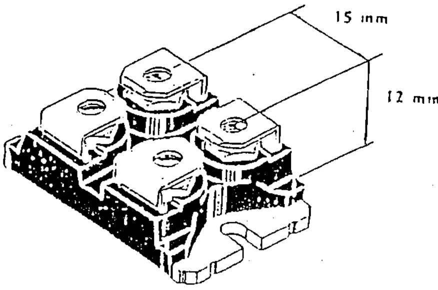
To reduce parameter spread, the IGBTs dice are mounted in the ISOTOP package with the "die sister" technique; the thermal resistance between the device junctions is reduced to a minimum and the gates are connected in parallel.

When the ISOTOP packages are paralleled, they give the following advantages:

- The small and compact size of the package (fig.22) and the low R_{thjc} value (0.5°C/W) give a minimal thermal resistance between the paralleled devices.

- This package was designed in order to minimize emitter ground wiring effects; In fact Isotop packages provide an auxiliary emitter pin which makes it simple to separate the driving circuit from the power circuit (fig.22,23).

Photo 9 & 10 show that unbalanced wiring connections have very little effect on the



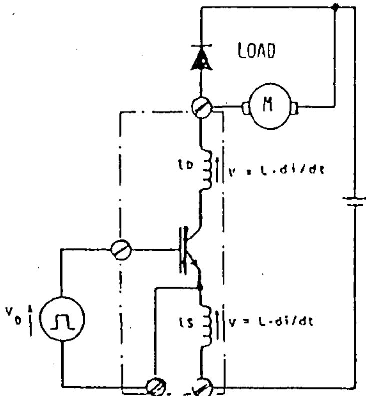


Fig. 22. Dimensions of the ISOTOP package and schematic diagram showing an auxiliary emitter pin.

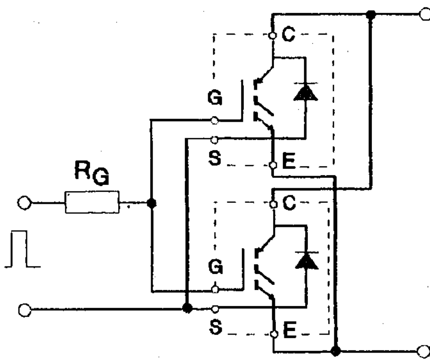


Fig. 23. Paralleling ISOTOP.

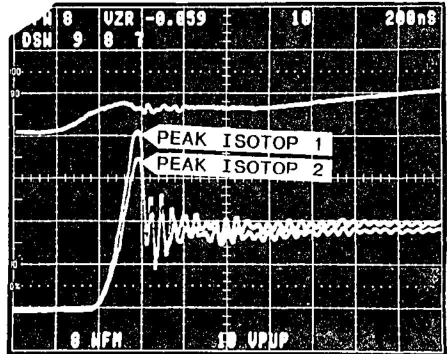


Photo 9. Turn-on of two TSG50N50DV with unbalanced emitter ground wiring. I_C=25A/div. V_{GE}=10V/div. t=200ns/div.

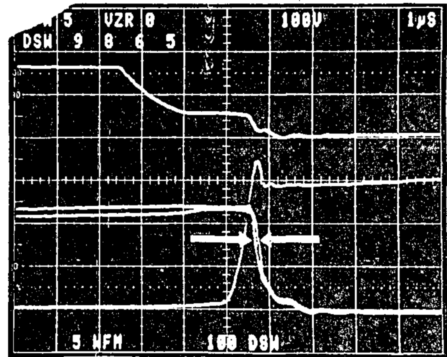


Photo 10. Turn-off of two paralleled TSG50N50DV. I_C = 25A/div. V_{CE} = 100V/div. V_{GE} = 10div. t = 1µs/div.

switching behaviour: the difference in length of emitter ground connections is 15 cm.

It can be seen in photo 10 that there is no peak voltage due to di/dt (V = L di/dt) on the gate-emitter auxiliary pin during current rise.

VII. CONCLUSIONS.

The performances in terms of current balance, thermal stability and switching behaviour when SGS-THOMSON IGBT devices are paralleled, are very satisfactory.
The transfer characteristics has no real influence on current balance in the on-state.
The on state current and the switching current balance are ensured respectively by the low spread of the V_{CEsat} values and by the low spread of device parameters.
High thermal stability is obtained by mounting the paralleled devices on the same heatsink even when the devices are insulated (mica, insulated package).
For an optimum switching behaviour of paralleled devices, it is necessary:

- to drive the gates with only one gate resistance.
- to balance the emitter-ground wiring.

When IGBTs are in the ISOTOP package, the wiring unbalance tolerance is high and the thermal resistance (R_{thjh}) is low; thus,the advantages of the ISOTOP package are:

- easy to design the lay-out when paralleling IGBTs in ISOTOP.
- small thermal resistance between the junctions of paralleled devices; thus, temperature difference between the junction of the devices in parallel is reduced to a minimal value.

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