
**SERIES CONNECTION OF MOSFET,
BIPOLAR AND IGBT DEVICES**

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ABSTRACT.

Fast power switches with voltage ratings much higher than those of single fast switching devices can be made by connecting Bipolar Transistors, Power MOSFET and IGBTs in series.

Problems associated with device characteristics such as balanced switching, steady state and thermal behaviour must be carefully considered when designing with such switches.

This note deals with the series connection behaviour analyzing both static and dynamic characteristics of the devices.

Two philosophies for driving circuits are

described and design criteria are given for obtaining optimum performance.

1.0 INTRODUCTION.

Advantages of BIPOLAR TRANSISTORS, Power MOSFETs and IGBTs reside in the simplicity of the driving circuit and on their high switching speed. But, applications of these devices are limited to maximum reverse voltage, generally up to 1000V - 1500V. Higher voltage ratings would make these devices unattractive due to problems related to their structure.

For example, theoretical $R_{DS(on)}$ of a Power MOSFET increases with the square of the voltage breakdown ($R_{DS(on)} = 5.93 \text{ E-9} \cdot (V_{DSMAX})^{2.5}$). Figure 1 showing the real behaviour of SGS-THOMSON Power MOSFETs versus breakdown voltage, demonstrates that the current rating of three 800V Power MOSFETs in series will be higher than a single 2000V Power MOSFET.

Moreover, the design of IGBTs and BIPOLAR transistors with higher voltage ratings can be difficult due to the rise time of the switching waveform shown in figure 2.

Therefore, in some applications like battery chargers, inverters for medium voltage lines such as railway traction using frequencies up to 20kHz or high resolution TV deflection with operating frequencies of up to 64kHz, the series connection of fast switching power devices can be an interesting solution.

When connecting switching devices in series, voltage sharing during the off-state, and during transient must be carefully considered.

In fact the spread of leakage current creates unequal reverse voltage sharing. Delay between commutation due to switching time

differences causes transient overvoltage. If the parameters are temperature dependent, junction temperature difference must also be considered.

2.0 STEADY STATE VOLTAGE SHARING.

2.1 HOW TO BALANCE STEADY STATE VOLTAGE SHARING.

Figure 4 illustrates how the difference in blocking voltage characteristics results in unequal state voltage and how a resistor connected in parallel to each device (figure 3) equalizes the voltage sharing.

Equations 1 and 2 can be derived from the graphical information in figure 4 and to evaluate the value of R that reduces the difference of blocking voltage to a fixed value ΔV_R with a fixed V_M .

$$\Delta V_{R12} = V_{R1} - V_{R2} = R_1 \cdot \Delta I_{R12} \quad (1)$$

$$V_M = V_{R1} + V_{R2} + \dots + V_{Rn} \quad (2)$$

Equation (1) assumes that the leakage current is constant, this approximation is errs on the side of caution and introduces a safety margin.

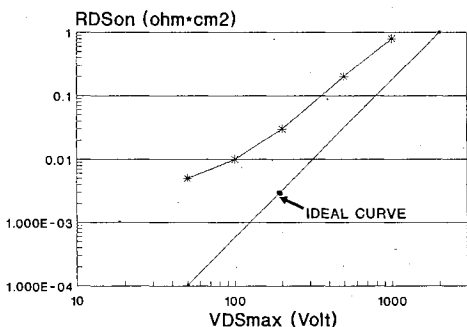


Fig. 1. Ideal and real behaviour of $R_{DS(on)}$ vs breakdown voltage.

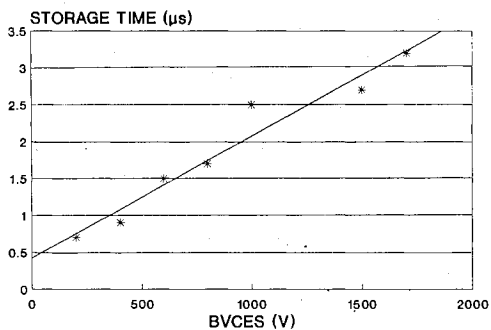


Fig. 2. Storage time behaviour versus rated BV_{CES} for bipolar transistors.

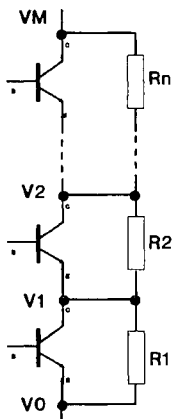


Fig. 3. Connection of sharing capacitors.

If we suppose that device 1 has the lower I_{RM} , V_{R1} will be the maximum reverse voltage ($V_{R1} = V_{RM}$) and developing the equation (2):

$$V_M = V_{RM} + V_{RM} - \Delta V_{R12} + \dots$$

$$\dots + V_{RM} - \Delta V_{R1n} = n \cdot V_{RM} - \sum_2^n \Delta V_{R1n} \quad (3)$$

The worst case condition, when n devices are connected in series, occurs when $(n-1)$ devices have maximum leakage current and one device has the lowest possible leakage current: $\Delta I_{R1n} = \Delta I_{Rmax}$.

In this case, setting $R_1 = R_2 = \dots = R_n$, the solution of the equations 1 and 2 gives:

$$R = (n \cdot V_{RRM} - V_M) / (n-1) \cdot \Delta I_{Rmax} \quad (4)$$

2.2 EVALUATION OF ΔI_{Rmax} .

ΔI_{Rmax} is the sum of $\Delta I_{RD} + \Delta I_{RT}$, where:

- ΔI_{RD} is the maximum leakage current dispersion at a fixed V_R and T_j .
- ΔI_{RT} is due to the difference between the junction temperatures of each device (ΔT_j).

For devices today available $\Delta I_{RD} \approx 0.6IRM$ @ $V_R = V_{RRM}$ and $T_j = 100^\circ C$.

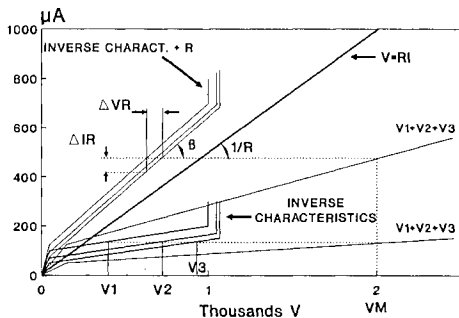


Fig. 4. Graphical calculation of sharing resistors when V_M and ΔV_R are fixed.

The difference in junction temperature depends on both differences of power dissipation and on the thermal resistance between devices.

$$\Delta T_j = \Delta (R_{th} \cdot P_{DISSIPATION})$$

Experience shows that $\Delta T_j = 10^\circ C$ is the maximum value for insulated devices mounted on the same heatsink.

Using the derating shown in figure 5, for $\Delta T_j = 10^\circ C$:

$$\Delta I_{RT} = 0.2 IRM.$$

Taking a safety margin we can use:

$$\Delta I_{R} = 0.85 IRM.$$

2.3 EXAMPLE 1: series connection of three STHV82 Power MOSFETs:

Ratings:

$$V_{DSS} = 800V$$

$$I_{DSS} \text{ max} = 1000\mu A @ T_j=125^\circ C$$

$$R_{DS(on)} \text{ max} = 2\Omega @ T_j=25^\circ C$$

$$R_{thj-case} = 1^\circ C/W$$

Conditions:

Maximum blocking voltage: $V_M = 2000V$

Maximum Current and duty cycle:

$I_M = 3A, t_{on}/T = 0.5$

Case temperature:

$T_{CASE} = 80^{\circ}C$

Switching frequency : 50KHz.

Calculation of sharing resistor values.

T_j can be estimated using:

$$R_{DS(on)} @ T_j = 100^{\circ}C \approx R_{DS(on)}(25^{\circ}C) \cdot 1.7$$

$$T_j \approx T_{case} + R_{thj-case} \cdot$$

$$R_{DS(on)} \cdot I_D^2 \cdot t_{on}/T \approx 100^{\circ}C.$$

For $T_j = 100^{\circ}C$ using the derating of figure 5:

$$I_{RM} = (1 - 0.6)mA = 0.4mA$$

For safety operation and reliability

$$V_{RM} = 0.9 V_{DSS} = 720V.$$

Using equation (4):

$$R = (3 \cdot 720 - 2000)/(2 \cdot 0.4 E-3) = 200 \text{ k}\Omega.$$

Maximum power dissipation of each resistor when $t_{on}=0$: $V^2/R = 2.6 \text{ W}.$

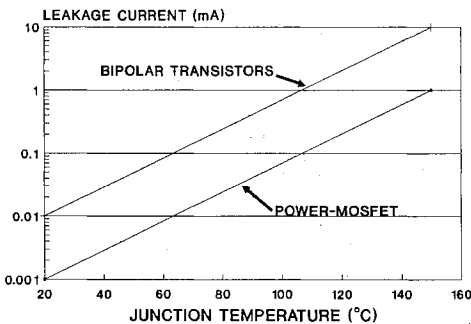


Fig. 5. Leakage current versus junction temperature.

2.4 IS IT POSSIBLE TO ELIMINATE THE SHARING RESISTORS?

For high frequency operation, it is necessary to consider the impedance of the output capacitance of the device which is in parallel with the sharing resistors.

In the previous example the impedance of the STHV82 output capacitance (150pF) is much lower than the calculated value of the sharing resistors:

$$Z_{Coss} = 1/2\pi f C_{oss} \approx 21 \text{ K}\Omega \ll 200\text{K}\Omega$$

Therefore, if only high switching frequency conditions are expected, then the sharing resistors can be omitted.

3.0 DRIVING CIRCUIT FOR FAST SWITCHING DEVICES IN SERIES.

Two philosophies for driving switching power devices in series and for optimizing transient voltage sharing can be developed:

- 1) Driving each device in series with synchronized pulses and masking the difference of switching time.
- 2) Equalizing switching times with an optimized driving circuit.

Synchronized driving pulses can be generated by a transformer and delay turn-off time difference can be masked by snubber capacitors.

When continuous mode and wide range of duty cycle are required, it is difficult to design a method for driving the transformer. In this case auxiliary supplies and optocouplers can be used.

Equalization of switching times and continuous mode can be achieved using capacitive coupling between output circuit and driving circuit and diode network can be used for continuous bias.

3.1 DRIVING CIRCUIT GENERATING SYNCHRONIZED PULSES AND TRANSFORMER COUPLING.

It is possible to achieve excellent synchronization of the driving pulses together with good control of the driving voltage and current.

Figure 6 shows a driving circuit for both voltage and current controlled devices.

The coupling inductances between the primary winding and every secondary must be as balanced as possible in order to equalize all the transfer impedances.

In both circuits the device driving current is limited on the primary side of the transformer; this feature reduces the difference in delay turn-off time of devices in series.

In fact during delay turn-off time or storage:

$$(I_{D1} + I_{D2}) = I_D \cdot n_2/n_1$$

Input impedances of devices ≈ 0

$$(-I_{B1} \approx -I_{B2} = I_D/2).$$

At the end of storage for bipolar transistors or at the end of Miller effect for voltage controlled devices (Power MOSFET, IGBT) the input

impedance becomes very high and the driving current fall, when the faster device turns-off, the device with the higher turn-off delay time increases its switching speed because it is driven by all the available current ($-I_{B(G)} = I_D \cdot n_2/n_1$).

3.2 EQUALIZATION OF TURN-OFF DELAY TIMES USING CAPACITANCES.

In the circuit of figure 7, the capacitors transmit driving voltage to the high side devices and the diodes supply continuous gate voltage during the on state. The circuit works as follows.

During transition: We suppose that initially all Power MOSFETs are in the off state and capacitor voltages are balanced. When the positive edge is applied to drive circuit, P₁ turns-on and pulls down the source of P₂. The capacitor network charges the gate of P₂. P₂ starts turn-on phase and pulls down source of P₃ etc...

The turn-off phase is similar to the turn-on phase. When P₁ turns-off, the source of P₂ is pulled up. A negative voltage discharges the gate of P₂ into the capacitor network turning

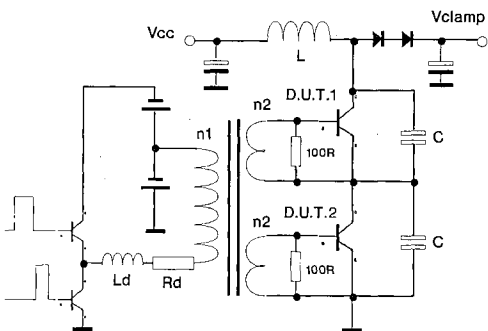


Fig. 6. Synchronized Drive of fast switching power devices in series using a transformer.

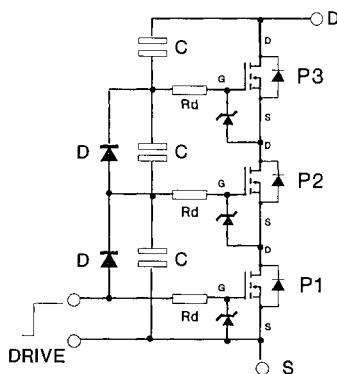


Fig. 7. Capacitors and diode network driving Power MOSFETs connected in series.

P₂ off, etc.

For a better voltage balance during switching, the capacitor must be charged to the same voltage ($V_{C1}=V_{C2}=...=V_{C3}$); imbalance is due to Power MOSFET gate charge and discharge of the capacitors network. For this

$$\Delta V_{\max} = (n-1) \cdot Q_{\text{GATE CHARGE}} / n \cdot C$$

During on state:

$$V_{\text{GATE}(n)} = V_{\text{DRIVE}} - (n-1) \cdot (V_{\text{DS(on)}} + V_{\text{F diode}})$$

Therefore, for full saturation of every device connected in series a driving voltage greater than 15V is necessary.

Possible configurations. This circuit configuration can be used for series connection of IGBTs and BIPOLAR TRANSISTORS.

When connecting IGBTs, sharing capacitors are necessary because the turn-off current tail of IGBTs does not depend on the driving circuit.

ADVANTAGES: Using POWER MOSFETs this circuit allows optimum dynamic voltage balance with low values of capacitors so minimizing energy dissipation.

DISADVANTAGES: The circuit is critical when driving bipolar transistors due to high drive energy.

It is difficult to optimize switching waveforms. You can see in Photo 1 that current fall waveforms are not correct.

The driving voltage necessary for full saturation can be greater than the rated gate voltage.

For better on-state and switching performances, a regulator for each POWER MOSFET gate must be introduced (Figure 8) and optimization of the driving circuit will be necessary.

EXAMPLE 2.

Photo 2 shows POWER MOSFET drain voltage balance and drain current behaviour in the circuit of figure 7, where STHV102 devices are connected in series and in parallel.

$$C = 1500\text{pF.}$$

$$Q_{\text{GATE CHARGE}} \text{ of } 2 \cdot \text{STHV102 @ } (V_G = 15V) = 2 \cdot 85\text{nc} = 170\text{nc}$$

$$\Delta V = 170 \text{ E-9} / 2 \cdot 1500 \text{ E-12} = 56.5V$$

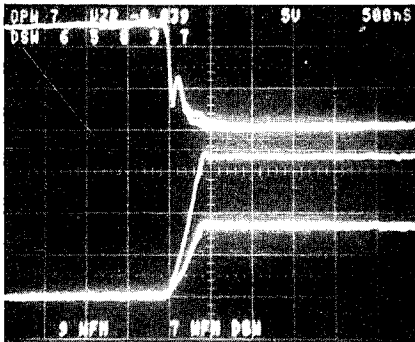


Photo 1. Voltage sharing and drain current of two Power MOSFETs in series as described in the example 1.
I = 2A/div, V = 500V/div.

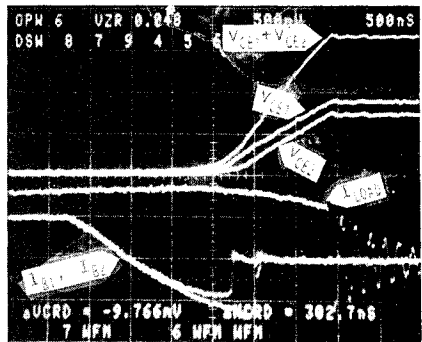


Photo 2. Load current and voltage sharing behaviour of two BUV46 in series as shown in figure 5. C_S = 4.7nF, I_B = 0.5A/div, I_{LOAD} = 2A/div, V = 500V/div.

4.0 TRANSIENT VOLTAGE SHARING WITH SYNCHRONIZED DRIVING CIRCUIT.

The transition overvoltages due to the difference between turn-off times can be controlled using sharing capacitors as shown in figure 9.

During switching operation, discharge of the sharing capacitors generates power losses so reducing efficiency of the converter.

In this note we define the losses of efficiency due to the capacitors discharge as follows:
Balancing losses/handled power = $n \cdot 0.5 \cdot C \cdot V^2 \cdot f / (V_M \cdot I_C \cdot \text{duty cycle})$.

4.1 HOW TO CALCULATE SHARING CAPACITORS.

Worst case condition occurs at turn-off with a inductive load. When the faster device in series turns-off, all the current load charges the capacitance in parallel to the slower device output, and generates a fast voltage rise. Using suitable capacitances it is possible to retard the voltage rise and to fix ΔV_R as shown in figure 9.

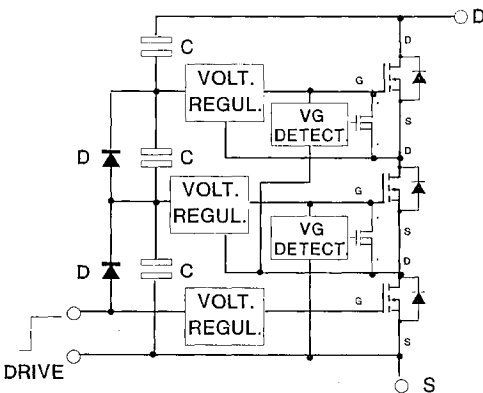


Fig. 8. Driving circuit of figure 7 for optimized driving voltage and switch-off.

$$C = \Delta Q / \Delta V_R = \int_{t_2}^{t_1} (I_1(t) - I_2(t)) dt / \Delta V_R \quad (5)$$

For n devices connected in series and setting $C_1 = C_2 = \dots = C_n$, Δt and ΔI are fixed to the maximum value.

4.2 SERIES OF BIPOLAR TRANSISTORS.

At turn-off the difference in storage time must be considered. In fact, denaturation at the end of the storage will cause collector voltage rise. For bipolar transistors the spread of this parameter, about 50%, is much higher than the fall time. For this $\Delta Q \approx I_{OFF} \cdot \Delta t_{storage}$ and the equation (5) becomes:

$$C_{MIN} = I_{OFF} \cdot \Delta t_{storage} / \Delta V_{R \max} \quad (6)$$

EXAMPLE 3:

Series connection of two BUV46AFI.

Ratings:

$V_{CES} = 1000V$

$1.5\mu s < t_{storage} < 2.5 \mu s @ I_C = 2.5A;$

$I_{B1} = -I_{B2} = 0.5A, T_c = 25^\circ C.$

$I_C \text{ nom.} = 5A$

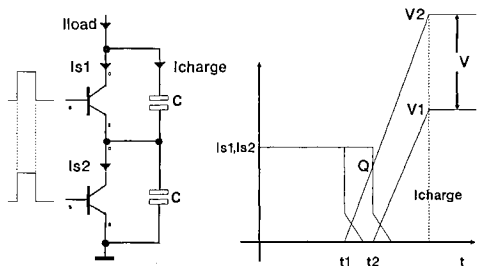


Fig. 9. Evaluation of sharing capacitors reducing the effect of delay turn-off time spread.

Conditions:

Maximum turn-off clamping voltage:

$$V_M = 1600V.$$

$$I_{OFF} \text{ max.} = 3A.$$

Switching frequency:

$$15 \text{ KHz, duty cycle} = 0.5$$

$$I_{B1} = -I_{B2} = 0.5A$$

Solution:

For safety margin:

$$V_{CEmax} = 0.9 \cdot V_{CES} = 900V$$

$$\Delta V_{R \text{ max}} = 2 \cdot V_{CEmax} - V_M = 200V$$

Using equation (6):

$$C_{2MIN} = (3 \cdot 1E-6)/200 = 15nF.$$

The power dissipation due to discharge of sharing capacitors is:

$$\text{Balancing losses} = P_D = C \cdot V^2 \cdot F = 144 \text{ W.}$$

(Balancing losses/handled power %) =

$$P_D / I \cdot V_{max} \cdot 0.5 \cdot \% = 6 \%$$

For better efficiency this energy must be reduced. For this, it is necessary to limit the maximum spread by a selection of devices.

If $\Delta t_{storage} = 300ns$, then a 4.7 nF sharing capacitor can be used as shown in photo 2.

4.3 SERIES OF POWER MOSFETs.

The current fall in POWER MOSFETs is very fast; equation (5) becomes:

$$\Delta V_R = I_{OFF} \cdot \Delta t_{OFF} / C$$

t_{OFFmax} can be calculated using gate charge, as shown in figure 7:

$$- t_{OFF} = (Q_1 + Q_2)/I_{GATE}$$

If I_{GATE} is balanced for all devices in series, then $\Delta t_{OFF} \text{ max}$ can be calculated using the distribution of figure 11; moreover, due to

temperature independance of gate charge, temperature difference between junction devices can be disregarded:

$$- \Delta t_{OFF} = 5/100 \cdot (\text{typical value of } t_{OFF})$$

If each POWER MOSFET has its own driving resistor, then tolerance of resistors must be considered and delay turn-off time can be calculated as follows:

$$- t_{OFF} = t_a + t_b = R_G C_{GS} \ln 3 + Q_2 R_G / (V_{Drive} - G_m I_D)$$

EXAMPLE 4: Series of two STHV102.

Ratings:

$$V_{DS} = 1000V$$

$$\text{Gate charge: } Q_1 + Q_2 = 62 \text{ nc} \pm 5\%$$

Conditions:

$$I_G = 100 \text{ mA.}$$

Maximum clamping voltage:

$$V_M = 1600V$$

$$I_{OFF} = 3A$$

$$F = 15 \text{ KHz, duty cycle} = 0.5$$

Solution:

For safety margin:

$$V_{DSmax} = 0.9 \cdot V_{DS} = 900V$$

$$\Delta V_{R \text{ max}} = 2 \cdot V_{DSmax} - V_{max} = 200V$$

$$\Delta t_{OFF} = \Delta (Q_1 + Q_2)/I_G =$$

$$6.2 \text{ E} - 9/ 100 \text{ E} - 3 = 62ns.$$

$$C_{MIN} = (3 \cdot 62 \text{ E} - 9) / 200 = 930pF.(1000pF)$$

$$P_{D@F=15 \text{ KHz}} = C V^2 \cdot f = 9.6 \text{ W}$$

(Balancing Losses/handled power) = 0.4 %
Photo 3 shows devices behaviour with the conditions of the example and $C = 1500pF$.

4.4 SERIES OF IGBTs.

Photo 4 shows the behaviour of two 1000 V IGBTs in series at turn-off using an inductive load with sharing capacitors (1500pF). Due to the high fall time value (figure 9), the total voltage ($V_{CE1} + V_{CE2}$) can reach the clamping voltage before the end of current fall.

Therefore, the equation (6) can not be simplified and ΔV_R must be split as follows:

$$\Delta V_R = \Delta V_{R1} + \Delta V_{R2}$$

where:

$\Delta V_{R1} = V_1 - V_2$ @ $t = t_a$ (photo 4) is due both, to the delay turn-off time difference, and to the difference of current tail during voltage rise.

ΔV_{R2} is due to the difference of sharing capacitor charge when $V_1 + V_2 = V_{CLAMP}$ = constant due to the difference of current tail and Δt_{FALL} : $\Delta V_2 = \Delta Q_2 / 2C$

The minimum value of sharing capacitor can not be calculated easily due to the influence of dV/dt on the current tail behaviour.

For easy evaluation, the charge time of the sharing capacitor ($t_a - t_b$) must be equal to the maximum t_{FALL} . In this case:

$$C = 2 \cdot (I_{OFF} - I_{TAIL}/2) \cdot t_{FALLmax}$$

$$\Delta V_R = \Delta V_{R1} = (\Delta t_{OFF} \cdot (I_{OFF} - I_{TAIL}/2)) / C + \Delta I_{TAIL} \cdot t_{FALLmax} / 2C$$

Δt_{OFF} depending on gate charge spread is temperature independent.

I_{TAIL} , ΔI_{TAIL} , t_{FALL} are temperature dependent as shown in figure 13.

EXAMPLE 5:

Series of two IGBTs STGH8N100.

Ratings:

$$V_{CESmax} = 1000 \text{ V}$$

$$I_{Cmax} = 8 \text{ A @ } T_c = 125^\circ \text{C}$$

$$t_{FALL} = 800 \text{ ns } \pm 20\% \text{ @ } T_c = 125^\circ \text{C}$$

(see figure 9)

$$\text{Gate charge} \approx 60 \text{ nc } \pm 5\%$$

(similar to STHV102)

Conditions:

$$V_{CLAMP} = 1600 \text{ V}$$

$$\Delta V_{Rmax} = 200 \text{ V}$$

$$I_{Cmax} = 8 \text{ A}$$

$$T_{Jmax} = 125^\circ \text{C}$$

$$I_{GATE} = 100 \text{ mA}$$

$$f = 15 \text{ KHz, duty cycle} = 0.5$$

Solution:

$$C = 2 \cdot (I_{OFF} - I_{TAIL}/2) \cdot t_{FALLmax}$$

$$t_{FALLmax} / V_{CLAMP} = 7.8 \text{ nF}$$

$$\Delta t_{OFF} = \Delta (Q_1 + Q_2) / I_G =$$

$$6.2 \text{ E} - 9 / 100 \text{ E} - 3 = 62 \text{ ns.}$$

$$\Delta V_R = \Delta V_{R1} = (\Delta t_{OFF} \cdot (I_{OFF} - I_{TAIL}/2)) / C +$$

$$\Delta I_{TAIL} \cdot t_{FALLmax} / 2C = 113 \text{ V}$$

Resulting $\Delta V_R \ll 200 \text{ V}$, a 6.8 nF capacitor can be used and $\Delta V_R = 130 \text{ V}$.

Balancing losses =

$$P_D (15 \text{ KHz}) = C \cdot V^2 \cdot f = 65 \text{ W}$$

(Balancing Losses/handled power) =

$$P_D / V_{max} \cdot I \cdot 0.5 = 1 \%$$

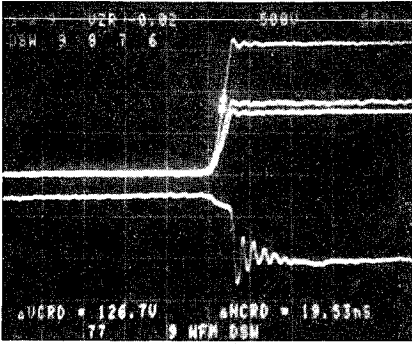


Photo 3. Load current and voltage sharing of two Power MOSFET STHV102 in series as shown in figure 5. $C_S = 1.5\text{nf}$, $\Delta t_{\text{off}} = 60\text{ns}$, $I = 2\text{A/div}$, $V = 500\text{V/div}$.

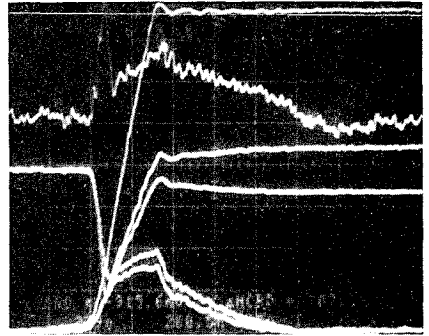


Photo 4. Turn-off behaviour of two IGBTs STGH8N100 in series with synchronized driving pulses. $C = 1.5\text{nF}$, $T_j = 100^\circ\text{C}$, $I = 2\text{a/div}$, $I_{\text{CHARGE}} = 0.5\text{A/div}$, $V = 200\text{V/div}$.

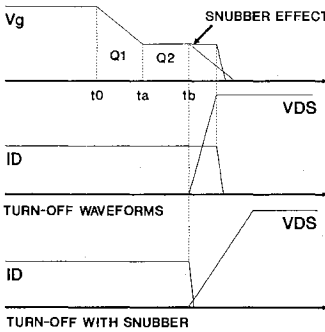


Fig. 10. Turn-off behaviour of Power MOSFET when connecting snubber capacitors.

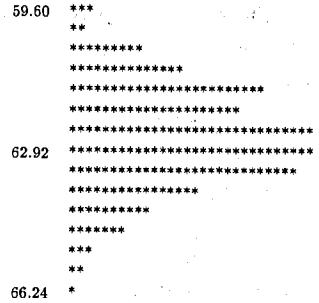


Fig. 11. Spread of the Power MOSFET gate charge.

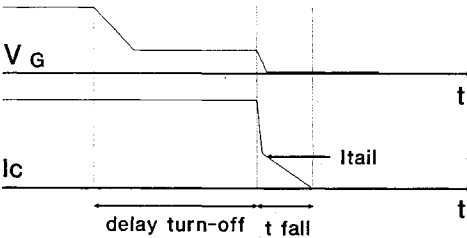
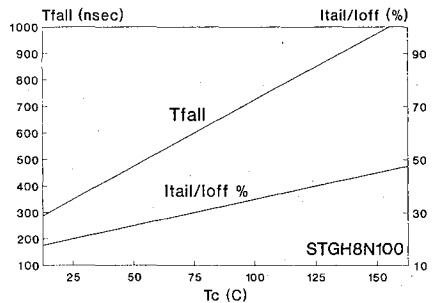


Fig. 12. Current fall behaviour of IGBT devices.



$V_{ce} = 800\text{V}$, $I_c = 8\text{A}$, $V_g = 15\text{V}$, $R_g = 100\text{ohm}$

Fig. 13. t_{FALL} and current tail of IGBTs vs junction temperature.

5.0 CONCLUSIONS.

Every switching power device can be connected in series successfully in order to make a power switch for fast switching applications working at a voltage greater than 1500 V.

For optimum voltage sharing during steady state and switching, it is necessary:

- to make a compromise with the additional power losses introduced by sharing capacitors and by sharing resistors.
- that the junction temperature difference between devices in series must be as low as possible; especially for bipolar transistors and IGBTs.

Bipolar transistors require a selection by storage time.

Power MOSFETs are temperature independent and have very low parameter

spread, making them easy to connect in series.

IGBTs need considerable sharing capacitors, but these devices are attractive thanks to their very low saturation voltage and low driving energy.

The driving circuit can be made either by using a transformer for synchronized driving pulses, or with a diode and capacitor network.

When using a transformer, driving voltage or current can be controlled easily, but, continuous mode and a wide range of duty cycle can be a problem .

The diode and capacitor network allows equalisation of devices turn-off time, so reducing sharing capacitors value when gate voltage controlled devices are used. This method requires hard optimization of the circuit for very fast switching applications.