SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SAFE BEHAVIOUR OF IGBTs SUBJECTED TO dV/dt

by R. Letor, M. Melito

ABSTRACT

When an IGBT in the off state is subjected to a high dV/dt, parasitic turn-on can occur leading to additional losses.

This paper describes the phenomenon and indicates the main parameters influencing this behaviour.

Several methods of suppressing this parasitic phenomenon are described.

Using a suitable design of gate drive, it is possible to increase the circuit reliability in all conditions.

Practical examples and measurements are given.

INTRODUCTION

The behaviour of IGBTs subjected to a dV/dt differs according to the working conditions. We can consider two distinct cases:

- **static dV/dt**

  The static condition occurs when the dV/dt applied to an IGBT in the off state, acting through the reverse capacitance $C_g \approx C_{res}$, causes the gate voltage to rise turning the device on. This behaviour is typical of a circuit in bridge configuration, where the dV/dt is generated during complementary switch turn-on. This undesired effect generates

additional losses, mostly in devices in the off-state, due to the presence of both high voltage and high current on the collector. Parasitic turn-on must be avoided and this can be prevented by modifying the design of the drive circuit.

dynamic dV/dt

In this condition the dV/dt is applied to an IGBT during the recombination of minority carriers in the substrate and a peak current appears during the collector voltage rise time even if the gate and the emitter are in short circuit. The dynamic condition can occur when the IGBT works in thyristor mode, typically in a quasi resonant converter with a zero curent switch (QRC-ZCS). In this case the power losses depend on the device structure and on the converter resonant frequency. Thus, this phenomenon sets a limit to the operating frequency.

1. SPURIOUS TURN-ON IN STATIC dV/dT CONDITION.

1.1 Description of the Phenomenon.

The equivalent diagram of fig.1 shows current flow across the structure of an IGBT in the off-state when a rising collector-emitter voltage is applied.

The current through the reverse capacitance C_{gc} ($C_{gc} << C_{ge} \approx C_{res} \Rightarrow i = C_{res} \cdot dV/dt$), charges the gate capacitance; in this way, the gate voltage can reach the IGBT threshold voltage and a conduction current appears.

Photo 1 shows the waveforms during a spurious dV/dt turn-on giving prominence to the simultaneous presence of high voltage and high current.

If the output impedance of the drive source is high this phenomenon occurs more easily because of the higher ratio between the reflected V_{ge} and the applied dV/dt.

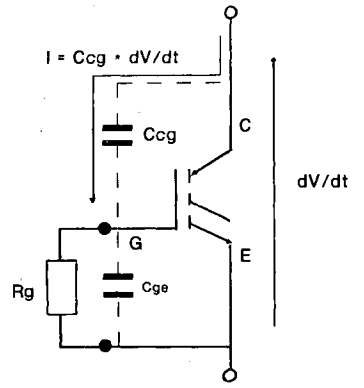


Fig.1 - Current flow through IGBT capacitances due to dV/dt

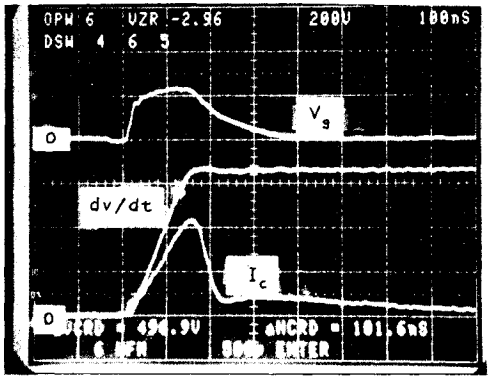


Photo 1 - Waveforms during a spurious turn-on due to static dv/dt condition.
Gate voltage = 2V/div,
Drain Voltage = 200V/div,
Drain current = 2A/div.

Thus the main parameters influencing an IGBT's behaviour in static dV/dt condition are:

- device characteristics (C_{res}, C_{ge}, V_{th}, g_{fs})
- temperature
- R_{ge}, dV/dt value
- gate bias

1.2 The influence of temperature.

When the temperature increases, IGBT parameters vary as follows:
- transconductance at low current increases
- threshold voltage decreases
- turn-off time increases

As a consequence, when the temperature increases the power losses due to dV/dt turn-on increase and the phenomenon occurs at a lower dV/dt value.
Photo 2 shows a comparison of the peak current at T_j = 25°C and T_j = 100°C with the same static dV/dt conditions.

1.3 The influence of dV/dt and R_{ge}.

The effect of R_{ge} and dV/dt can be evaluated with the simplified circuit in fig.2 but the mathematical resolution is not easy because of the influence of the voltage on C_{gc} and C_{ge}. The behaviour of SGS-THOMSON's IGBTs were characterized by the test circuit in fig.3, taking care to measure the energy dissipated in the devices at Tc = 100°C $E = \int v(t) \cdot i(t)dt$.

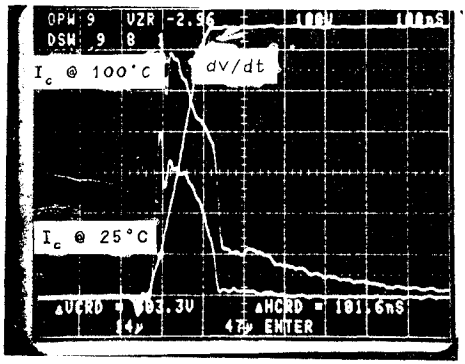


Photo 2 - Comparison between the peak current due to static dv/dt with Tc = 25°C and Tc = 100°C, ID = 2A/div, V_D = 100V/div, Rg = 100 W, E@25°C = 226 mJ, E@100°C = 1. 2m6 mJ

The curves in fig.4 show this measured energy versus both R_{ge} and a typical dV/dt.
Considering a single curve, dV/dt = constant, it can be observed that it has a minimum constant value for R_{ge} lower than the "knee" value.
In this region IGBT parasitic turn-on does not occur and the absorbed energy only charges the IGBT output capacitance.

1.4 The influence of gate bias.

Gate bias voltage influence was analyzed for negative voltage (V_{EE}) using the test circuit in fig. 3.
Figs.5 and 6 show that, when V_{EE} = -5V spurious turn-on does not occur even if the value of the resistance connected to the gate is high (180Ω). Looking at the waveforms in fig. 7 we can note two different effects on the gate voltage due to the negative bias. The first is obviously that the gate voltage is offset from V_{EE} and the second is that there is a different gate voltage peak even if the applied dV/dt is the same. This happens because of the influence of gate voltage on C_{ge}.
Photo 3 shows the gate charge curve and clearly demonstrates the variation of the slope

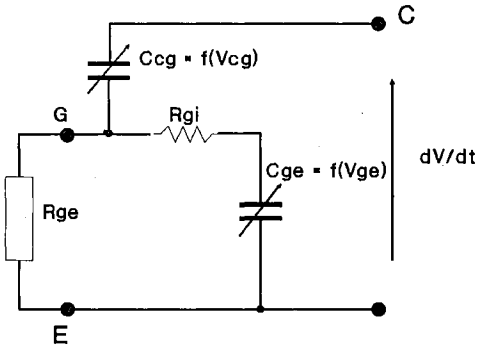
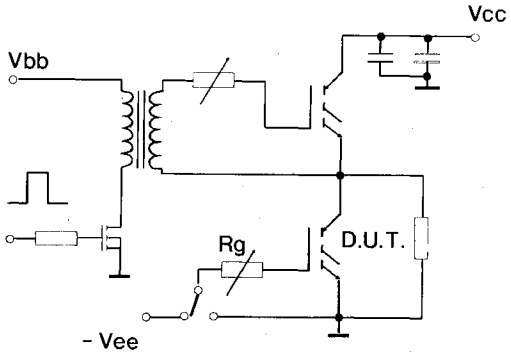


Fig. 2 - Simplified input circuit.



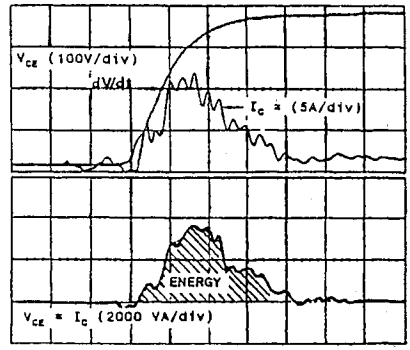


Fig. 3 - Test circuit and related waveforms

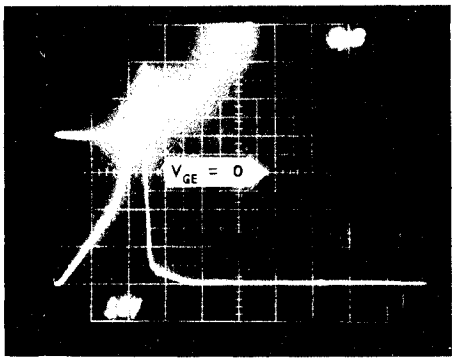


Photo 3 - Gate charge. Curve Vge = 2V/div. Vce = 100V/div

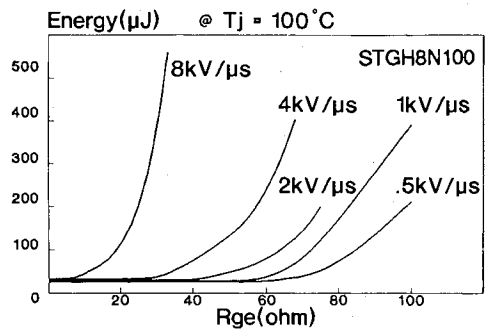


Fig. 4 - Energy dissipated versus R_{ge} and dV/dt

of the voltage occuring at V_{ge}=-2V. If V_{ge} is greater than this value then $C_{ge} = C_{ies}$ (input capacitance, output short circuited) if V_{ge} is lower than this then C_{ge} is about four times C_{ies} and reduces the gate voltage peak.

2. HOW TO AVOID PARASITIC dV/dt TURN-ON.

The previous paragraph shows that it is possible to avoid undesired turn-on during dV/dt by:

a) connecting gate and emitter by a low turn-off resistance

b) reducing dV/dt

c) biasing the gate, during the off state, with a negative voltage

2.1 LOW R_{ge} VALUE DURING THE OFF PHASE.

Depending on the required performance, this solution can be applied as follows:

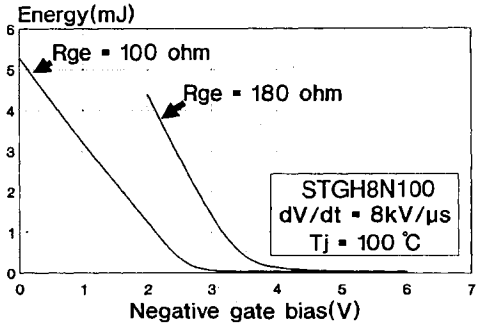


Fig. 5 - Dissipated energy versus negative gate bias and R_{ge}

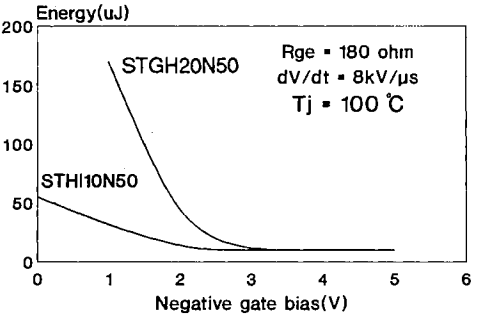


Fig. 6 - Dissipated energy versus negative gate bias

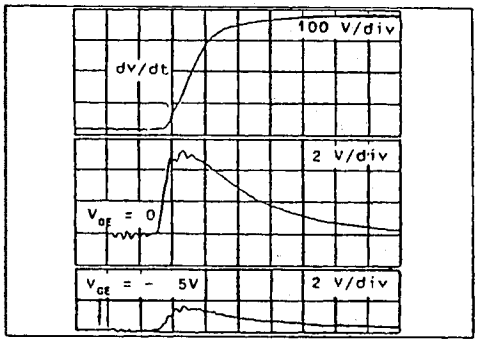


Fig. 7 - Comparison of gate voltage behaviour with and without negative bias

1) R_{ge} is the gate turn-off resistance as shown in fig.8a.

2) R_{ge} is connected just after turn-off as shown in fig.8b.

The disadvantage of the driving circuit shown in fig.8a is that this circuit does not guarantee the full safe operating area (RBSOA) when Rgs is less than 100Ω, for the following reasons:

- the latching current depends on dV/dt during turn-off
- R_{ge} strongly influences dV/dt at turn-off
- the RBSOA is guaranteed for $R_g = 100\Omega$

Fig.9 shows this behaviour and the diagram in fig.10 shows that the maximum R_{ge} necessary to avoid dV/dt problem is less than 100Ω
Thus, the driving circuit of fig.9 is suitable for applications where the full safe operating area @ Rg = 100Ω is not required.
The driving circuit of fig.8b turns-off the IGBT with Rg = 100Ω obtaining the full RBSOA but the delay "d= $t_{storage}$ + t_{fall}" for each must be optimised for each application.

2.2 Reduction of dV/dt.

The spurious turn-on problem due to dV/dt is typical of the circuit shown in fig.11; in this circuit, the free-wheeling diode in the parallel with the lower IGBT, which is in the off state, is turned off during the upper IGBT turn-on and a high dV/dt is generated.
Thus, dV/dt value depends on :

- complementary IGBT turn-on speed (dI/dt)
- free-wheeling diode "softness"
- wiring inductances

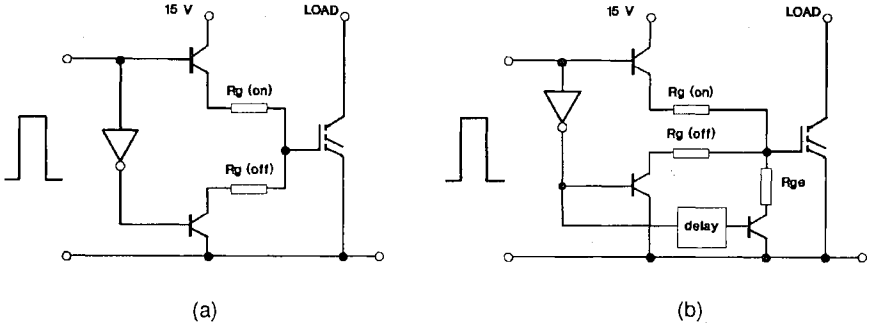


Fig. 8 - IGBT driving circuits

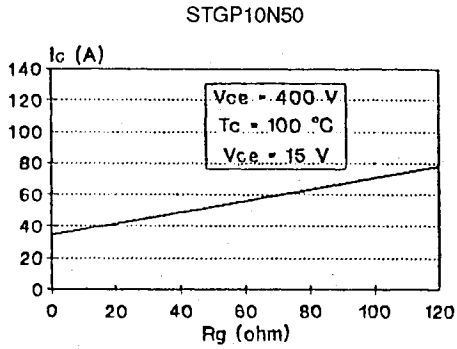


Fig. 9 - I_{latch} versus R_{goff}

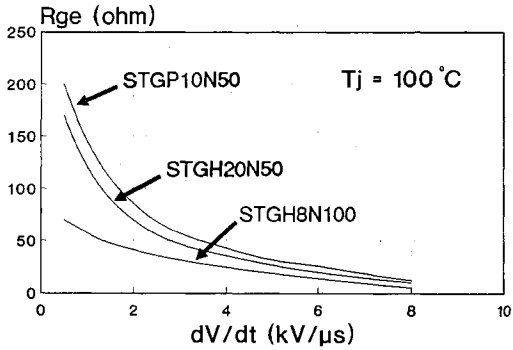


Fig. 10 -Max R_{ge} values that avoid static dV/dt turn-on versus dV/dt

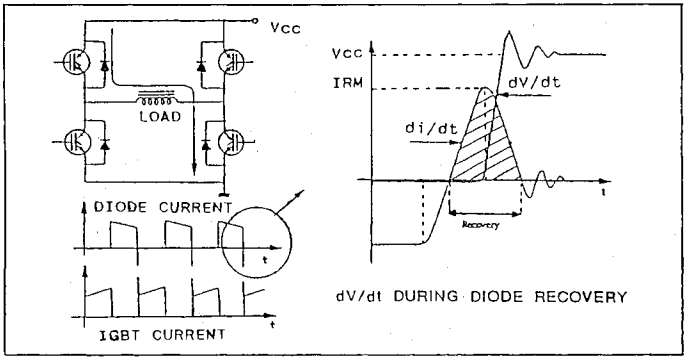


Fig. 11 - Typical circuit where static dV/dt conduction can occur.

Diode current recovery
during turn-off = 10A/div

Drain voltage and dv/dt
due to the diode turn off 200V/div.

Current due to spurious
turn-on with Rgs = 100 Ω2A/div

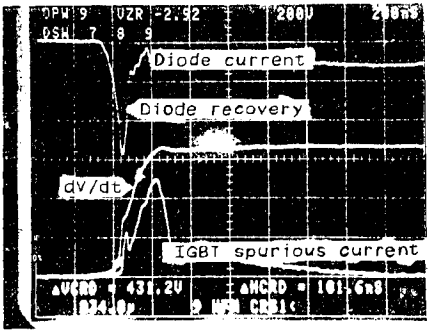


Photo 4 - Waveforms in the circuit of fig. 11 when: R_{gon} = 100 Ω

Diode recovery = 5A/div.

Dv/dt due to diode turn-off 200V/div.

Current in the IGBT in off state 2A/div.

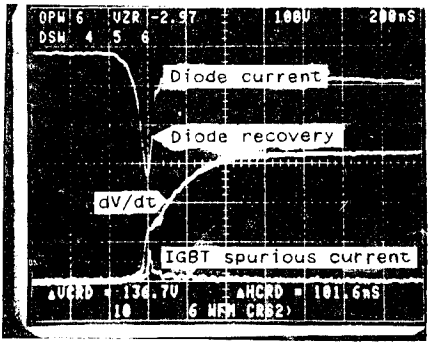


Photo 5 - Waveforms in the circuit of fig. 11 when R_{gon} = 200Ω. In this condition turn-on due the dv/dt does not occur.

and it can be minimized:

- using fast soft recovery diodes.
- reducing wiring length.
- turning on IGBTs slowly, with a high value of turn-on gate resistance.

Photo 4 and 5 show that the dV/dt is reduced to a safe value in the circuit of fig.11. Photo 4 uses a low value of turn-on gate resistance whereas photo 5 uses a high value gate resistance. In the case of photo 5 spurious turn-on due to the dV/dt does not occur.

2.3 driving the IGBT with a negative voltage.

Biasing the gate negatively, as shown in photo 6, causes a higher dV/dt during turn off because of the availability of a large gate current. It is possible to avoid this drawback, which reduces the effective RBSOA, simply by increasing the value of $R_{g(off)}$.

3. DYNAMIC dV/dt.

This condition may occur in a zero current quasi resonant converter where the IGBT works as a thyristor.

In this application, see fig. 12 and photo 6 the IGBT is turned-off when the collector current is zero and the collector voltage starts to rise after a delay time $t_d \approx (2 * f_{resonance})^{-1}$, corresponding to the end of the reverse recovery phase of the antiparallel diode.

This increasing voltage causes a current spike, leading to power losses because of the minority carriers in the IGBT substrate. The amplitude of the spike depends on several factors which involve both IGBT and circuit characteristics. One of the factors is the amount of the stored charge when the dV/dt is applied. The stored charge depends on the type of IGBT (slow or fast), junction temperature and resonant frequency.

Increasing temperature and/or frequency leads

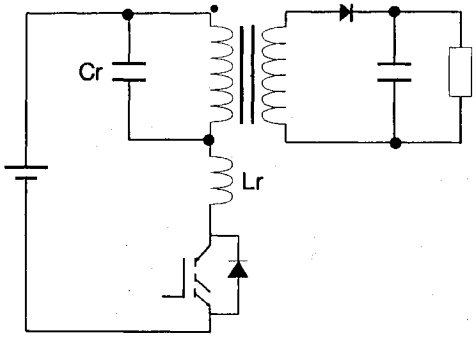


Fig. 12

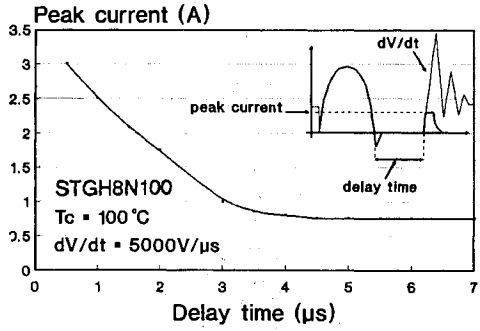


Fig. 13 - Peak current versus t_{delay}

Gate voltage = 10V/div

Drain current = 2A/div

Drain voltage = 200V/div

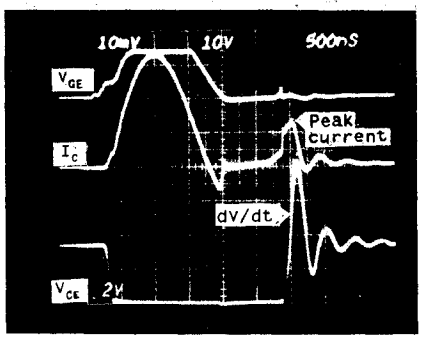


Photo 6 - Waveforms in a resonant converter where dynamic dv/dt occurs. Device = STGH8N100, Tc = 100°C

to a higher current peak. The diagram in fig.13 shows how increasing resonant frequency affects the current peak.
For frequencies lower than about 120 kHz the current peak is constant, because there is no more stored charge and due solely to capacitive effects that are similar to those in Power MOSFETs.
The other factor is related to the rate of voltage rise which depends strongly on the softness of the diode. Using a slower IGBT emphasizes the effects discussed above. In low frequency working conditions the power losses are no longer negligible and must be considered during the circuit design in order to avoid thermal runaway and consequent device failure.

4. CONCLUSION.

The dV/dt phenomenon causes power dissipation in IGBT devices and this may lead to the failure due to thermal runaway. The way to avoid this phenomenon depends on the operating conditions.
When an IGBT works in a static dV/dt condition, as for example in a bridge circuit, it is possible to prevent the dV/dt phenomenon by modifying the design of the IGBT drive circuit:

- reducing dV/dt.
- connecting a low gate-emitter resistance.
- driving the IGBT with a negative voltage at turn-off.

If a high current is to be controlled with a switched mode technique, it is necessary to design the drive circuit to obtain the full guaranteed RBSOA.

When the IGBT works in dynamic dV/dt condition, as in a QRC-ZCS, it is not possible to avoid power dissipation in the device by optimization of the drive circuit. These kind of losses can only be limited by selecting a suitable converter resonant frequency and antiparallel diode.