NOVEL PROTECTION AND GATE DRIVES FOR MOSFETs USED IN DRIDGE-LEG CONFIGURATIONS

BY C. PATNI

INTRODUCTION

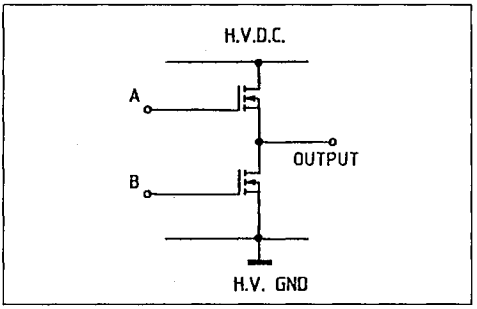
The bridge-leg is an important building block for many applications such as drives and switch-mode power supplies. Simple gate drives with protection for POWER MOSFETs need to be designed for the "low-side" and the "high-side" switches in the bridge-leg. The POWER MOSFET can conduct a peak drain current, I_D, which is more than three times its continuous current rating. The POWER MOSFET peak current capability and its linear operating mode are used to good effect in designing device protection circuitry.

Bridge-leg configurations have a direct bearing on the degree of protection that can be incorporated. Consequently, bridge-leg configurations, protection concepts and gate drives are created simultaneously to design optimised and reliable power electronic circuits.

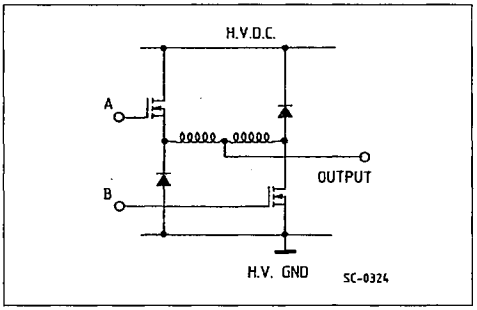
H-BRIDGE USING POWER MOSFETs

Three POWER MOSFET based bridge configurations are illustrated in figure 1. Figure 1a illustrates a bridge-leg which uses the internal parasitic diode as a free-wheeling diode thus reducing cost. However, since the reverse recovery of this parasitic diode is in the order of a microsecond, the turn-on switching times of the POWER MOSFET have to be increased in order to reduce the reverse recovery current. The turn-on time of the POWER MOSFET is controlled such that the pulse current rating of the internal diode is not exceeded. Hence a compromise is made between maintaining the safe operating area of the MOSFET and reducing turn-on switching losses. For example, an SGSP477 MOSFET has a diode pulse current rating in excess of 80A and a typical diode reverse recovery time of 300ns. A rate of change of current at turn-on, limited to 50A/s, is a realistic compromise between reverse recovery current magnitude and turn-on losses. Consequently switching speed is sacrificed for cost. For switching frequencies up to 10kHz, when operating on a 400V DC high voltage rail, this configuration can be chosen as switching losses are limited, thus enabling a realistic thermal design.

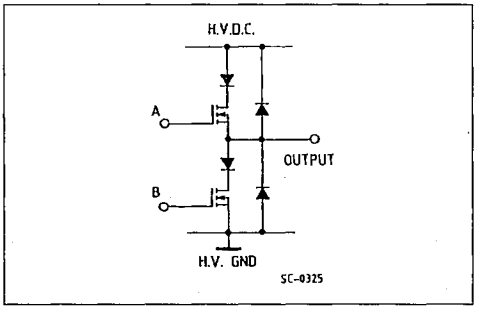
Figure 1 : Bridge Configurations.



a) Bridge-leg using Internal Parasitic Diode.



b) Asymetrical Bridge-leg providing di/dt Protection.



b) Bridge-leg with blocking Diodes.

The turn-off speed of the POWER MOSFET in this configuration has no restrictions. Thus a fast turn-off is desirable to reduce turn-off losses. As the rate of change of current is limited, radio frequency interference (RFI) and electromagnetic interference (EMI) are reduced.

An asymmetrical bridge-leg, illustrated in figure 1b ; can be used to limit di/dt during a short-circuit condition thus providing sufficient time to switch-off the appropriate power devices. The inductors limit the rate of rise of output current. They also limit the freewheeling current through the internal parasitic diodes of the MOSFETs. Adding external freewheel diodes and inductors increases reliability at the cost of increased complexity. The inductors reduce RFI and EMI as the rate of change of current is limited.

The configuration illustrated in figure 1c has Schottky "blocking" diodes to prevent current going through the MOSFET internal parasitic diodes. Schottky diodes are often used since conduction losses are kept to a minimum.

Bridge configurations shown in figure 1b and 1c are considered for high frequency switching applications. The advantage of the asymmetrical bridge-leg configuration over the bridge configurations in figures 1a and 1c is that the bridge-leg is capable of withstanding simultaneous conduction of the two devices in the bridge-leg since there are series inductors which reduce the dI/dt under this condition. Hence the short-circuit detection loop time is not so critical and the devices are not stressed with high dI/dt and high pulse currents.

The choice of the bridge configuration depends on the technical specification of the application. For example, if the technical specification for a specific application can be met by using the configuration shown in figure 1a, then this configuration should be used as costs are lower than with the other two configurations shown in figures 1b and 1c.

GATE DRIVE CIRCUITS

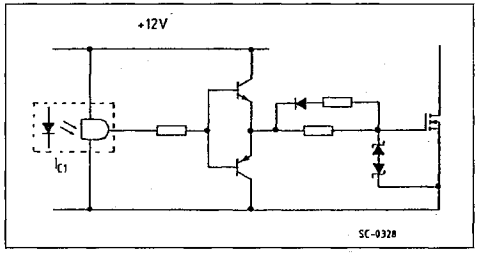
The POWER MOSFET is a voltage controlled device, unlike the bipolar transistor which requires a continuous base drive. An application of a positive voltage between the gate and the source results in the device conducting a drain current. The gate to source voltage sets up an electric field which modulates the drain to source resistance. The following precautions should be considered when designing the gate drive ;

1 - Limit V_{GS} to 20V maximum. Use of a gate to source voltage in excess of 16V has a marked effect on the lifetime of the device.

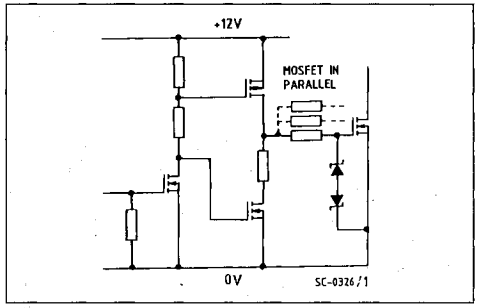
2 - Gate drive parasitic inductance can cause oscillations with the MOSFET input capacitance. This problem becomes more pronounced when connecting devices in parallel.

3 - There should be sufficient gate to source voltage for the transistor to be fully conducting.

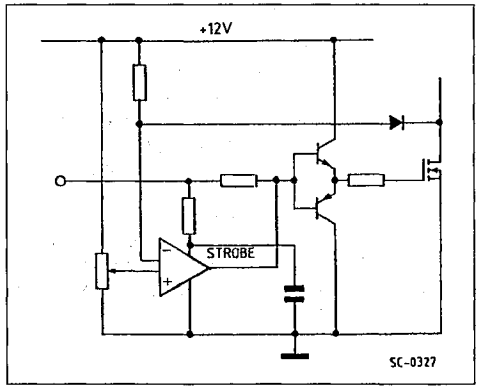
Figure 2 : Gate Drive Circuits.
a) Isolated gate drive with controllable switching times.



b) Simple gate drive for N-Channel MOSFETs in parallel.



c) Gate drive with VDS (on) control for short-circuit protection.



Bipolar, MOSFET, CMOS or open-collector TTL logic can be used in the design of simple high performance gate drives. Totem-pole buffers, (figure 2a), are often effectively used to control the turn-on and turn-off individually. Figure 2b illustrates a total MOSFET based gate drive with which the switching speeds at turn-off can be individually controlled. CMOS or open-collector TTL logic can be used to drive MOSFETs directly, provided an ultrafast switching speed (50ns) is not necessary. In motor drive applications switching speeds of 100 to 200 nanoseconds are sufficient as switching frequency is seldom in excess of 50kHz. Discrete buffers are used to provide high current source and sinking capability when improved switching speeds are required or when MOSFETs are connected in parallel.

Short-circuit protection techniques similar to bipolar transistors may be considered for MOSFETs. $V_{DS(on)}$ monitoring permits the detection of short-circuit conditions which lead to device failure. The device can be switched off before the drain current reaches a value in excess of the peak pulse current capability of the MOSFET. This form of protection is very effective with MOSFETs as they can sustain a pulse current in excess of three times the nominal continuous current. Figure 2c illustrates a gate drive which incorporates $V_{DS(on)}$ monitoring and linear operating mode detection for the MOSFET in the case of short-circuit conditions. When the MOSFET is turned on the on-state voltage of the device ($V_{DS(on)}$) is compared with a fixed reference voltage. At turn-on, $V_{DS(on)}$ monitoring is inhibited for a period of approximately 400ns in order to allow the MOSFET to turn-on fully. After this period, if $V_{DS(on)}$ becomes greater than the reference value, the device is latched-off until the control signal is turned-off and turned-on again.

"HIGH-SIDE" SWITCH GATE DRIVES

The top transistor in a bridge-leg requires a "high-side" gate drive circuit with respect to the bridge ground. Three possible gate drive concepts are shown in figure 3 :

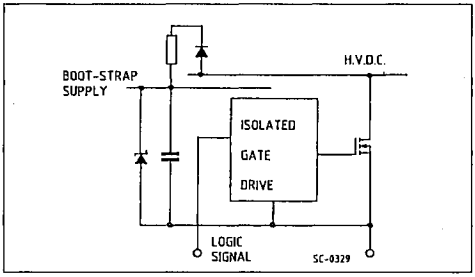
a) The "bootstrap" drive, requiring logic signal isolation, but no auxiliary floating supply.

b) The level shifting drive.

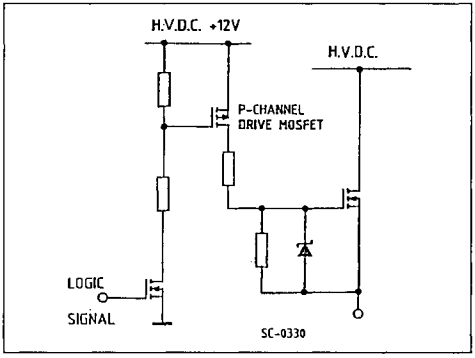
c) The floating gate drive with optically coupled isolators, pulse transformers or DC to DC chopper circuit with transformer isolation.

Figure 3 : Gate Drives for Top Transistor of Inverter Leg.

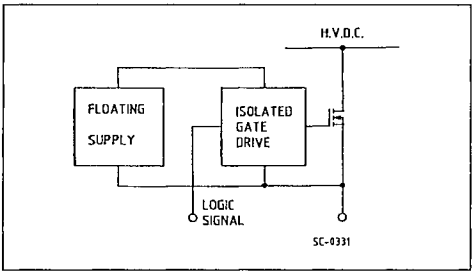
a) "Bootstrap" supply floating gate drive.



b) Level shifting gate drive.



c) Floating supply isolated gate drive.



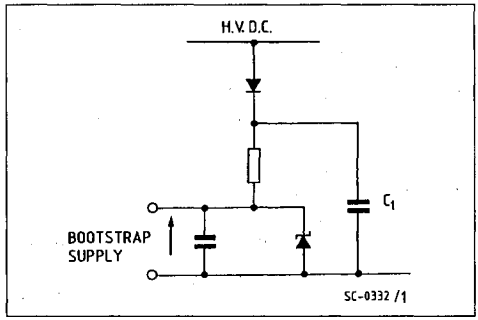
Bootstrap supplies are particularly well suited to POWER MOSFET gate drives which require low power consumption. Figure 4 illustrates two bootstrap supply techniques. Bootstrap supplies limit transistor duty cycle since they require a minimum transistor off time during which they are refreshed.

Supply efficiency and maximum duty-cycle are parameters which govern the design of the bootstrap. Figure 4a illustrates a conventional bootstrap with an additional capacitor, C1, which improves the maximum duty cycle as the supply is refreshed even during transistor on time by this capacitor. Figure 4b illustrates a high efficiency bootstrap supply which uses a small MOSFET, Q1, for regulation. In this design a low power bootstrap drives the gate of Q1.

The level shifting gate drive, (figure 3b), requires a high voltage p-channel MOSFET which drives the n-channel power device. The p-channel MOSFET is switched using a resistor divider network. No floating supplies are required. A power supply of 12V, referenced to the high voltage d.c., is used to provide positive gate source voltage for n-channel POWER MOSFET. This circuit eliminates the need for logic signal isolation and a floating supply. The disadvantage of this circuit is the high cost of the p-channel drive MOSFET.

Figure 3c illustrates a floating gate drive with a floating supply. This drive is the most expensive out of the three shown in figure 3. However, the floating supply need only have a low output power, since MOSFETs are voltage controlled devices. The advantages of this drive are its high efficiency and unrestricted transistor duty-cycle.

Figure 4 : Bootstrap Supply Techniques.
a) Conventional bootstrap with additional capacitor C1.



b) High efficiency bootstrap.

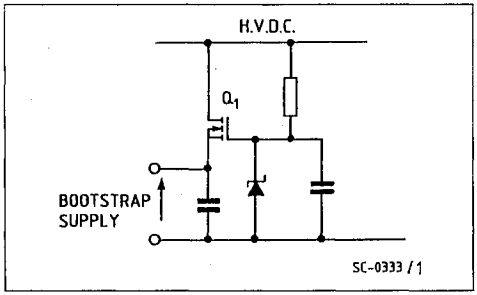
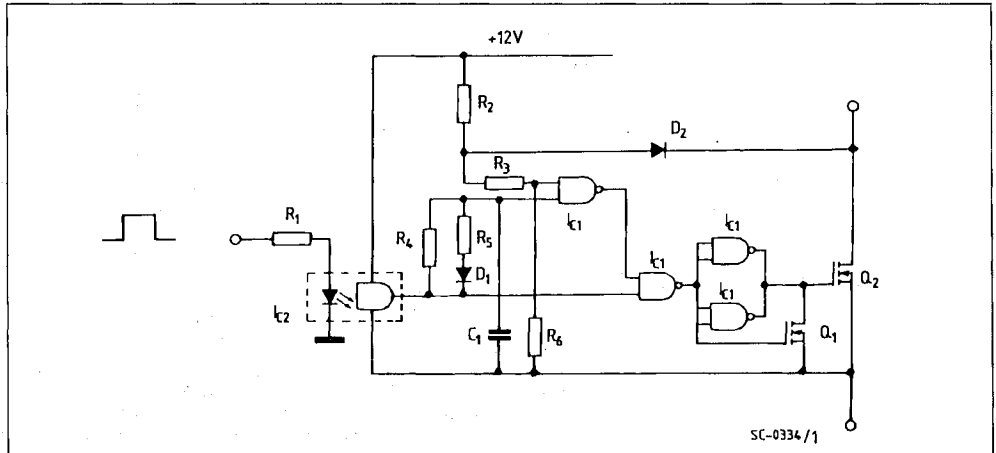


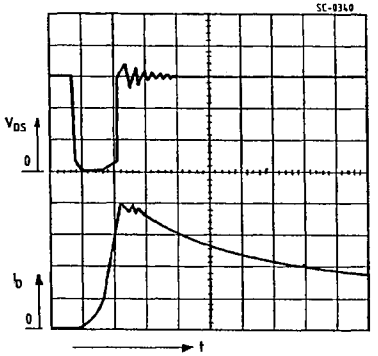
Figure 5 : Isolated CMOS Drive with V_{DS} Control for Short-circuit Protection.



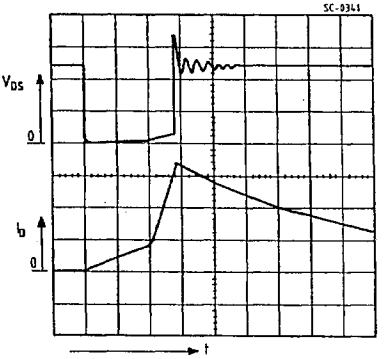
R1	= Dependent on application	R4	= 1kΩ	I_{C2}	= HCPL2200	Q1	= BSS100
R2	= 10kΩ	R5	= 120kΩ	C1	= 560pF	Q2	= SGSP477
R3	= 22kΩ	R6	= 56kΩ	D1	= 1N41448		
		I_{C1}	= HCF4093	D2	= BYT11/600		

Figure 6 : Short-circuit Conditions for an SGSP477 V_{DS} & I_D.

V_{DS} : 50V/DIV
I_D : 10A/DIV
t : 2µs/DIV
a) Output to high voltage short-circuit.



b) Output to Output Short-circuit.



PROTECTION

Power electronic circuits such as bridge-legs are often required to have protection against output to output short-circuit, over-temperature, simultaneous conduction of devices in series in a bridge-leg and output to high voltage supply or ground rail short-circuit. These power stages are generally part of an expensive system such as a machine-tool or a robot motor drive. Thus the additional cost of protection circuitry is commercially acceptable. A compromise is generally reached between equipment costs and the degree of protection required.

Short-circuit protection of a power MOSFET can be achieved by either $V_{DS(on)}$ monitoring or a current sense. In the previous section gate drives using the $V_{DS(on)}$ monitoring technique were presented. Figure 6 illustrates the MOSFET drain to source voltage, V_{DS}, and the drain current, I_D, when short-circuits are experienced by the POWER MOSFET, SGSP477, driven by the gate drive illustrated in figure 5.

The MOSFET is turned-off when the drain current increases sufficiently and $V_{DS(on)}$ monitoring is inhibited for a period of 400ns to allow the device to turn-on fully.

An inductor is used in series with the device, as illustrated in figure 1b. This inductor saturates when a large short-circuit current flows. The rate of change of the short-circuit current due to the saturation of this inductor is illustrated in figure 6a and 6b. Figure 6a illustrates the POWER MOSFET drain to source voltage, V_{DS}, and the drain current, I_D, when a bridge-leg output to high voltage supply rail short-circuit occurs. Figure 6b illustrates an output to output short-circuit of two bridge-legs.

Another protection technique uses the "current mirror concept", (1). An image of drain current is obtained by having a small MOSFET, (integral or discrete), in parallel with the main power MOSFET as illustrated in figure 7.

Figure 7 : The Current Mirror.

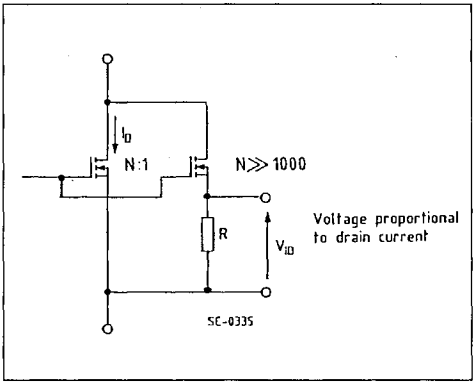
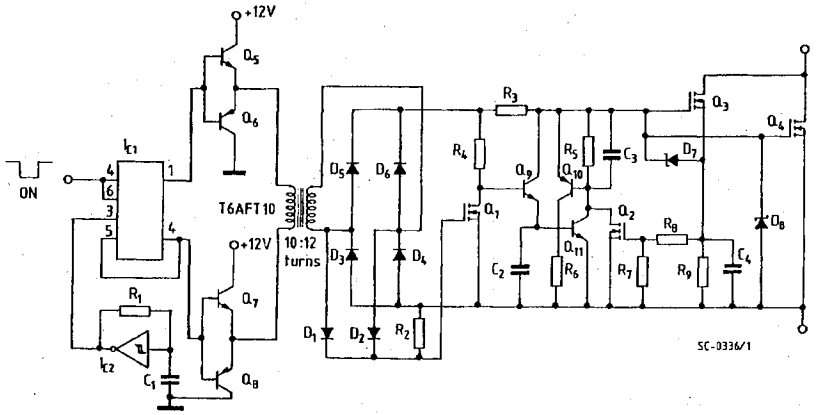


Figure 8 illustrates a floating gate drive which utilizes a pulse transformer for transmitting simultaneously the MOSFET on-signal together and the gate to source capacitance charging current. The current mirror technique is used to provide short-circuit and over-load current protection. The pulse transformer operates at an oscillating frequency of 1MHz when a turn-on control signal is present.

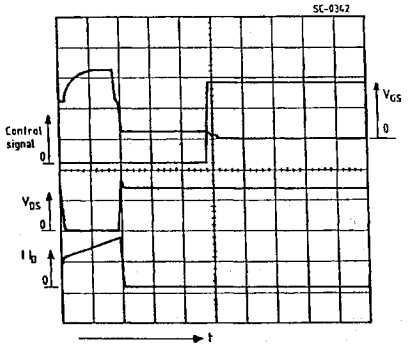
The secondary is rectified to provide the gate source capacitance charging voltage. The current mirror provides a voltage "image" of the main MOSFET drain current. This voltage is compared with a fixed reference voltage in order that the gate drive be latched-off when the drain current becomes in excess of a specificed value. Figure 9 illustrates how the MOSFET, SGSP477, is latched-off when the drain current exceeds 10A with this gate drive circuit.

Figure 8 : Pulse Transformer Gate Drive with Current Mirror Protection for an SGSP477.



R1 = 470Ω	R9 = 100Ω	D4 = 1N4148	Q4 = SGS477
R2 = 1kΩ	C1 = 330pF	D5 = 1N4148	Q5 = BC337
R3 = 33Ω	C2 = 10nF	D6 = 1N4148	Q6 = BC327
R4 = 2kΩ	C3 = 10nF	D7 = BZX85C15	Q7 = BC337
R5 = 100Ω	C4 = 220pF	D8 = BZX85C15V	Q8 = BC327
R6 = 100Ω	D1 = 1N4148	Q1 = small	Q9 = BC337
R7 = 100Ω	D2 = 1N4148	Q2 = signal	Q10 = BC327
R8 = 100Ω	D3 = 1N4148	Q3 = n-channel MOSFETs	Q11 = BC337

Figure 9 : Overload Current Protection using Current Mirror Concept with the Gate Drive of Figure 8 for an SGSP477.



Time scale : 5µs/DIV – I_D : 5A/DIV – V_{DS} : 100V/DIV
Control signal : 5V/DIV – V_{GS} : 5V/DIV.

CONCLUSION

MOSFET based bridge-leg configurations requiring protection and floating gate drives have been presented. Novel self-protecting gate drives for the "high-side" and "low-side" switching have been discussed. These drives provide protection against output to high voltage d.c., output to ground and output short-circuit. For the high-side switch "bootstrap" supply gate drive, level shifting gate drive and floating supply isolated gate drives have been compared.

Protection against short-circuit condition has been demonstrated using $V_{DS(on)}$ monitoring and the current mirror concept. Both techniques are well suited for protection against short-circuit conditions. However, the current mirror concept also provides a sufficiently linear image of the current for regulation.

REFERENCES :

1. Fuy G.
Current-mirror FETs cut costs and sensing losses EDN September 4 th, 1986.