SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

HOW SHORT CIRCUIT CAPABILITIES GOVERN THE DESIRED CHARACTERISTICS OF IGBTs

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ABSTRACT.

Short circuit tolerance of IGBTs can be obtained by the optimization of both the protection circuit and the intrinsic ruggedness of devices.

This note discusses application design criteria and IGBT characteristics compared to the intrinsic short circuit ruggedness.

1.0 INTRODUCTION.

The continuous growth of IGBT applications requires more differentiation of device electrical characteristics. In fact, the structure of IGBTs makes them flexible to use and their switching performance can be specifically matched to many different applications.

For the best match between application requirements and IGBT characteristics, some compromise between the saturation voltage, switching speed and ruggedness is necessary.

To define the suitable IGBT short circuit ruggedness specification, this note analyzes the parameters influencing their behaviour during short circuit operation, and verifies the performance of the more usual short circuit protection compared to IGBT short

circuit ruggedness.
It is also shown that modification of the IGBT structure improves the short circuit performance without compromising the saturation voltage and switching speed.

2.0 SHORT CIRCUIT OPERATION OF IGBTs.

Static and dynamic characteristics are not sufficient to predict the short circuit behaviour of IGBTs. Also, dynamic phenomena correlated to stray parameters and to the short circuits circumstances must be carefully considered.

2.1 SHORT CIRCUIT MODES AND WAVEFORMS.

Real short circuit mode can be simulated using the test circuits "A" and "B" illustrated respectively in figure 1 and figure 5.

TEST CIRCUIT "A": The device is turned on when the collector is directly connected to the supply voltage and the short circuit inductance can be changed.This circuit simulates either a short circuit in one leg of a bridge circuit, or a permanent short circuit of the load [4].

The waveforms of figure 2 show the behaviour in the test circuit "A" when all the stray parameters are reduced to a minimal value. The effect of a significant short circuit inductance is shown in figure 4. The inductance, the reverse capacitance "C_{RS}", the gate capacitance "C_G", R_G, together with the IGBT amplification, constitute a resonant R,L,C circuit as shown in figure 3. Hence di/dt at turn-on generates a very high peak current due to a gate voltage overshoot.

TEST CIRCUIT "B": The short circuit is actived during the on-state. In this case a dV/dt is applied to the collector when the gate voltage is high and the device is in full conduction. This condition simulates accidental short circuit of the load during normal operation [4].

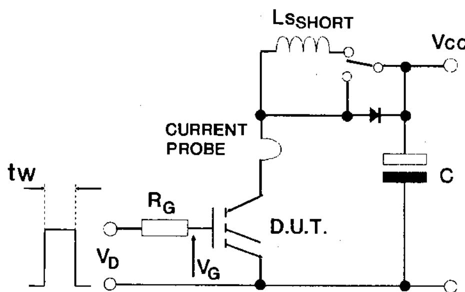

Fig. 1. Testcircuit "A" $L_{SHORT} \approx 4\mu H$, $L_{STRAY} \approx 150nH$.

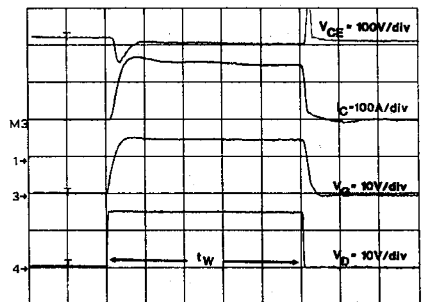

Fig. 2. Short circuit test with short circuit inductance = L_{STRAY}. Time scale: 2µs/div.

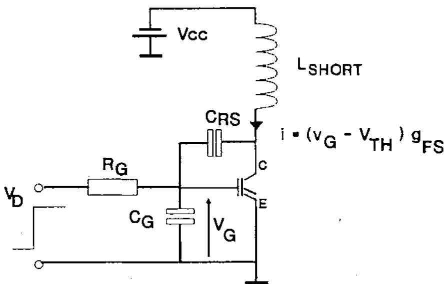

Fig. 3. Simplified equivalent circuit of the short circuit condition.

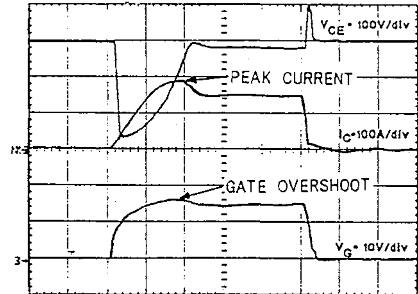

Fig. 4. Short circuit test with short circuit inductance = L_{SHORT}. Time scale = 2µs/div.

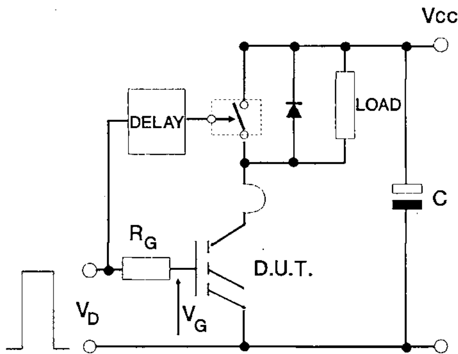

Fig. 5. Test circuit "B". Short during saturation.

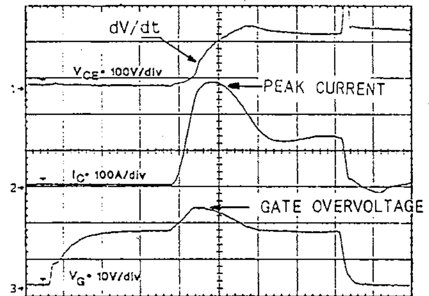

Fig. 6. Effect of the dV/dt when the short circuit occurs during IGBT full conduction. t = 2µs/div.

The waveforms of figure 6 show the effect of the dV/dt in the test circuit "B". The dV/dt acting trough reverse capacitance causes the gate voltage to rise over the driving voltage [6]. A peak current much higher than short circuit current is generated.

2.2 SHORT CIRCUIT STRESSES.

The failure of IGBTs during short circuit condition occurs either with static latch or with dynamic latch of the parasitic SCR of the structure (figure 14) [2]:

- Static latch is due to the high current density.
- Dynamic latching is due to the high dV/dt at turn-off.

The influence of the temperature is critical because the latching current decreases when temperature increases. Moreover, during short circuit there is a very fast temperature rise due to the very high energy increase dissipated in the device.

For this, gate voltage overshoot must be avoided and the short circuit current must be reduced as much possible. In fact:

During overshoot, the collector current ($i_C = g_{FS}(v_g - V_{TH})$) can reach the static latching current, especially if the transconductance of the device is high.

At turn-off the junction temperature is higher than at turn-on, so the dV/dt due to the stray inductance "Ls_C" can cause a dynamic latch-up.

Moreover, the stray inductance "Ls_C" creates an overvoltage at turn-off (see figures 2,4,6) due to the di/dt. If the di/dt at turn-off is not controlled by a suitable gate resistance the overvoltage can reach breakdown causing device failure.

2.3 PARAMETERS INFLUENCING SHORT CIRCUIT BEHAVIOUR (figure 7).

The main parameters influencing static and dynamic short circuit behaviour are:

- Transconductance g_{FS}, C_G, C_{RS} (Device parameters)
- Driving voltage V_D, R_G (Driving circuit)
- Ls_C, Ls_E (Stray inductance of lay-out and of capacitance)
- Ls_{SHORT}, dV_{CE}/dt, V_{CE} (Short circuit conditions)

The stray inductances Ls_E (emitter-ground) and Ls_G (gate-drive) mainly influence di/dt at turn-on, but they are not critical for usual circuit lay-out and must be carefully considered, only when devices are paralleled [8].

Transconductance g_{FS} is the most critical parameter. In fact, a high value of g_{FS} can generate very high continuous short circuit current and very high peak current during transient.

2.4 SHORT CIRCUIT CAPABILITY CHARACTERIZATION.

In order to make test conditions as reproducible as possible, the short circuit capability characterization was implemented using test circuit "A" with stray inductances reduced to minimum value.

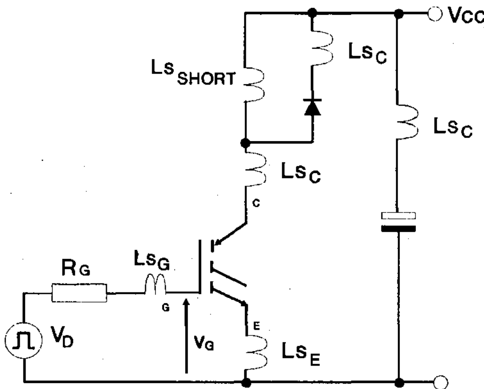

Fig. 7. Circuit parameters influencing short circuit current of the IGBTs.

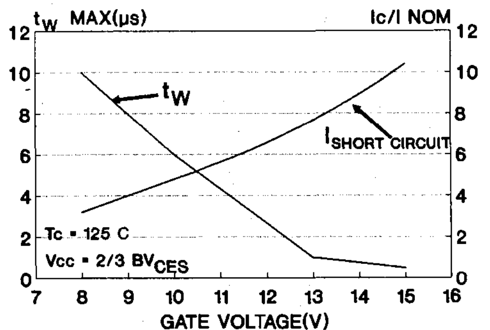

Fig. 8. Short circuit performance versus gate bias of IGBTs having a high transconductance. Maximum current overshoot ≤ 20% $I_{SHORT\ CIRCUIT}$.

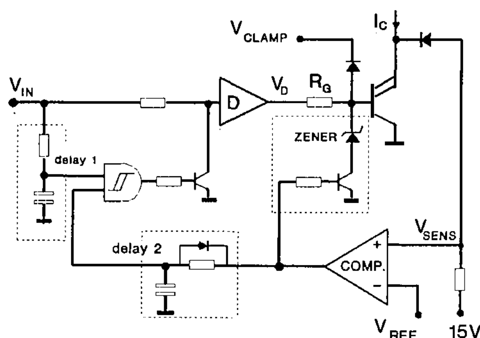

Fig. 9. Short circuit protection with high false alarm immunity.

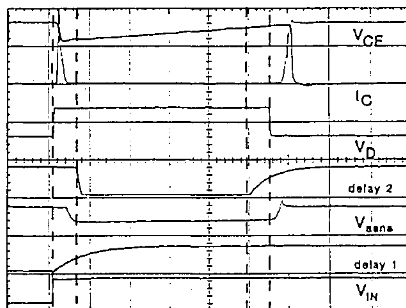

Fig. 10. Timing diagram of the protection circuit at turn-on and during overcurrent condition.

Short circuit capability is expressed in terms of:

- MAX SHORT CIRCUIT TIME (t_W as defined in figure 2)
- SHORT CIRCUIT CURRENT & PEAK CURRENT (I_{SHORT}, I_{PEAK})
  Versus: - V_G, R_G, T_C, V_{cc}.

Figure 8 shows a characterization example of a IGBT having a high value of the transconductance. For $V_G \geq 13V$ the device fails at turn-on due to static latch-up.

3.0 SHORT CIRCUIT PROTECTION.

To ensure short circuit tolerance of a power control system and of its output power switches, the following problems must be carefully considered:

1 - Limitation of the short circuit current.

2 - Limitation of short circuit protection delay.

3 - Nuisance tripping creating false alarm.

3.1 DESCRIPTION OF THE PROTECTION CIRCUIT.

The figure 9 shows the schematic diagram of a protection circuit using the IGBT saturation voltage for sensing. Sensing resistors or current transformers can also be employed without significant changes.

The zener diode limits the gate voltage during a short circuit condition so limiting short circuit current.

Delay 1 and delay 2 realized with a R, C filter and Schmitt trigger avoid activation of the protection circuit in case of false short circuit conditions. Delay 1 must filter transitory phenomena at IGBT turn-on, delay 2 gives noise immunity to the circuit.

The diode "**D2**" clamps gate voltage overshoots due to dV/dt.When a short circuit is detected the IGBT is turned off by its gate resistor in order to limit dV/dt and collector overvoltages.

The timing diagram in figure 10 shows the working mode of the circuit at turn-on and with an overcurrent condition during operation:

- At turn-on, the input 1 of the "AND" becomes high (IN_{HIGH} = 8V) after delay 1; If IGBT saturation was not detected (IN_{LOW} = 2V) during delay 1 the driving circuit input taken low.

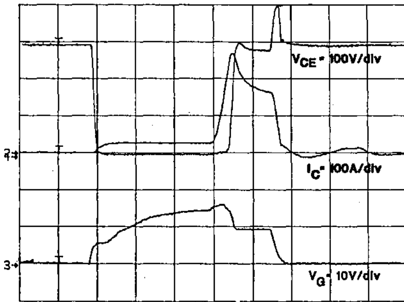

Fig. 11. Short circuit protection waveforms in the test condition "B". IGBT is TSG50N50DV. Time scale: 2μs/div.

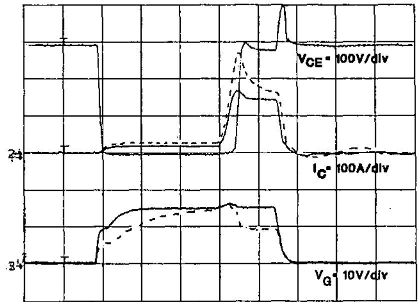

Fig. 12. Short circuit waveforms without voltage reduction of a IGBT having low transconductance compared to waveforms of figure 11 in dotted lines. t = 2μs/div.

- When, during normal operation, there is a overcurrent condition, the IGBT saturation voltage reaches reference voltage "V_{REF}" and the comparator activate the zener and the delay 2. If the overcurrent condition continues after delay 2, then the driver input is pulled down and the IGBT is turned-off.

This circuit works as a monostable multivibrator with positive edge triggering, but the IGBT is "ON" only if V_{IN} is high, so the noise immunity is assured. If a overcurrent or a short circuit condition were detected, it is necessary to take V_{IN} to the low.

3.2 PERFORMANCE OF THE PROTECTION CIRCUIT.

When the short circuit exists at turn-on (test circuit "A"), test conditions of the characterization are respected.

The performances of the circuit can be critical when the short circuit occurs during normal working conditions and the device is in full saturation. Figure 11 shows that a significant current overshoot stresses the IGBT (STGP50N50) under this short circuit condition even if the protection works correctly.

In fact the protection circuit needs a delay to pull the gate voltage to a safe value. This delay depends on the saturation voltage detection time and on the discharge time of the IGBT input capacitance. The discharge time can be significant due to the Miller effect during collector voltage rise. Moreover a high value of g_{FS} can induce a very sharp rise of the current during delay.

To avoid this phenomenon, IGBTs with a lower value of saturation current and transconductance should be employed. In fact, if the short circuit current is limited by the device itself, then it is not necessary to reduce the gate voltage during short circuit time. Figure 12 shows collector current and gate voltage waveforms of an IGBT having low saturation current ($I_{Csat} = 3 \cdot I_{NOM}$ @ $V_G = 15V$) subjected to the same short circuit condition shown in figure 11 and without any gate voltage reduction, compared to the STGP50N50 with high transconductance and gate voltage reduction during short circuit (same waveforms of figure 11 in dotted lines).

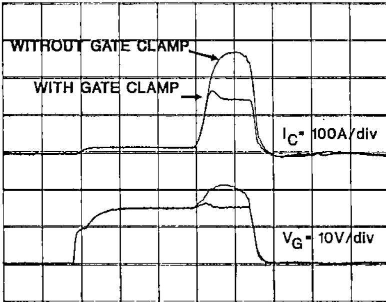

Fig. 13. Gate voltage and collector current with and without gate voltage clamping. t = 2μs/div.

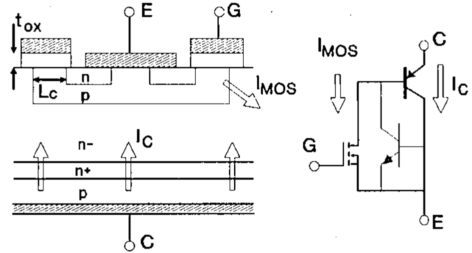

Fig. 14. Cross section of IGBT structure and simplified equivalent circuit.

If the gate voltage reduction is eliminated a fast clamping circuit is necessary. Figure 13 shows a comparison of the gate voltage and collector current waveforms with and without gate clamping voltage. This diode also limits gate voltage overshoots in the short circuit condition.

3.3 SHORT CIRCUIT SPECIFICATION OF IGBTs.

The criteria for providing short circuit protection to match the reliability of the more usual protection circuits are:

- $t_W > 5\mu s$ (delay to avoid false allarm)
- $I_{Csat} < 3 \cdot I_{NOM}$ (to ensure safe turn-off)
- $T_c = 125°C$ (working temperature)

5μs is the time necessary to ensure full saturation of IGBTs.

To give sufficient margin for safe operation $t_W \approx 10\mu s$.

4.0 DESIGN OF AN IGBT UNDER SHORT CIRCUIT CONDITIONS

The intrinsic short circuit ruggedness of IGBTs was improved by a optimization of the device structure aimed at obtaining a suitable value of the saturation current ("I_{Csat}" @ V_G=15V, Tj=150°C).

Parameters influencing transconductance and I_{Csat} ($I_{Csat} = g_{FS} \cdot (V_G - V_{TH})$ saturation current also affect saturation voltage "V_{CEsat}" [2] as shown by (1) and (2).

$$I_{Csat} = \frac{1}{(1-\alpha_{PNP})} \frac{\mu_{ns} C_{ox}}{2} \frac{Z}{L_C} (V_G - V_{TH}) \quad (1)$$

$$V_{CE} = \frac{KT}{q} \ln \left[\frac{(1-\alpha_{PNP}) dI_C}{2qW_R Z D_a niF(d/L_a)} \right] + \frac{(1-\alpha_{PNP}) L_C I_C}{\mu_{ns} C_{ox} Z (V_G - V_{TH})} \quad (2)$$

Where "L_C" is the channel lengh, "Z" is the channel perimeter, "C_{ox}" is the oxide capacitance ($C_{ox} = \varepsilon\, S/t_{ox}$).

I_{Csat} can be limited both by reducing the gain of the PNP transistor (α_{PNP}) and by acting on the MOSFET characteristics (L_c, Z, C_{ox}).

"α_{PNP}" influence both the PN junction threshold (first term of equation (2)) and the second term. For this reason only the MOSFET characteristics were optimized, so gaining advantages both in dynamic performances (C_G reduction) and in thermal stability [8].

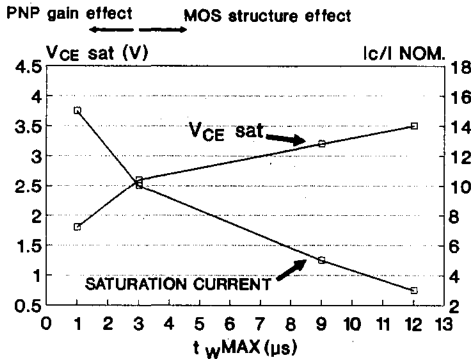

Fig. 15. Trade-off between saturation voltage and the short circuit ruggedness expressed as MAX t_w and saturation current @ $V_G = 15V$.

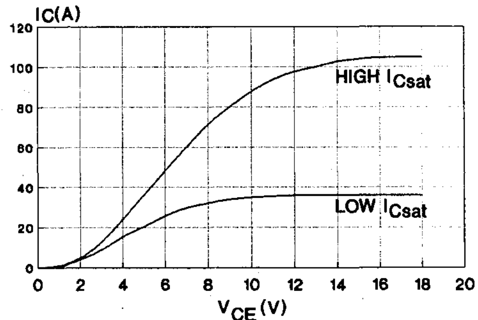

Fig. 16. Comparison of two IGBT output characteristics, with low I_{Csat} (ICsat ≈ INOM) and HIGH I_{Csat} ($10 \cdot I_{NOM}$) @ $V_G = 15V$.

To reduce the saturation current by 70%, channel lengh (L_c) and oxide thickness "t_{ox}" were increased by 40%. This gives the best compromise between short circuit performances and saturation voltage as figure 15 and 16 show.

The lefthand side of figure 15 shows the effect of the PNP gain reduction due to life time reduction processes.

5.0 CONCLUSION.

The analysis of parameters influencing short circuit operation of IGBTs has led to the design of a suitable protection circuit, even for devices having modest short circuit performance.

This solution allows the use of IGBTs with very low saturation voltage.

However, an additional very fast circuit that reduces gate voltage during short circuit is necessary. During the delay of this circuit the dV/dt due to the IGBT desaturation can cuase a dangerous peak current. IGBTs having low transconductance can solve this problem.

Deacreasing transconductance of a IGBT causes saturation voltage to increase. The optimization of the IGBT structure allowed the realization of an IGBT with sufficient short circuit capability (t_W MAX = 10 µs), and with a value of V_{CEsat} that is 20% higher than the V_{CE}sat of a IGBT having t_W MAX = 1µs. This IGBT requires a simplified short circuit protection network and it does not compromise the efficiency or the short circuit ruggedness of the system.

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