ENVIRONMENT DESIGN RULES OF MOSFET IN MEDIUM POWER APPLICATION

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ABSTRACT

The use of POWER MOSFET allows high switching speed in power applications above 10kW. Nevertheless the main limitations come from the characteristics of the circuit design. From a practical example, this paper analyses and proposes solutions to adapt the POWER MOSFET and the layout in order to minimize parasistic inductances. Special emphasis is given to the driver circuit, package, wiring rules and voltage spike protection at turn-off.

I - INTRODUCTION

POWER MOSFETs are now considered standard tools by circuit designers working at tens of Amps and hundreds of Volts. Their traditional advantages (easy drive and over current capability) remain true when switching over 10KWatts. Nevertheless, the main limitations encountered are not from the MOSFET itself as it can switch high current at high speed (over 1000Amps/sec), but from characteristics of the circuit design. After presentation of a specific example of Power MOS drive, the optimisation of the power devices and the layout will be analysed in the practical example of a chopper operating with ISOFET (1000V - 0.7Ω or 100V - 0.014Ω). Finally, an over-voltage protection circuit is presented.

II - HIGH POWER MOS DRIVE

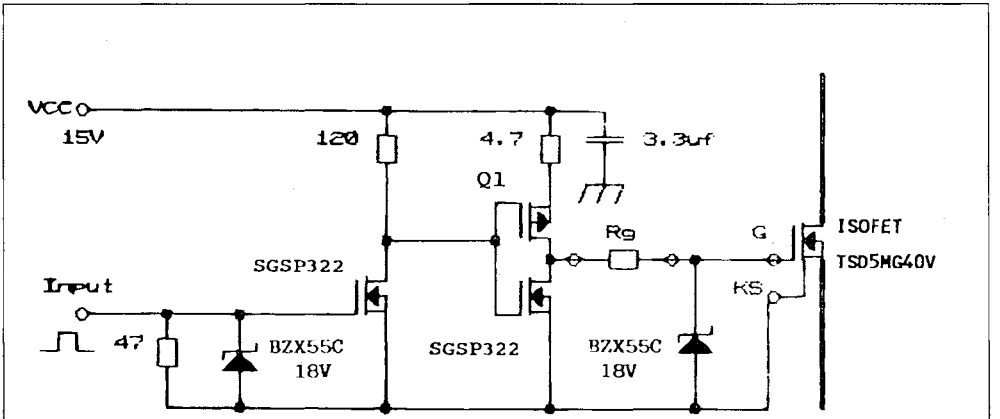
Even with high power switching (over 10KW), the driver circuit can be very simple (fig. 1), comparable to the ones used for low power circuits.

The major characteristics of a POWER MOSFET is its high input capacitance (ie : $C_{iss} \approx 12nF$ for 100V - 14mΩ MOSFET) which must be rapidly charged and discharged when switching without creating oscillations.

The following rules have been used for the design of the driver :

- A low dynamic internal impedance which permits peak current greater than 1Amp for 300nanosec to charge and discharge the ISOFET input capacitance.
- A low impedance circuit reduces the sensitivity to dV_{DS}/dt at turn-off of the ISOFET.
- The total resistance of the gate circuit must be greater than 5Ω in order to sufficiently damp the circuit preventing oscillations and possible parasitic turn-on of the ISOFET.

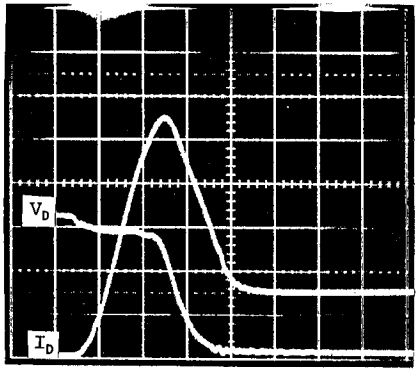
Figure 1 : Driving Circuit for ISOFET Over 10kW Switching.



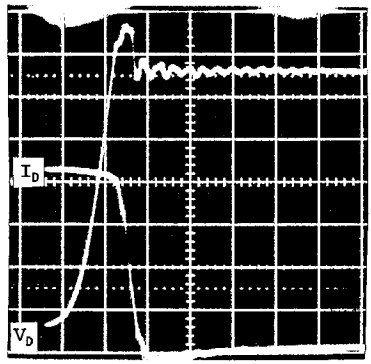
Q_i = 100V 0.4Ω P-channel MOSFET

- The links between drive and gate, short and non-inductive, are made between the gate pin and the "Kelvin Source" pin. The use of the "Kelvin Source" pin is very important when driving Power MOS. It avoids parasitic effects caused by dI/dt in the source lead.
- The gate protection Zener diode has to be mounted close to the ISOFET package.

Figure 2 : Over Current Capability and Switching Speed with ISOFET TSD5MG40 (1000V – 0.7Ω – I_D = 13A).
a. Turn-on ; the ISOFET controls 30A-650V and sustains 110A peak (8 x I_D). The over current is due to the recovery of the free-wheeling diode (BYT230PIV 1000).
b. Turn-off ; with dI/dt = 1600A/usec ; and dV/dt = 15000V/usec.
The switched power = 25kW ; and the switching losses = 1.3mj



a. Turn-on
VD = 200V/div
ID = 20A/div
t = 50ns/div.
Rg = 5Ω



b. Turn-off
VD = 100V/div
ID = 10A/div

III - LAYOUT DESIGN FOR HIGH SPEED SWITCHING

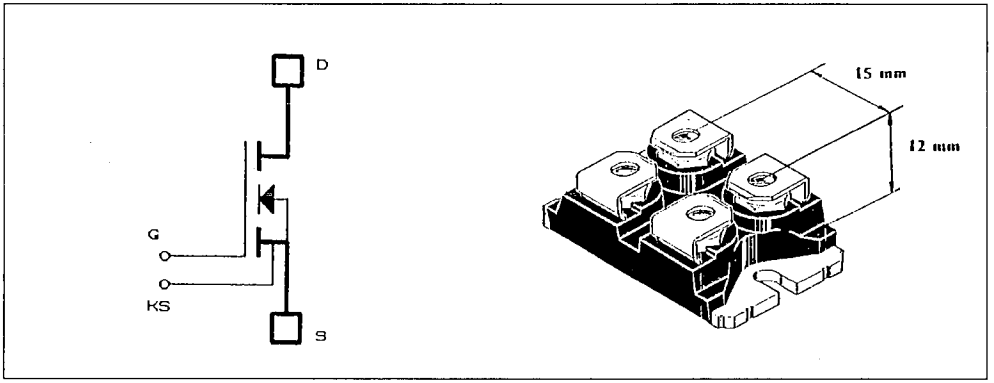
The reduction of the parasitic inductances is a major challenge for power switching especially with a power MOSFET switching over 1000Amps/usec (figure 2). With this switching leading edge, a 10cm diameter wiring loop causes a 100V voltage overshoot. To solve this potential problems two actions are necessary : choosing a well adapted device and optimise the layout design.

a. Adapting the device to the layout

ISOFET is a MOSFET housed in an ISOTOP package (figure 3) :

- The ISOTOP package can be directly screwed on the printboard because all of its terminals are at the same level. Therefore, all inductances due to the length of external wiring connexions, are eliminated.
- As a result of a low profile package (12mm), the internal parasitic inductance is less than 10nH. Moreover, its Kelvin source (KS) enables the minimisation of disturbances induced by the power circuit in the driver circuit.
- Even though it has a thermal resistance value of only 0.25°C/W, the case is fully internally insulated at 2.5kV_{RMS}. Therefore it can be mounted near to the diode package on a common heatsink in order to obtain a very compact circuit layout.

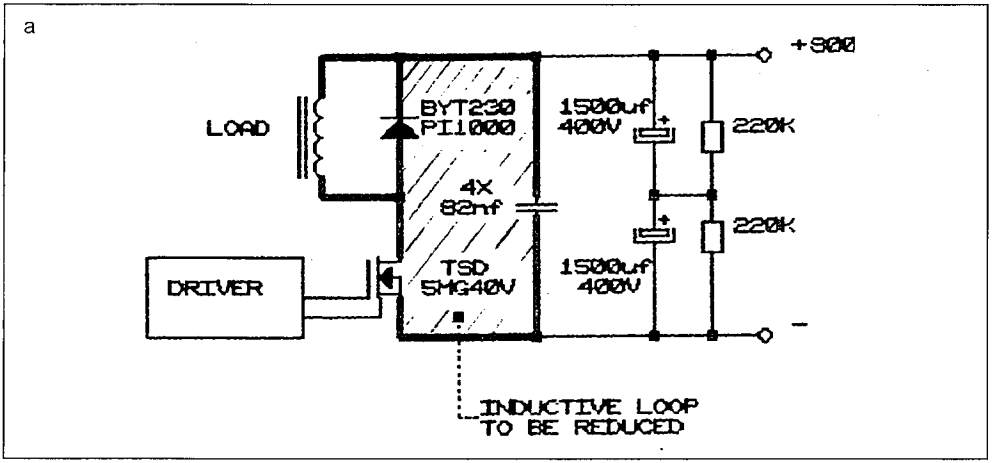
Figure 3 : An ISOFET is a MOSFET housed in an ISOTOP package, which has a low profile.
It is easily integrated in low inductive layouts.
The "Kelvin Source" lead (KS) separates the gate circuit from the internal inductance of the source connection.

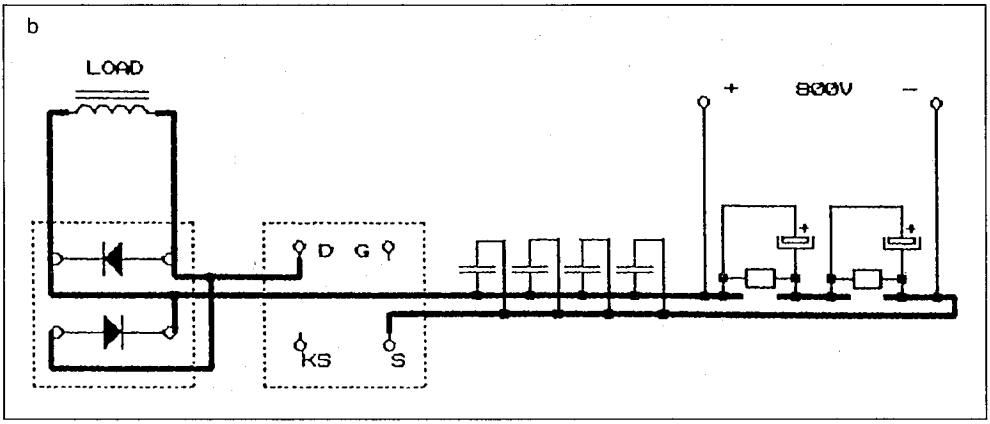


b. Design of the layout

The chopper shown in figure 4 contains two active components : the Power MOS and the freewheeling diode ; both in ISOTOP package screwed side by side, on a common heatsink and directly connected on the printed circuit board (PCB).

Figure 4 : a. Chopper Schematic showing the Inductive Loop to be Reduced.
b. The Same Circuit with two ISOTOP Packages (diode and ISOFET). The packages and links adopt an "in line" configuration in order to reduce the inductive loop.





By observation of the facts presented in appendix 1, the design rules used for the layout are summarized :

- Use of double sided PCB where each high current path is immediately above its returns path on the other side of the board.
- The current densigy has been reduced by enlarging the copper tracks in order to decrease the local dI/dt and consequently the resulting induced voltage.
- Use of several links instead of one, between two large copper tracks, avoids high current concentrations and reduces the inductance (figure 5).
- Decoupling capacitors have been configured in the same direction as the direction of current flow. This prevents the formation of an inductive loop. (compare figure 6a and figure 6b hatched surfaces).
- The use of several smaller capacitors in parallel permits reduction of the equivalent internal parasitic inductance. (figure 6c).
- Choose components (e.g. capacitors) specified with a low internal inductance. (electrolytical capacitor 700µF/400V can have a parasitic inductance of several tens of nH). Prefer the capacitor packages which minimize the inductive connection length.

Figure 5 : Junction between two wide copper tracks is less inductive when several spaced links are used rather then a single link.

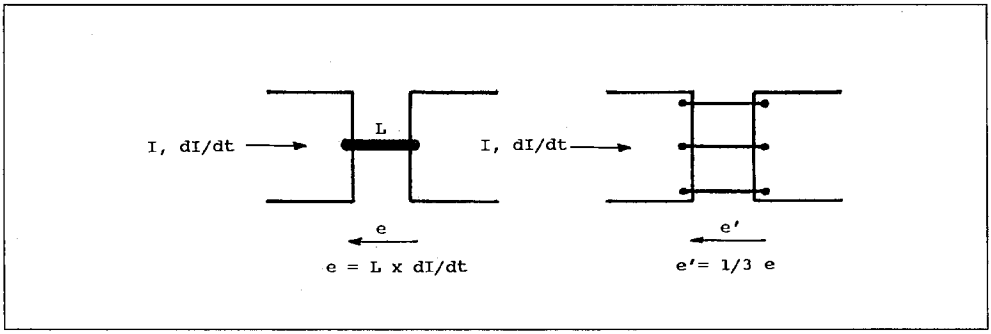
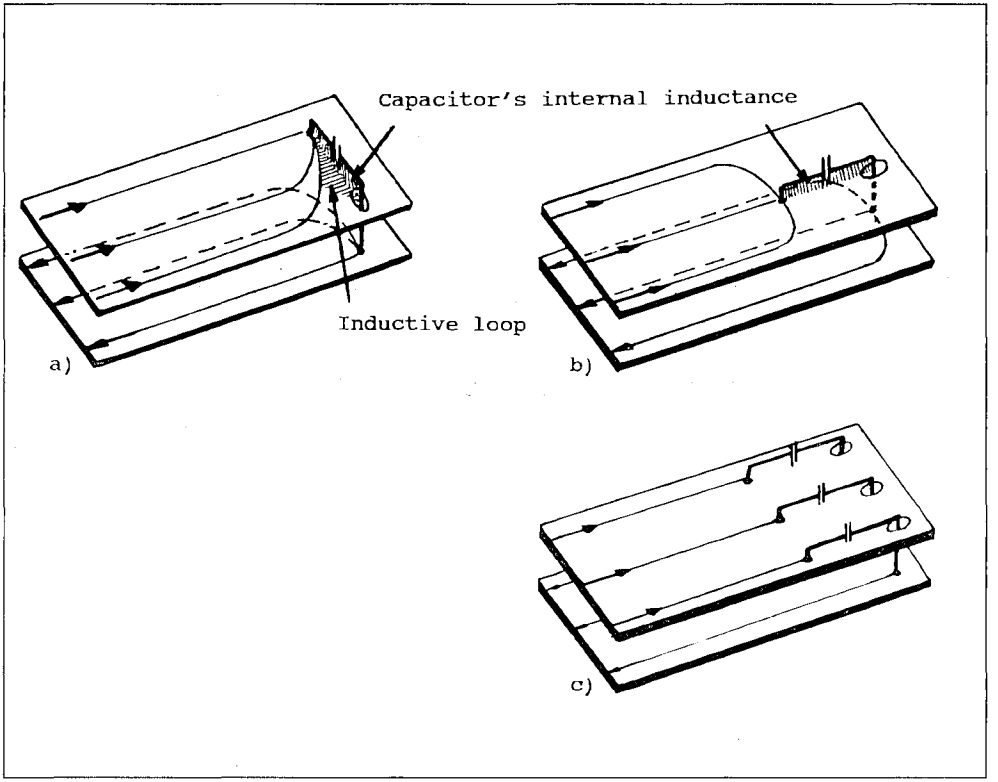


Figure 6 : Configuration of Decoupling Capacitors :

a. An inductive loop is formed, perpendicular to the current flow, because the current flow is not super imposed near the capacitor,

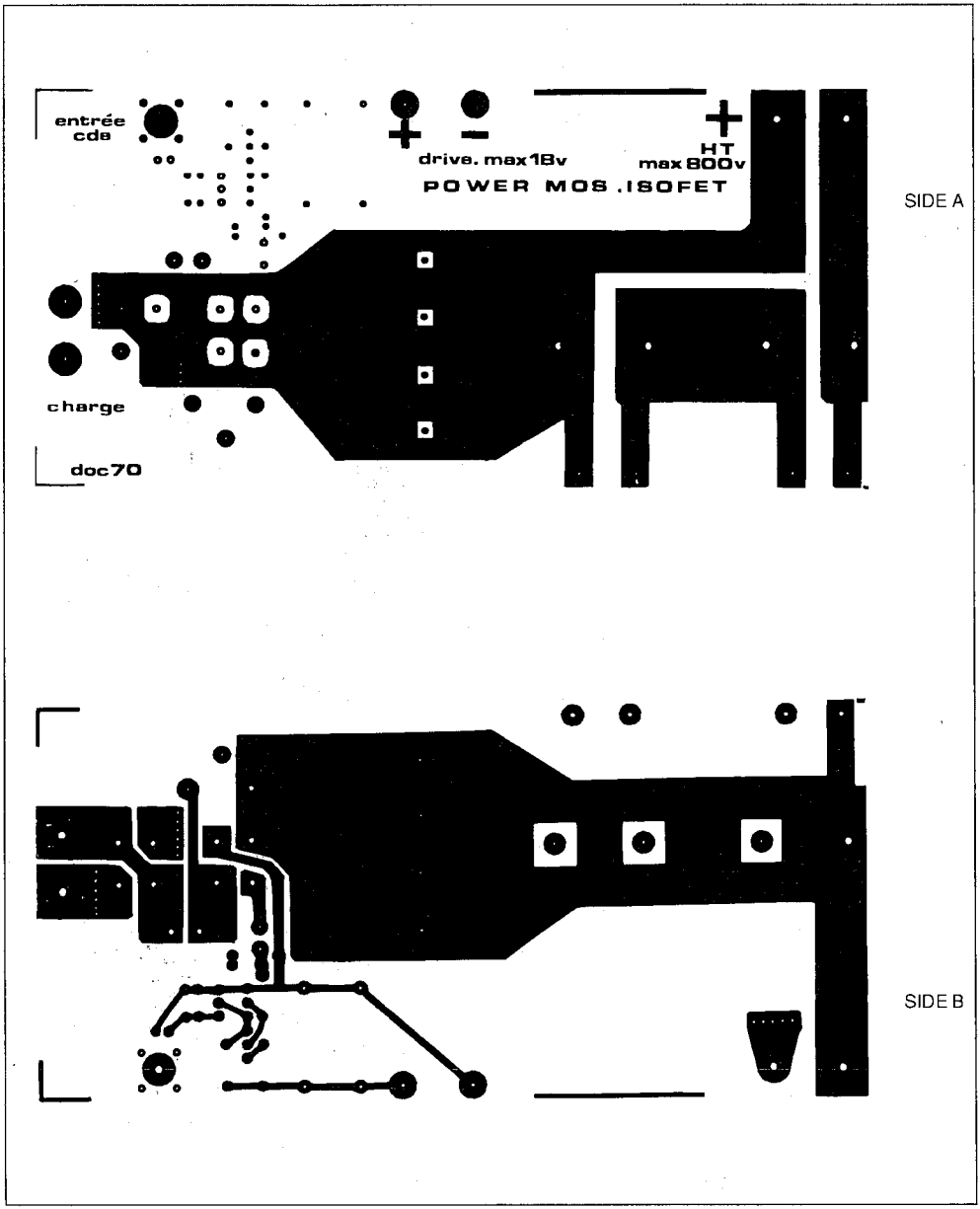
b. Capacitor lying in the same direction as the direction of current flow. inductive loop minimised.

c. Several smaller capacitors in parallel reduce their equivalent internal parasitic inductance for the optimum solution.



As a result the residual inductance of the finished layout (fig. 7) has been measured as 35nH, (fig. 8) plus 15nH when a current sensing loop ($15mm^2$) is added to the layout.

Figure 7 : A Double Side Very Low Inductive Print Circuit Board. (scale : 0.5)
Note the Multi Links (A) to connect One Side to the Other.



IV - OVERVOLTAGE DURING TURN OFF

We have previously seen that by following these sound rules a parasitic inductance value of 35nH can be achieved. It represents the sum of several small components : active components, passive components and PCB. It seems difficult to reduce it further in a circuit without paralleling several power switches.

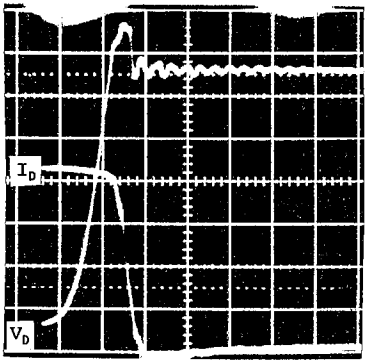
In view of the ISOFET fast switching speed at turn-off (1000Amp/usec), the inductive voltage spike with 35nH will be 35 Volts. This overvoltage is acceptable for devices rated over 500V. It is not negligeable in low voltage applications such as battery powered equipment.

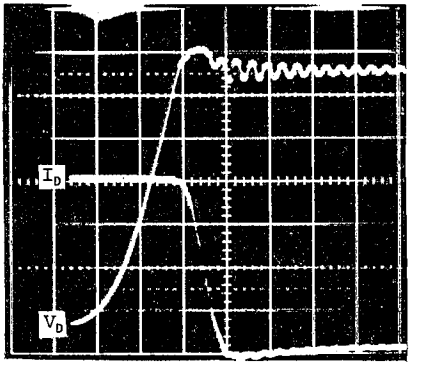
Two solutions are possible :

a. Slowing down the ISOFET

The switching speed at turn-off can be slowed down by increasing the gate resistor value. This method increases the commutating time and consequently the switching losses. These losses are increased by 50% when R_g increases fro 5 to 10Ω. (figure 8).

Figure 8 : Increased Gate Resistor reduces dI/dt and Overvoltage at Turn-off. (driver circuit fig. 1). The total parasitic inductive loop (50nH) includes the inductance of the sense current loop.
I_D = 10A/div V_D = 100V/div t = 50ns/div (ISOFET TSD5MG40V 1000V – 0.7Ω)
Switched power = 25kW ; Switching losses = 1.3mJ in (a) and 2.0mJ in (b).





b. Protection against over-voltage at turn-off

Use of a MOSFET with a low margin for the rating voltage ($V_{BR(DSS)}$) can be achieved by using active protection (i.e. Transil) in order to clamp the voltage spikes.

One solution is to connect a Transil acros the drain-source leads. In this case, the energy is dissipated in the Transil which has to be cooled in order to dissipate the average power.

(1/2 LI^2f = 20W with 40nH, 100A, 100kHz)

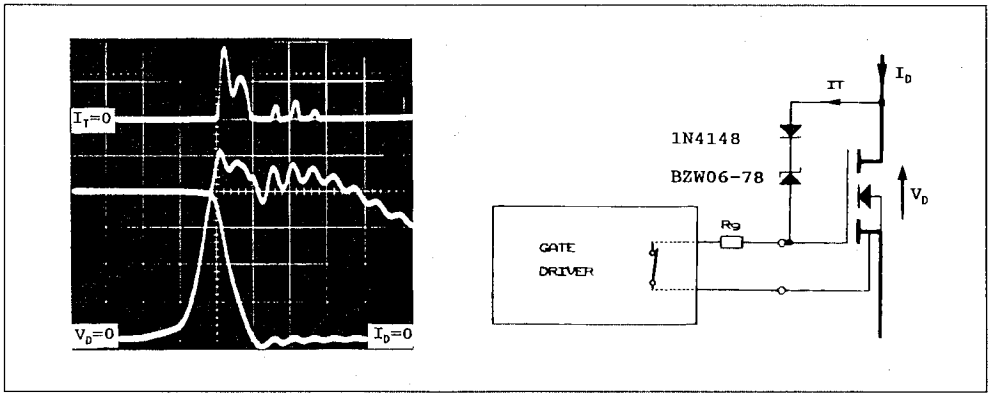
We have chosen another solution by connecting the Transil across the drain-gate leads (figure 9). When the over voltage transient reaches the clamping voltage, the clamping current goes through the gate resistance and biases gate above 5V. (ex : 1A into 5Ω).

This way, the clamping power is dissipated in the MOSFET and a smaller Transil is required (P ≈ 1W at 100kHz in our case).

As the Transil does not heat up, the clamping voltage does not vary with temperature. The equivalent dynamic resistance is very low because the serial resistance of the Transil is divided by R_g and by the MOSFET transconductance.

The current though the Transil being low, the voltage to be considered for its choice is the breakdown voltage at test level (V_{BR} at I_R) instead of the surge clamping voltage (V_{CL}). The Transil breakdown voltage should be chosen to be lower than the maximum desired clamping voltage less 5 Volts to take into account the MOSFET gate threshold voltage.

Figure 9 : Over Voltage clamping by a Transil across the Drain-gate Leads durring turn-off. (ISOFET TSD4M150V 100V – 14mΩ). Upper Trace shows the Current in the Transil (IT). I_D = 20A/div, V_D = 20V/div, I_T = 1A/div, t = 100ns/div.



V - CONCLUSION

MOSFETs switching power over 10kW have the same basic advantages as lower power Mosfet. The driving circuit remains very simple and the over current capability is huge. A specific emphasis has been placed on the minimization of circuit layout inductance. Because of the very fast switching (easily over 1000A/s) it is advantageous to use :

- packages like ISOFET which minimise their internal inductance and allow easy connection to printed circuit board and to heatsink. Also Kelvin Source contact to minimise drive circuit interference.
- double side printed circuit board with symmetrical copper tracks, reduced current concentration, and components positioned in order to minimise parasitic inductance.
- overvoltage protection which avoids oversizing the voltage rating of MOSFETs in low voltage applications.

BIBLIOGRAPHY

[1] An Innovative High Frequency High Current Transistor Chopper. L. PERIER ; E.P.E. Bruxelles 1985.

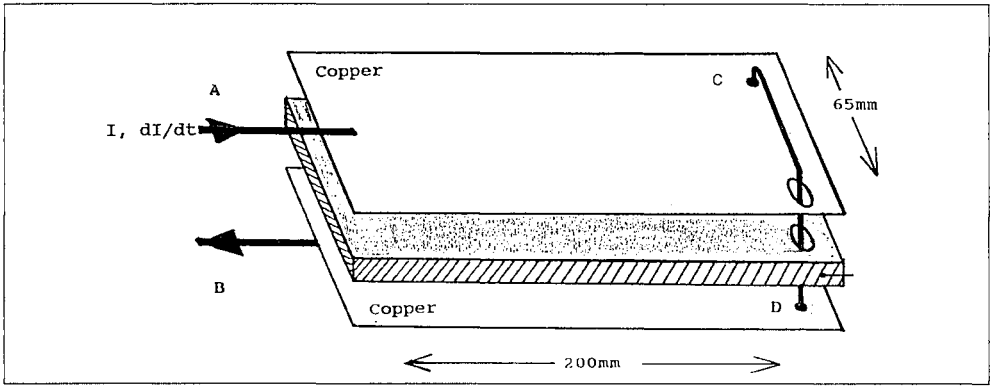
[2] POWER MOS DEVICES Data Book 1st edition June 1988 SGS-THOMSON Microelectronics.

APPENDIX 1

MEASUREMENT OF PARASITIC INDUCTANCES ON A DOUBLE SIDED PCB

- In the figure below, the link between points C and D simulates the connection of a capacitor with nop internal inductance, connected on double sided Printed Circuit Board.

Figure 10.

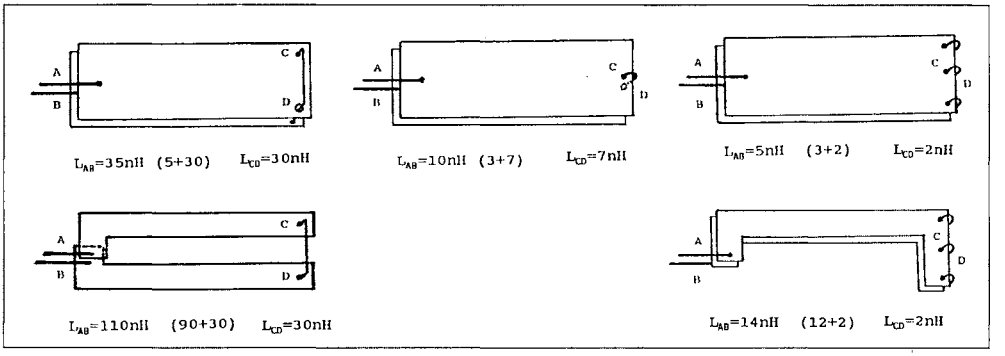


- The measurements are made with a dI/dt generator :
- I = 0 to 40Amps with a dI/dt = 1000A/s

The measurement of the induction voltage VL between A to B, and C to D, permits calculation of L = V_L / (dI/dt)

MEASUREMENT RESULTS

Figure 11.



MEASUREMENT CONCLUSIONS

- Capacitors should be positioned in the same direction as direction of current flow.
  Compare : a. to b.
- Several links between two large copper tracks are less inductive than a single link.
  Compare : b. to c.
- Every current path should be exactly above its return path on the other side of the board.
  Compare : d. to e.
- Decrease local dI/dt density by enlarging copper tracks.
  Compare : c. to e.