Synchronous Rectification in High–Performance Power Converter Design

— *By Robert Selders, Jr., Applications Engineer*

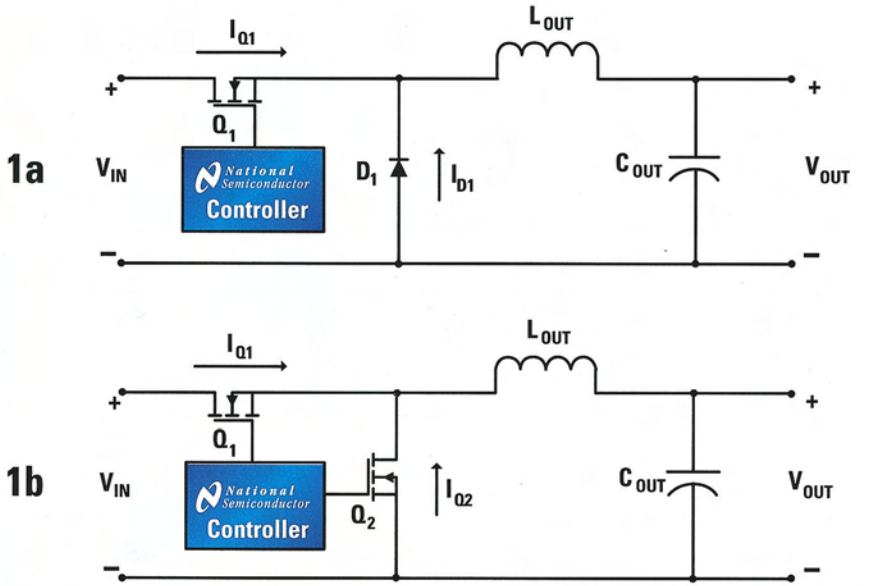

Figure 1. (a) Non-synchronous and (b) Synchronous Buck Converters

Power converters are becoming increasingly commonplace in the electrical industry. Product manufacturers and suppliers of electrical equipment are demanding ever-increasing functionality (i.e., lower input and output voltages, higher currents, faster transient response) from their power supply systems.

To meet these demands, switching power supply designers in the late 1990s began adopting Synchronous Rectification (SR)—the use of MOSFETs to achieve the rectification function typically performed by diodes. SR improves efficiency, thermal performance, power density, manufacturability, and reliability, and decreases the overall system cost of power supply systems. This article will examine the advantages of SR and discuss the challenges encountered in its implementation.

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Drawbacks of Diode Rectification

Nonsynchronous and synchronous buck converters are shown in ***Figure 1***. A nonsynchronous buck converter uses a FET and Schottky diode as its switches ***(Figure 1a)***. When the FET turns on, energy is delivered to the output inductor and the load. When the FET turns off, the current in the inductor commutates to the Schottky diode. Provided the load current is higher than half the ripple current of the output inductor, the converter operates in the continuous conduction mode.

The Schottky diode is selected by its forward voltage drop and reverse leakage current characteristics. But as output voltages drop, the diode's forward voltage is more significant which reduces the converter's efficiency. Physical limitations prevent the forward voltage drop of diodes from being reduced below approximately 0.3V.

In contrast, the on resistance, R_{DSON}, of MOSFETs can be lowered, either by increasing the size of the die or by paralleling discrete devices. Consequently, a MOSFET used in place of a diode can have a significantly smaller voltage drop at a given current than the diode.

This makes SR attractive, especially in applications sensitive to efficiency, converter size, and thermal performance, such as portable or handheld devices. MOSFET manufacturers are constantly introducing new MOSFET technologies that have lower R_{DSON} and total gate charge, (Q_G), which makes it easier to implement SR in power converter design.

What is Synchronous Rectification?

In the synchronous buck converter, for example, the efficiency is increased by replacing the Schottky diode with a low side MOSFET ***(Figure 1b)***. The two MOSFETs must be driven in a complimentary manner with a small dead time between their conduction intervals to avoid shoot–through. The synchronous FET operates in the third quadrant, because the current flows from the source to the drain. In contrast to its nonsynchronous counterpart converter, the synchronous buck converter always operates in continuous conduction, even down to no load.

During the dead time periods, the inductor current flows through the lower FET's body diode. This body diode usually has a very slow reverse recovery characteristic that can adversely affect the converter's efficiency. An external Schottky diode can be placed in parallel with the low-side FET to shunt the body diode and prevent it from affecting the converter's performance. The added Schottky can have a much lower current rating than the diode in a nonsynchronous buck converter because it only conducts during the small dead time (which is typically less than a few percent of the switching cycle) when both FETs are off.

Benefits of Synchronous Rectification

The advantages of using SR in high-performance, high-power converters include better efficiency, lower power dissipation, better thermal performance, lower profile, increased quality, improved manufacturing yields though automated assembly processes (higher reliability), and inherently optimal current sharing when synchronous FETs are paralleled.

As mentioned above, a number of MOSFETs can be paralleled to handle higher output currents. Because the effective R_{DSON} in this case is inversely proportional to the number of paralleled devices, conduction losses are reduced. Also, the R_{DSON} has a positive temperature coefficient so the FETs will automatically tend to share current equally,

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facilitating optimal thermal distribution among the SR devices. This improves the ability to remove heat from the components and the PCB, directly improving the thermal performance of the design. Other potential benefits from SR include smaller form factors, open frame configurations, lower profiles, higher ambient operating temperatures, and higher power densities.

Design Trade-Offs in Synchronous Rectified Converters

In an effort to minimize the size of the converter and decrease output ripple voltage for low-voltage applications, designers often increase the switching frequency to reduce the size of the output inductor and capacitor. If multiple FETs are paralleled, this increase in frequency can also increase gate drive and switching losses.

Design trade-offs must be made on a per-application basis. For example, in a high input voltage, low output voltage synchronous buck converter, since the operating conditions are such that the high-side FET has a significantly lower RMS current than the low-side FET, the high-side FET should be chosen with less Q_G and higher R_{DSON}. It is more critical to lower switching losses for this device than conduction losses. Conversely, the low-side FET carries more RMS current so its R_{DSON} should be as low possible.

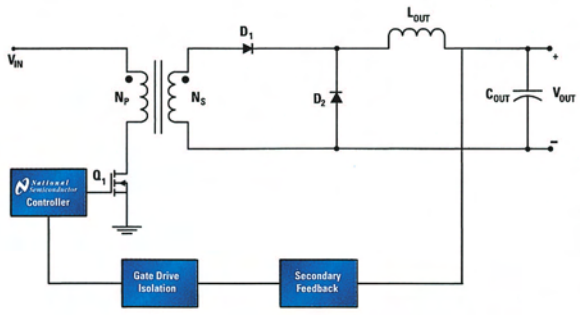

Figure 2. Isolated power converter with output synchronous rectification

Selecting controllers with stronger gate drivers in synchronous converters reduces switching losses by minimizing the time the FETs take to switch. However, faster rise and fall times generate high frequency noise that can lead to system noise and EMI compliance issues.

Driving Synchronous Rectifiers in Isolated Topologies

Power converters utilizing isolated topologies are used in systems requiring galvanic isolation among system grounds. Such systems include distributed bus architectures, Power-over-Ethernet systems, and wireless basestations. *(Figure 2)*.

Using SR in isolated converters can improve their performance significantly. All isolated topologies: forward, flyback, push-pull, half and full bridge (current and voltage fed), can be synchronously rectified. However, providing adequate and well-timed gate drive signals to the SRs in each topology presents its own set of challenges.

There are basically two types of drive schemes for FETs on the secondary stage of isolated topologies: self-driven gate signals taken directly from the secondary transformer windings, and control-driven gate signals derived from the PWM controller or some other primary referenced signal. For a given application several different implementations of these drives are possible. The designer should choose the simplest solution that also meets the performance requirements.

The self-driven scheme is the simplest, most straight forward SR drive scheme *(Figure 3)* and works well in topologies where the transformer

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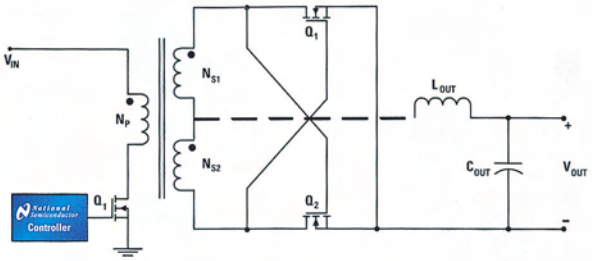

Figure 3. Self-driven synchronous rectification output stage

voltage is not zero for any significant period of time. Two SR FETs replace the output rectifier diodes, and voltage generated across the secondary windings drives the gates of the SRs. In most cases, higher or lower output voltages can be achieved with same topology by utilizing a different transformer turns ratio (N_P:N_{S1}:N_{S2}) and by appropriately selecting the SR FETs.

The main problem with self-driven SRs in topologies where the transformer voltage periodically goes to and stays at zero is that there is no signal to drive the gates of the SR FETs during these intervals. During these times, body diodes of the SRs conduct the load current, thus increasing power losses. Lower output voltages may require additional windings to increase the normal operating voltage applied to the SR FET gates to an adequate level.

Because the secondary winding voltage varies with input line voltage, the voltage on the SR gates will vary. The efficiency is impacted because R_{DSON} depends on the gate-source voltage (V_{GS}). In wide input voltage range converters this R_{DSON} variation can be as high as 2:1.

There are alternate gate drive techniques that can be employed for transformer-based topologies. In low-voltage, high-current applications, these drive techniques both reduce losses associated with the dead time intervals and produce nearly constant-amplitude gate drive pulses so efficiency is not adversely impacted by varying line voltages.

Control-driven schemes tend to solve the limitations of self-driven methods. However, they are typically more complex and expensive *(Figure 4)*. Depending on how parts-intensive the self-driven scheme is, a control-driven scheme may actually be the better alternative. The control signals used to drive the SR FETs can be derived from a primary or secondary side referenced controller.

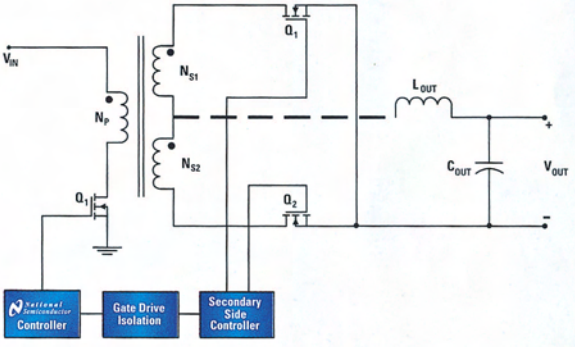

Figure 4. Control-driven synchronous rectification output stage

Conclusion

Synchronous switching power converters give better performance than nonsynchronous converters in low output voltage, high output current systems applications. Ensuring the proper timing of the gate drive signals for the SRs is an important task that designers must address to maximize converter performance. ■

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