EDN | DESIGN IDEAS

EDITED BY BILL TRAVIS & ANNE WATSON SWAGER

Circuit protects FPGAs from killer spikes

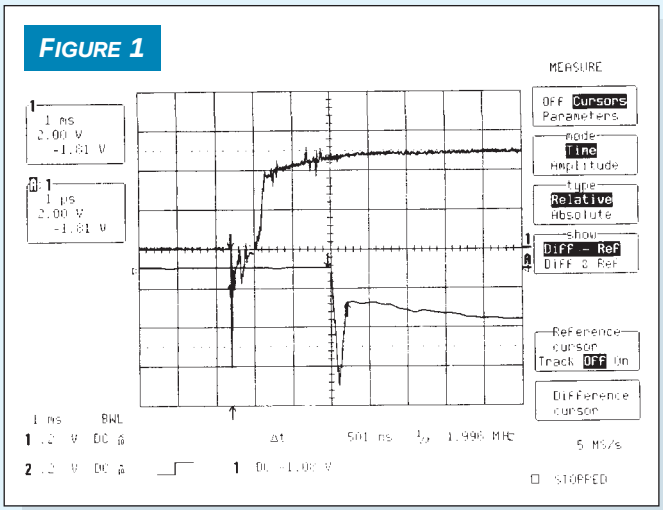
NELSON NGUYEN, ANRITSU CORP, MORGAN HILL, CA

A project using Xilinx FPGAs brought an interesting problem to light. When you turn on the board, one FPGA in three succumbs to this problem. A lot of frustration and testing uncovered a negative-going spike (**Figure 1**) in the 5V line from the dc/dc converter. The system uses a dc/dc converter to convert –48V to 5V and other voltages. The spike occurs before the converter delivers its intended 5V. Spikes greater than 5V would kill the FPGA with the shortest path to the converter. The circuit in **Figure 2** solves the problem.

Because the spike occurs before the 5V supply line turns on, to prevent the spike from destroying the FPGA, you should open the 5V path when you turn on the power switch and then close the path when the 5V supply voltage is present. The R_{19}-C_{13} RC network provides a delay in turning relay K_1 on. The turn-on voltage for K_1 is approximately 3.7V. The voltage divider comprising R_{19} and K_1's coil resistance (approximately 780Ω for an NEC EA2-5NU) provides a voltage at the junction of C_{13} and R_{19} sufficient to turn K_1 on. The value of C_{13} sets the delay at approximately 2 msec. (DI #2181) EDN

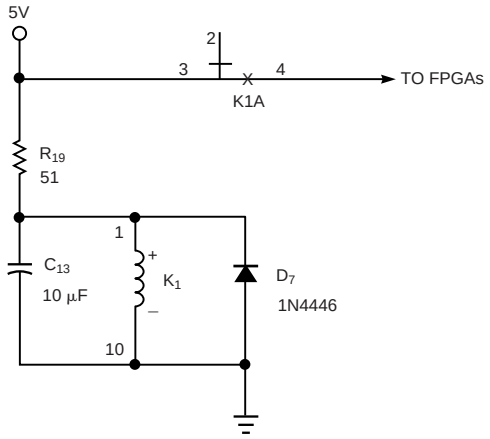
To Vote For This Design, Circle No. 366

FIGURE 1



A large negative spike (top waveform) in the turn-on waveform of the 5V supply line is an effective FPGA destroyer.

FIGURE 2



NOTE: K_1 = NEC EA2 – 5NU.

A simple RC network and a relay provide a 2-msec turn-on delay in the power-supply line to the FPGAs, thereby blocking the killer negative spike.