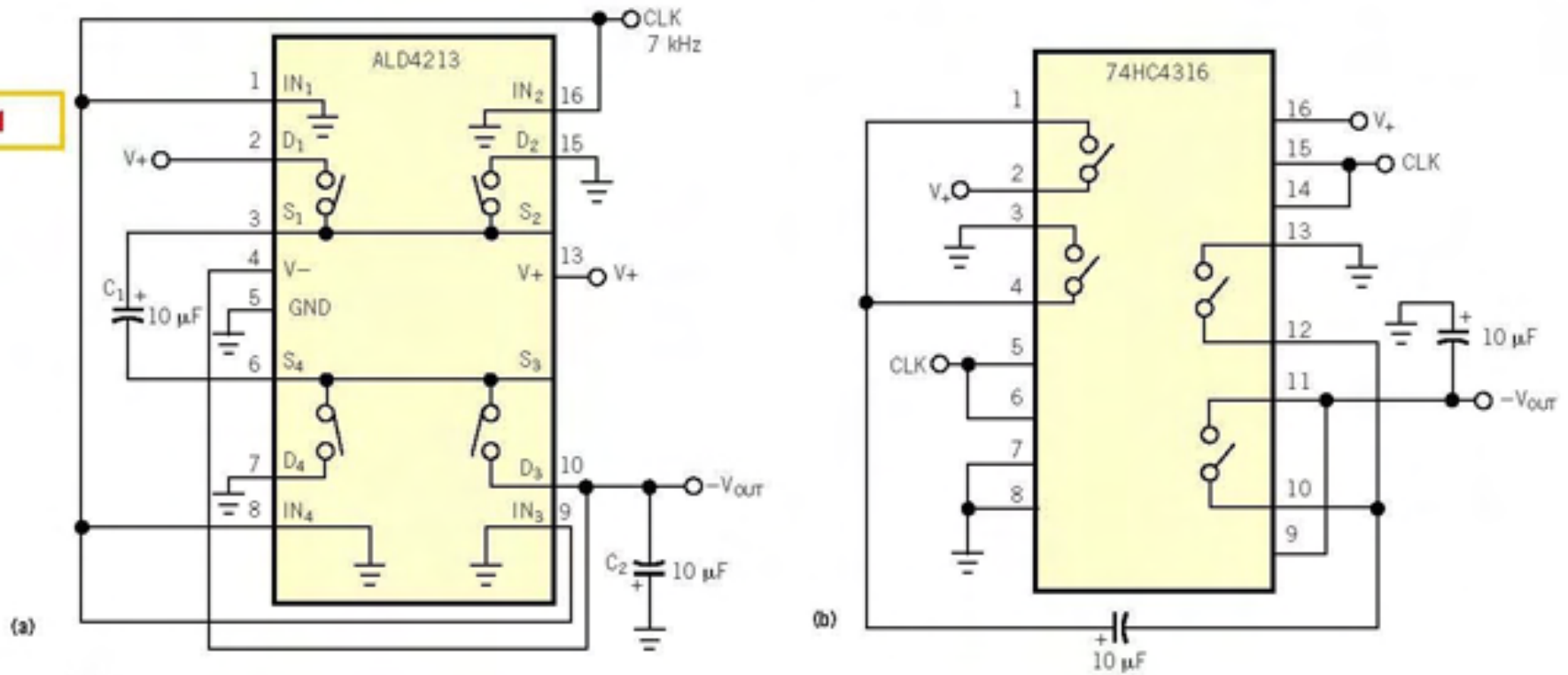
Analog switch acts as dc/dc converter

John P Skurla, Advanced Linear Devices Inc, Sunnyvale, CA

MANY LOW-CURRENT DEVICES that require 65V supplies can operate reliably in a single 5V power-supply environment if you use an appropriate localized dc/dc converter to generate the −5V bias. Often, the capabilities and advantages of these 5V ICs far outweigh the minor inconvenience and added costs of an additional −5V-converter function. Many companies manufacture dc/dc-converter ICs and modules in a variety of power ratings and footprints. However, these typical dc/dc converters can be overkill for simple, single-chip applications that require only a negative bias voltage with low operating currents. For these applications, typical negative-voltage requirements range from −4 to −6V with a supply current of 1 mA, and requirements for the −5V supply are generally noncritical.

A lower cost alternative to conventional dc/dc converter modules for generating negative dc voltages from a posi-

Figure 1



NOTES:
2V≤V+≤5V.
CLK IS CMOS LOGIC LEVEL WITH FREQUENCY OF 5 TO 500 kHz.
V+ IS THE DC-TO-DC INPUT.
$-V_{OUT}$ IS THE DC-TO-DC OUTPUT.

Using an analog switch with two external capacitors and an external clock is a viable way to produce 25V from a 5V input for low-power, −5V needs. One approach uses only one phase of the clock (a); a second approach requires both phases (b).

tive supply uses a low-cost quad- semiconductor analog switch and an onboard system clock (**Figure 1a**). This type of voltage converter generates a low-power, negative bias voltage from a 5V input. This circuit emulates charge-pump dc/dc converters, which are suitable for generating an output voltage whose polarity is opposite that of the input voltage. Two charge-storage capacitors are also necessary, as with conventional converters. Unlike the conventional self-contained dc/dc converter approach, this circuit requires a single external clock input to sequence the switches on and off and approximately the same amount of pc-board space. You can tap this clock from any 5V logic-gate output with continuous, regular periods of 5- to 500-kHz signals.

Charge-pump converters operate by first charging up one capacitor and alternately transferring that charge to another capacitor using a switching circuit. The switching circuit in **Figure 1a** alternately charges and discharges C_1 and C_2 to generate a −5V output from a 5V input. Integrated level translators and logic gates inside the ALD4213 analog switch provide the logic translation to convert a single 5V input to a ±5V logic swing.

The circuit closes two switches, S_1 and S_4, under clock control. During the first half of a clock cycle, C_1 charges up to a voltage equal to the input voltage, V+. The next half-cycle of the clock control opens S_1 and S_4 and closes S_2 and S_3. C_1 now connects across C_2 through S_2 and S_3, and the charge on C_1 subsequently transfers to C_2 until the voltage across both C_1 and C_2 is equal. Notice the "inverted" polarity across C_2, which forces the output voltage on C_2 to be V−, or the opposite of V+.

Each subsequent clock cycle, which again begins with the closing of S_1 and S_4, causes C_1 to charge up from the previous voltage to V+. After many repeated clock cycles, the voltage on C_2 remains charged to a value equal to the negative of V+, or close to it; it performs the function of a voltage inverter, which is more commonly called a converter.

An alternative analog-switch-based converter uses the industry-standard 74HC4316 quad analog switch with level translator (**Figure 1b**). The circuit is similar to the circuit in Figure **1a** but has different pin connections. This circuit also requires both phases of the clock. You can use an additional inverting logic gate to generate both clock phases if necessary. The recommended input is a logic clock that has a useful frequency range of 5 to 500 kHz.

Figure 1a's single-phase design costs less than $1 in large quantities. The cost of the circuit in **Figure 1b** can be less than half the cost of the circuit in **Figure 1a** provided that both clock phases exist and that you don't have to add an external logic-gate inverter. You can also integrate analog-switching inverters with other analog functions in a custom ASIC; the ALD4213 and ALD500A are compatible with the company's library of standard cells. (DI #2476)