Source impedance and regulator stability

In the February and March *Circuit Surgery* columns I discussed some issues related to power supply design posted by **Tuurbo46/Rocket Ron** on the old *EPE Chat Zone* (and continued on *EPE's* new forum home on EEWeb: **www.eeweb.com/forum/**). Martin Walker responded to these articles with another forum thread on EEWeb, tagged with 'EPE Magazine' to highlight its relevance to *EPE*. He wrote: 'I have been enjoying the recent *Circuit Surgery* columns on power supplies and potential dividers in *EPE Magazine*. I love the way that Ian Bell tackles each subject, explaining the theory clearly from first principles using worked examples to aid understanding. I wondered whether *Circuit Surgery* would take a look at a subject that has always been a little fuzzy for me – switching power supply source impedance and how to mitigate for it. We all know the rule of thumb that the source impedance of the input to a voltage regulator must be lower than the negative input impedance of the converter (negative because the line voltage drops when more current is taken by the regulator) by a factor of at least 10 times. We also know that if the source has a high impedance (e.g., long wires from the source to the regulator) then this can be mitigated with some input capacitance, usually a large-value electrolytic. What's not clear to me is how big that capacitor should be for a given source impedance. Explanations range from the highly mathematical to the generic 'use a 470µF for everything'. Is there a way to work out a suitable minimum capacitance value, based on the estimated or calculated impedance of the source?'

First, thanks to Martin for his positive comments about the articles. Martin obviously has some familiarity with this topic, but we will step back a bit to explain some of the background, including basic switching regulator operation, before discussing some of the issues related to input capacitor selection.

The basic configuration, without any capacitors or filters added, is shown in Fig.1. A DC source provides a voltage (V_I) to the input of the regulator, which in turn delivers a regulated output voltage (V_O) to the load, R_L. V_O will remain (more or less) fixed for a certain range of source voltages – the input operating range of the regulator. V_O will also remain fixed as the load varies (again within limits), implying a variation in load current. In the context of Martin's question the regulator is assumed to be a switch-mode DC-DC converter.

As discussed in the February article, real voltage sources (e.g., batteries and mains-rectified and/or stepped down by a transformer) are not perfect, but can be represented by an ideal voltage source in series with a source resistance. Where a circuit is simplified to this form, it is known as a 'Thévenin equivalent circuit'. For sources such as batteries, R_S is referred to as the 'internal resistance'. Fig.1 shows the source/internal resistance for the voltage source and regulator (R_S and R_P respectively).

The regulator takes electrical power from the source, at voltage V_I and delivers it to the load at voltage V_O. The input power taken by the regulator is $P_I = V_I I_I$ (I_I is the regulator input current, see Fig.1). The output power delivered to the load is $P_O = V_O I_O$ (I_O is the regulator input current/load current). A real power supply will not deliver all of its input power to the load because it will require power to operate and some losses will occur. The ratio of input power to usable output power is the efficiency (η) of the regulator, where: $\eta = P_O/P_I$. Switching regulators can achieve 80% efficiency or better, but in the following discussion we will assume 100% efficiency to simplify things.

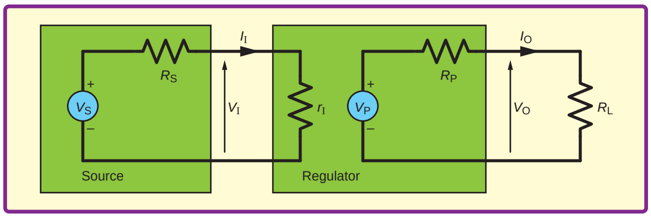

Fig.1. Power supply unit connected to a source and load

Fig.1 shows that the regulator has an input resistance; however, this is not a simple constant resistance. For an ordinary resistor, an increase in voltage across it will result in an increase in current through it, but *here*, because the regulator's power is constant (with constant load), increasing the input voltage *decreases* the input current. This opposite direction of change means that the effective input resistance of the regulator is negative (as mentioned by Martin). Furthermore, the input resistance of the regulator is not constant, so we refer to it as incremental or dynamic resistance and use a lower-case symbol, r_I.

Dynamic and negative resistance

For an ideal resistor, with resistance R, we have the well-known Ohm's law relationships $I = V/R$, $V = IR$ and $R = V/I$. If we plot a graph of current (I) against applied voltage (V) we get a straight line. The generic equation for a straight line is $y = mx + c$, where m is slope of the line and c is the value of y when $x = 0$. For a resistor, y corresponds to I and x to V. Zero voltage results in zero current, so $c = 0$ in the generic equation, leaving $y = mx$ or $I = (1/R)V$ – thus the slope of the line is $1/R$. A steep slope (large increase in current for a small increase in voltage) indicates a small resistance and vice versa.

The resistance of an ideal resistor does not change with voltage or current (the slope of the line of the *I-V* graph is constant). However, the resistance of other components is not always the same at different applied voltages. In such cases we cannot state a single value of resistance, but we can measure the slope of the line at any point on the curve of interest to find the (dynamic) resistance (r) at that point. We can do this by choosing two points close together on the curve (V_1, I_1) and (V_2, I_2) and then determine the slope at that point – the ratio of the change in the y value (I in this case) to the change in the x value (V in this case):

$$slope = \frac{1}{r} = \frac{\Delta I}{\Delta V} = \frac{I_2 - I_1}{V_2 - V_1}$$

Finding $1/slope$ gives the incremental resistance. The slope is most accurately determined if the difference between the two points is a small as possible. In the limit, the difference tends to zero and we write dV instead of ΔV. This takes us to the mathematics of calculus and the definition of dynamic resistance as the differential of the voltage-current relationship:

$$r_d = \frac{dV}{dI}$$

If current decreases as voltage increases then the slope is in the opposite direction to that of a resistor and the resistance is *negative*. (Note that we can still use small differences or differential calculus to find the resistance at a point of interest on the curve.)

Regulator dynamic input resistance

A regulator contains a negative feedback control loop, which attempts to keep its output voltage constant; this will result in changes in input current if the input voltage changes. However, initially consider the situation where the load and input voltage do not vary. We have $P_O = V_O I_O$ and $I_O = V_O/R_L$, in which V_O and R_L are constant due to the unchanging situation, so I_O is also constant and hence P_O is constant. Assuming 100% efficiency, the input power must also be constant and equal to P_I. Therefore $P_I = P_O = V_I I_I = V_O I_O$. From this we can also write $I_I = P_I/V_I = P_O/V_I = V_O I_O/V_I$. With everything constant we can consider the input resistance as a standard voltage/current ratio – this is referred to as the DC or static input resistance of the regulator, $R_{I,DC}$

$$R_{I,DC} = \frac{V_I}{I_I} = \frac{V_I^2}{V_O I_O}$$

Here, I_I was substituted with $V_O I_O/V_I$, as derived above. As an example, consider a DC-DC converter delivering V_O = 12V at I_O = 1A from a 24V input. The static input resistance is 24²/(12×1) = 48Ω.

One reason for having a regulator is to keep V_O constant as its source voltage varies. Given that $P_I = V_I I_I$ and P_I is constant, any increase in V_I will result in a proportional decrease in I_I. Under these conditions we need to consider the dynamic or incremental resistance. To do this, we assume that the input voltage changes by ΔV – that is, it changes from V_I to $(V_I + \Delta V)$. We can then use $I_I = V_O I_O/V_I$ to find the change in input current as it changes from $V_O I_O/V_I$ to $V_O I_O/(V_I + \Delta V)$. Using this in the definition of incremental resistance we get:

$$r_I = \frac{\Delta V}{\Delta I} = \frac{(V_I + \Delta V) - V_I}{\frac{V_O I_O}{(V_I + \Delta V)} - \frac{V_O I_O}{V_I}}$$

After some algebraic manipulation we get:

$$r_I = -\frac{(V_I + \Delta V)V_I}{V_O I_O}$$

ΔV is very small (tends to zero for dynamic resistance), so we can simplify this to:

$$r_I = -\frac{V_I^2}{V_O I_O} = -\frac{V_I}{I_I}$$

Which, by comparison with the equation above, can be seen to be the negative of the static resistance. This is a simplified analysis that assumes perfect regulation and 100% efficiency. In practice, the regulation is not perfect and the efficiency is not only less than 100%, but will vary with input voltage.

An important point here is the relationship between what the regulator is doing (in terms of regulation activity) and the effective input resistance of the regulator. To understand this we need to know something about how the regulator works. This will vary depending on the type of regulator, so we will just look at one example.

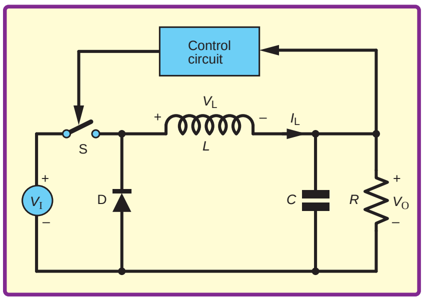

Fig.2. Basic switching converter schematic (buck converter)

Regulator operation

We will consider a switching regulator DC-DC converter that uses pulse-width modulation to control the output voltage. A simplified example circuit is shown in Fig.2 – this is a step-down buck converter ($V_I < V_O$). When the switch (S) closes, current flows from the source to the inductor and through the load. The inductor acts as an energy store (stored in its magnetic field). When the switch is open, the stored energy is released into the load, with the forward-biased diode providing the complete circuit for current to flow. When the switch is closed and the input voltage is connected across the diode, the diode is reverse biased and does not conduct.

When the switch closes the voltage across the inductor is $V_I - V_O$. If we assume V_O is constant (that is the job of the regulator) and V_I is also constant (for the situation under discussion) then the voltage across the inductor is constant at $V_I - V_O$. Applying a constant voltage to an inductor results in a constant rate of increase in current. This comes from the fundamental equation for the voltage-current relationship of an inductor:

$$V = L\frac{di}{dt}$$

Where i is the inductor current at a given time (t), V is the voltage across the inductor, L is the inductance. Again, we have differential equation: di/dt is the rate of change of current. If V and L are constant we can use $\Delta I/\Delta T$ instead of di/dt. From this we can write the inductor current change as:

$$\Delta I = \frac{V}{L}\Delta T$$

When the switch is open the voltage across the inductor is also constant and is equal to the load voltage, but opposite in sign (see the voltage orientations denoted on Fig.2). Under these conditions the inductor is outputting energy into the load and its current is ramping down at a constant rate – a negative slope of di/dt in the above equation corresponds with the negative voltage. Note that the inductor current flows in the same direction irrespective of switch position, but the relative polarity of the inductor and load voltage change by virtue of the switching arrangement. The switched nature of the circuit means that the output voltage has a tendency to vary (ripple) with the switching cycle, but this is smoothed by the capacitor (C).

The control circuit manipulates the time the switch is on in order to maintain the correct output voltage. The switch is activated on a cycle of constant duration T, so it is on for time DT, where D is the duty cycle – the fraction of time the switch is on for. In each cycle the switch is off for time $(1 - D)T$. The timing of the switch and corresponding inductor current waveform is shown in Fig.3. The control circuit varies the duration of the voltage pulse into the circuit, so this is a form of pulse-width modulation (PWM) control.

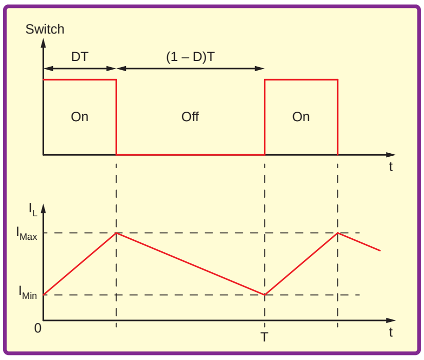

Fig.3. Timing and waveforms for the circuit in Fig.3

With the help of Fig.3 we can find the change of current $\Delta I = (I_{max} - I_{min})$ for the two parts of the cycle using the equation for ΔI given above. With the switch closed $\Delta t = DT$ and we have VI – V_O across the inductor, so

$$I_{max} - I_{min} = \frac{(V_I - V_O)}{L}DT$$

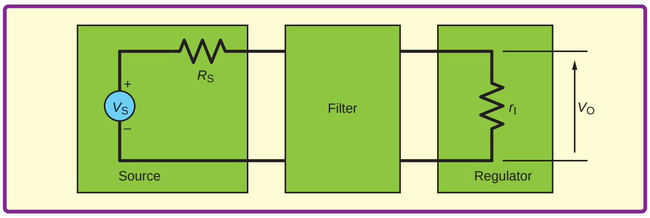

Fig.4. Regulator with input filter

With the switch open $\Delta t = (1 - D)T$ and we have $-V_O$ across the inductor, so:

$$I_{min} - I_{max} = \frac{-V_O}{L}(1 - D)T$$

As can be seen from Fig.4, the inductor current changes by the same amount in each part of the cycle. For steady operation we can equate the two ΔI equations:

$$\frac{(V_I - V_O)}{L} DT = -\frac{-V_O}{L}(1 - D)T$$

With a little algebraic manipualtion, this simplifies to:

$$\frac{V_O}{V_I} = D$$

Thus the control circuit will manipulate the duty cycle to set the output voltage. Given that (assuming 100% efficiency) $P_O = P_I = V_O V_I = I_O I_I$ so $V_O/V_I = I_I/I_O = D$ (using the equation above) we can also write $I_I = DI_O$ and $VI = V_O/D$. Returning to the equation for dynamic resistance and substituting for V_I and V_O we get:

$$r_I = -\frac{V_I}{I_I} = -\frac{V_O/_D}{I_O D} = -\frac{1}{D^2}\frac{V_O}{I_O} = -\frac{R_L}{D^2}$$

Thus, the dynamic input resistance is determined by the regulator's duty cycle and the load resistance. Similar equations can be obtained for regulators operating on different principles.

Input filter and capacitors

A low-pass filter is commonly inserted between the source and regulator input (see Fig.4). The purpose of this filter is to prevent any high frequency noise and interference from reaching the regulator. The filter also prevents the regulator from causing electromagnetic interference (EMI), either by conduction via the circuit, or by radiation. It blocks high frequencies from the regulator to isolate its switching noise from other circuits and wiring which might radiate signals. The filter can be implemented by just a capacitor across the regulator inputs, or as a simple LC filter, as show in Fig.5, but a number of other variations are possible.

Fig.5 shows a single input capacitor, however switching regulators often have multiple capacitors on their input; reflecting multiple roles for the capacitor(s) to:

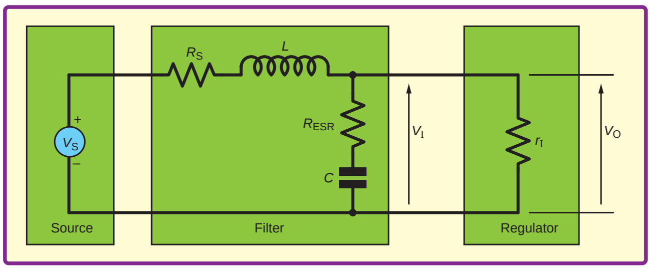

Fig.5. Fig.6. Regulator with example filter circuit model. This is a two-component LC filter, but the capacitor's ESR and the source resistance/inductor resistance will also influence the filter's characteristics.

- Smooth input voltage variation due to switching (ripple)
- Help cope with transient demands in load current
- Provide high-frequency bypass for the internal control circuits (for stability)
- Help shape the overall frequency response of the input filter.

Selection of capacitors is not simply a matter of the correct capacitor value. Real capacitors have effective series inductance and resistance (ESR), possible voltage dependence and ripple current ratings that need to be considered, along with physical and thermal characteristics. Thus, particular types of capacitor are likely to be more suitable than others and various trade-offs may need to be thought about. Typically, regulator datasheets provide guidance on capacitor selection. Multiple capacitors may be used because the imperfections and limitations of real components mean that one component cannot cover everything.

To look at ripple smoothing in a little more detail, we note that the regulator demands a varying input current from the source at the switching frequency (as shown in Fig.3), which in turn causes voltage variations due to inductance and resistance in the external circuit. These voltage and current variations are a potential source of EMI, as noted above. Connecting a suitable capacitor across the regulator input, as close as possible to the input, creates a bypass path at the relevant frequency, which shorts out any ripple. Typically, ceramic chip capacitors of units to tens of microfarads are used here, but when using a particular regulator IC, the datasheet should be consulted for details of capacitors selection.

When the regulator is responding to abrupt increases in load current it will in turn increase its input current demand. It is often the case that the source will not be able to respond quickly enough to meet this demand. Again, the effect of current variation is to cause voltage variation on the input, which in this situation is potentially large enough to disrupt regulator operation. The problem is most likely to occur if there is long wiring from the source to the regulator input and can be overcome by using a sufficiently large capacitor across the inputs, referred to as a bulk capacitor. Electrolytic capacitors of tens or hundreds of microfarads may be used for this purpose, but again, the datasheet may provide more specific guidance.

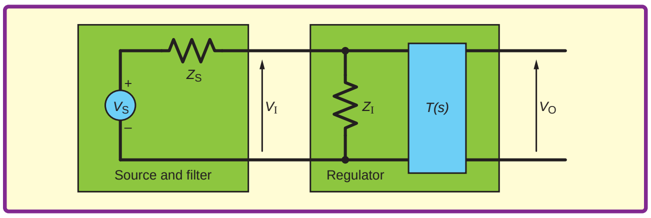

Fig.6. Regulator with example filter represented in the source impedance.

Source impedance and stability

The filter and source resistance can be combined into a Thévenin-style source impedance, as shown in Fig.6. We use Z_S rather than R_S to indicate that we dealing with a frequency-dependent impedance rather than resistance. Similarly, we represent the input to the regulator with impedance Z_I. The regulator's control circuit is represented by its transfer function $T(s)$, in which s is the Laplace complex frequency variable. As Martin indicates, a full analysis of the stability of the regulator's control circuit typically involves significant amount of mathematics, which is beyond the scope of this article.

We can get some insight into possible stability problems using Fig.6 without a full analysis. The overall relationship between the source voltage V_S and the regulator output is influenced by both $T(s)$ and the impedances Z_S and Z_I. In fact, Z_S and Z_I form a potential divider providing V_I to $T(s)$, so we can write:

$$\frac{V_O}{V_S} = \left(\frac{Z_I}{Z_S + Z_I}\right)T(s)$$

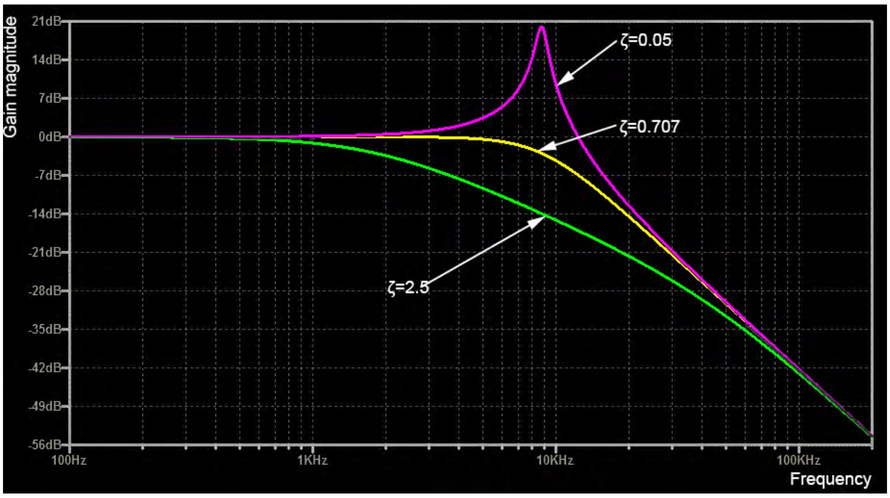

Fig.7. Typical filter response of an RLC second-order low-pass filter. This graph illustrates the general shape of the response and is not related to any specific regulator design

From this, we can conclude that if Z_S is much smaller than Z_I, then $Z_I/(Z_S + Z_I)$ will be close to unity and the relationship between V_O and V_S will be dominated by the control circuit $T(s)$. Under these conditions we assume the control circuit will be stable, but if Z_S becomes significant the behaviour of the system may change, with instability being a possibility. This leads to the rule of thumb that Martin mentioned that the magnitude of the source impedance should be at least ten times smaller than the magnitude of the regulator input impedance.

If the filter in Fig.5 is used, assuming $R_S = 0$ for simplicity, then we have a second-order RLC low-pass filter. The frequency response (see Fig.7) of this filter depends on the relative values of the components. Of particular important here is the parameter known as 'damping' (symbol ζ). If the damping is relatively high then the filter gain will decrease slowly past the cut-off frequency. With less damping the response will exhibit a peak near the cut-off frequency. This will effectively amplify the noise in the circuit at that frequency, and the condition discussed above ($Z_S << Z_I$) may not be met, so instability may occur. Suitable filter design can avoid this problem and there are a number of technical articles from semiconductor manufacturers that discuss regulator input filter design in detail.

If one performs a stability analysis of the system in Fig.6, with the filter from Fig.5 (again with $R_S = 0$) conditions for the relationship between r_I and the filter components to ensure stability can obtained. The results (for the particular situation discussed) are:

$$|r_I| > R_{ESR}$$

$$|r_I| > \frac{L}{CR_{ESR}}$$

If the resistance (R_{ESR} in this case) is low then these conditions may not be met – also, from another perspective, the RLC circuit damping will be low and the previously discussed condition ($Z_S << Z_I$) may not be met at all frequencies.

Martin has found 'highly mathematical' treatments because this is a complex topic – so we cannot provide a simple comprehensive answer, except perhaps to say read the datasheet of any switching regulator you use carefully and follow any component selection and board layout guidelines provided.